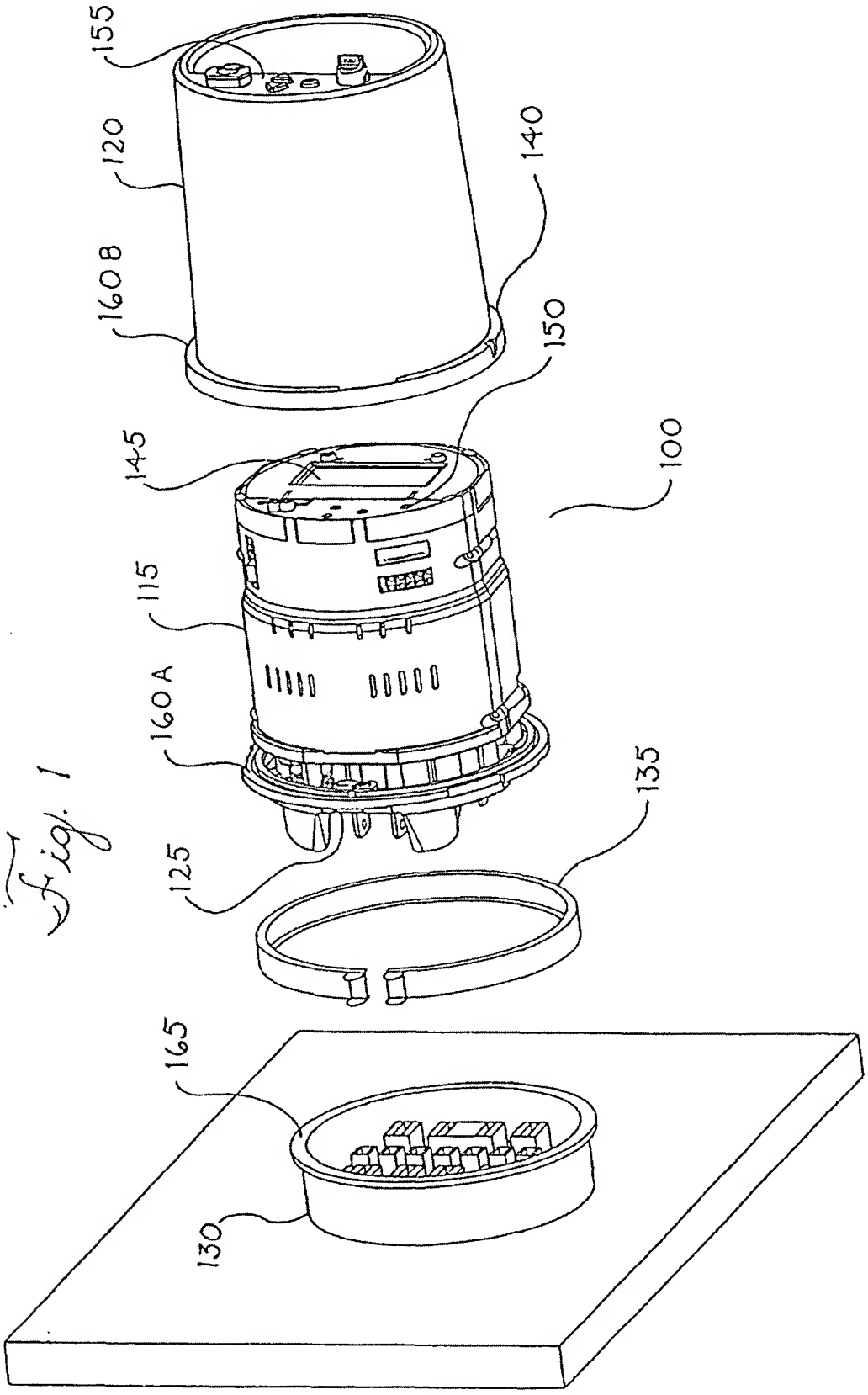
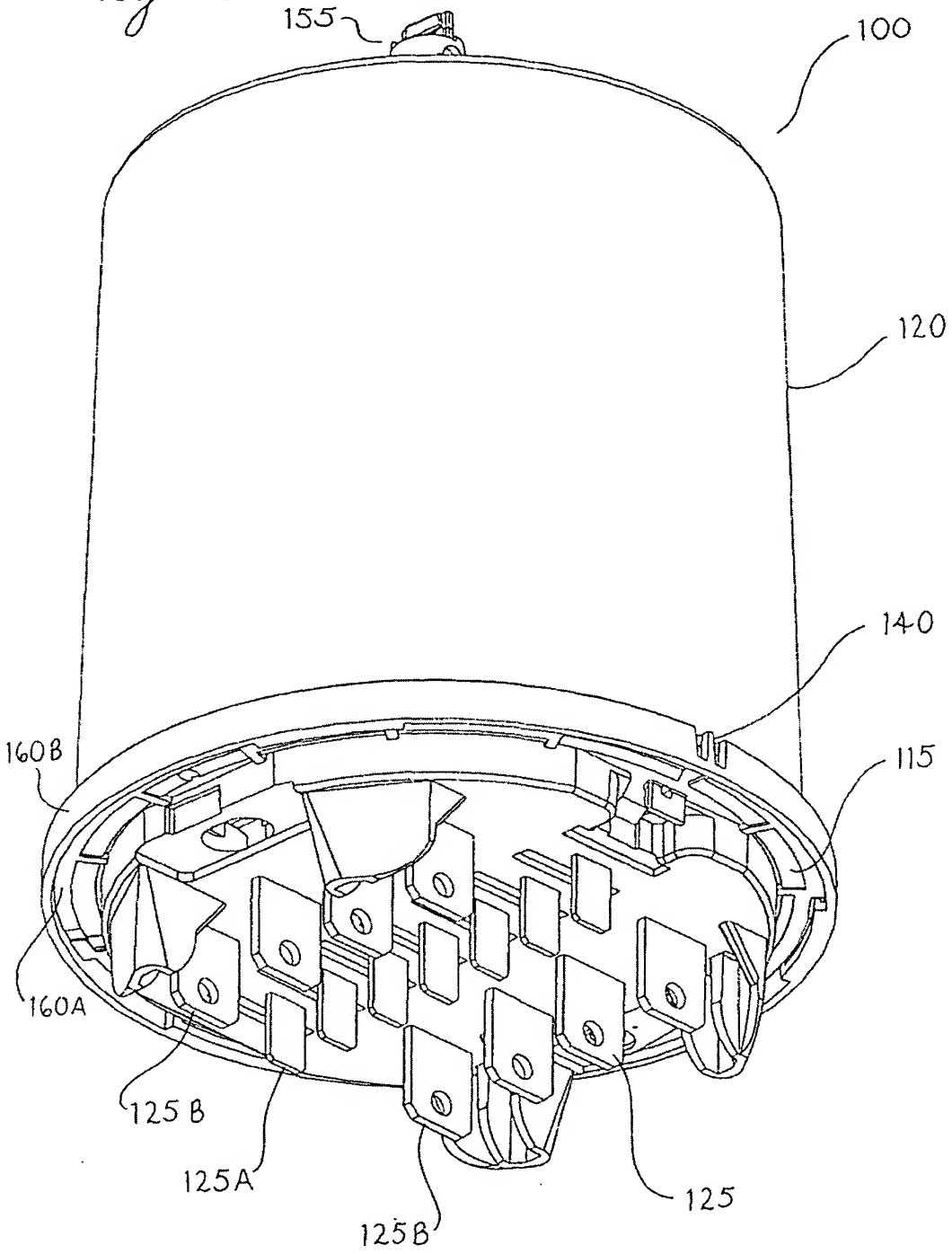


Fig. 1

Fig. 2



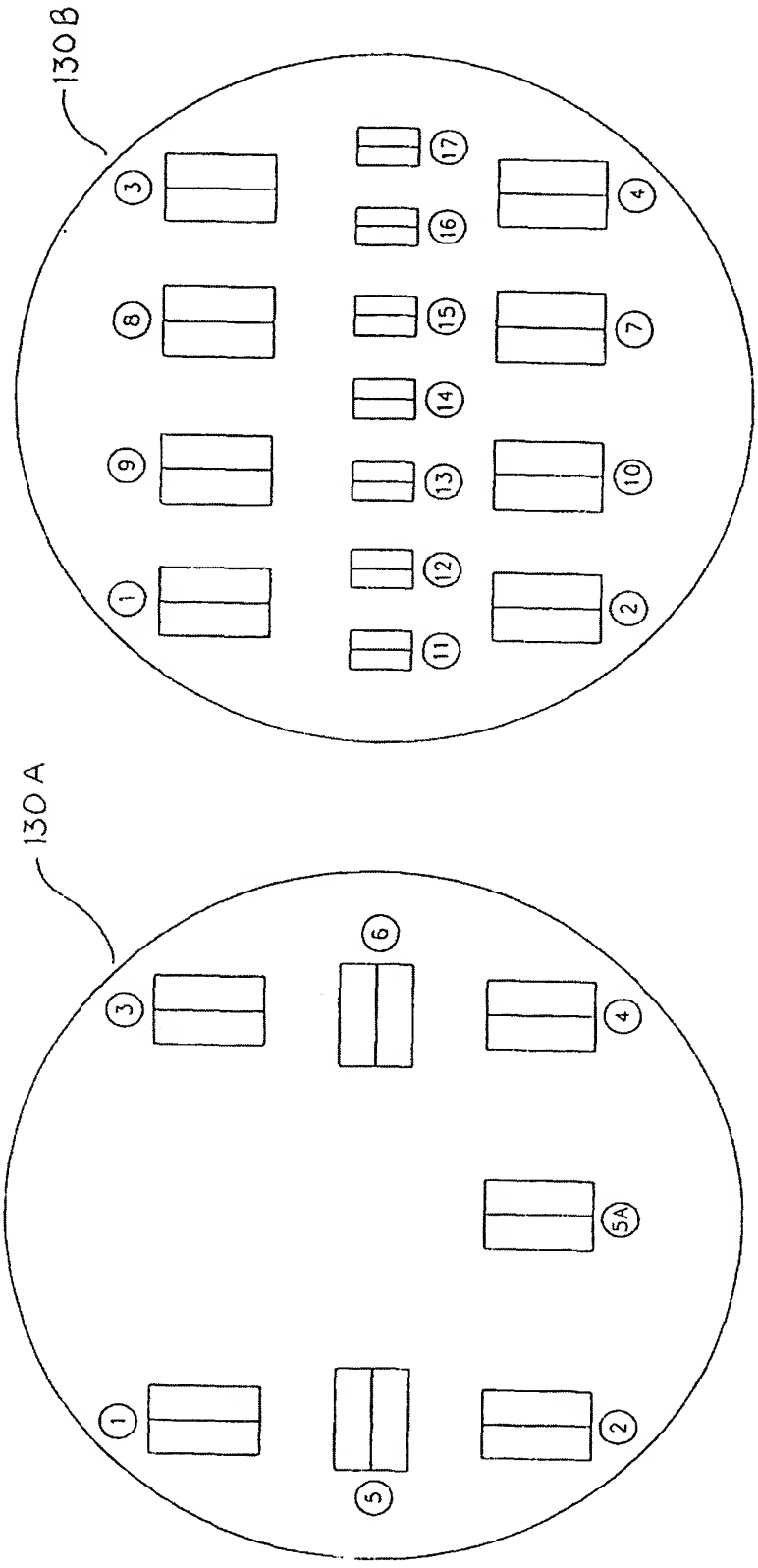


Fig. 3

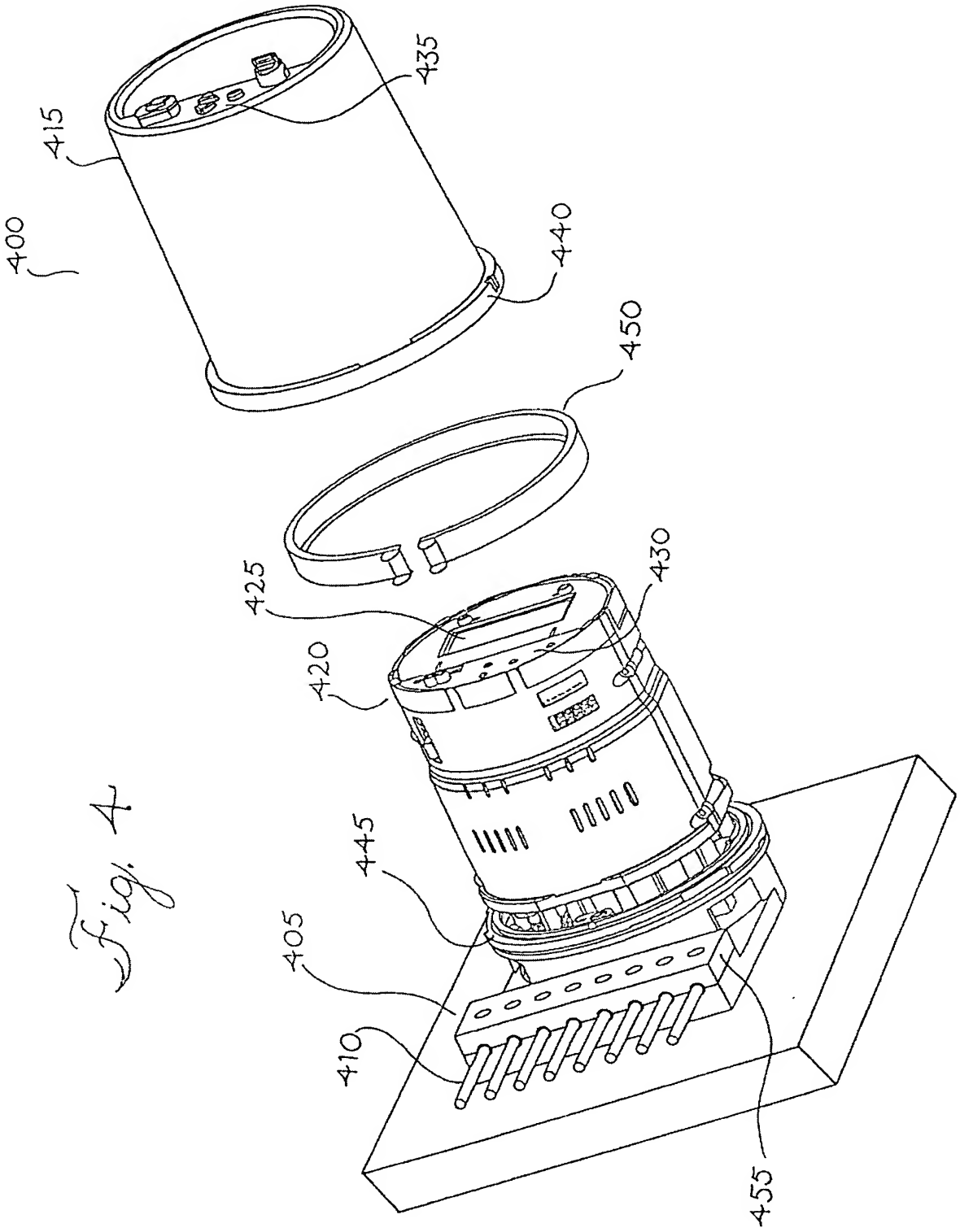


Fig. 4

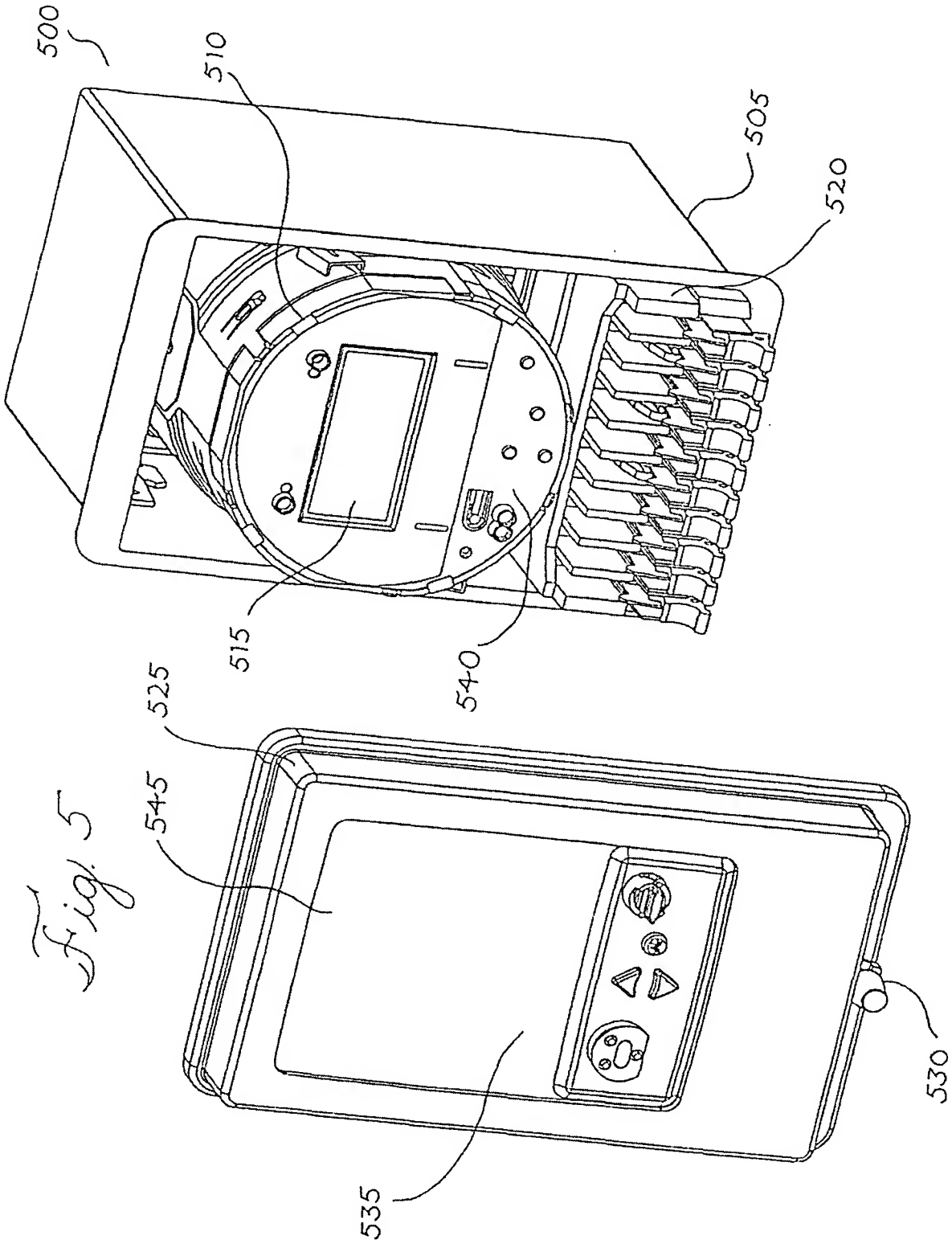


Fig. 5

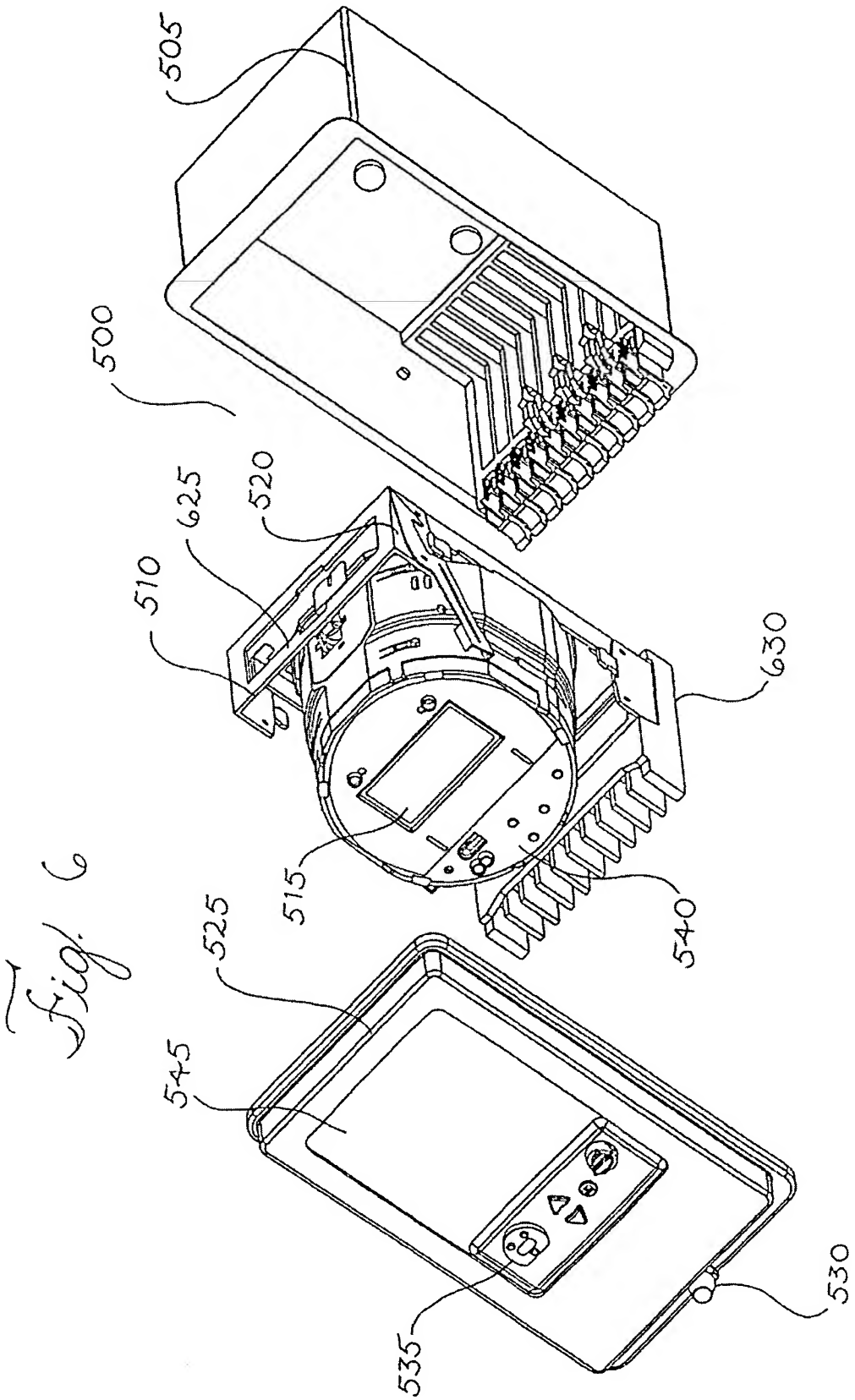


Fig. 6

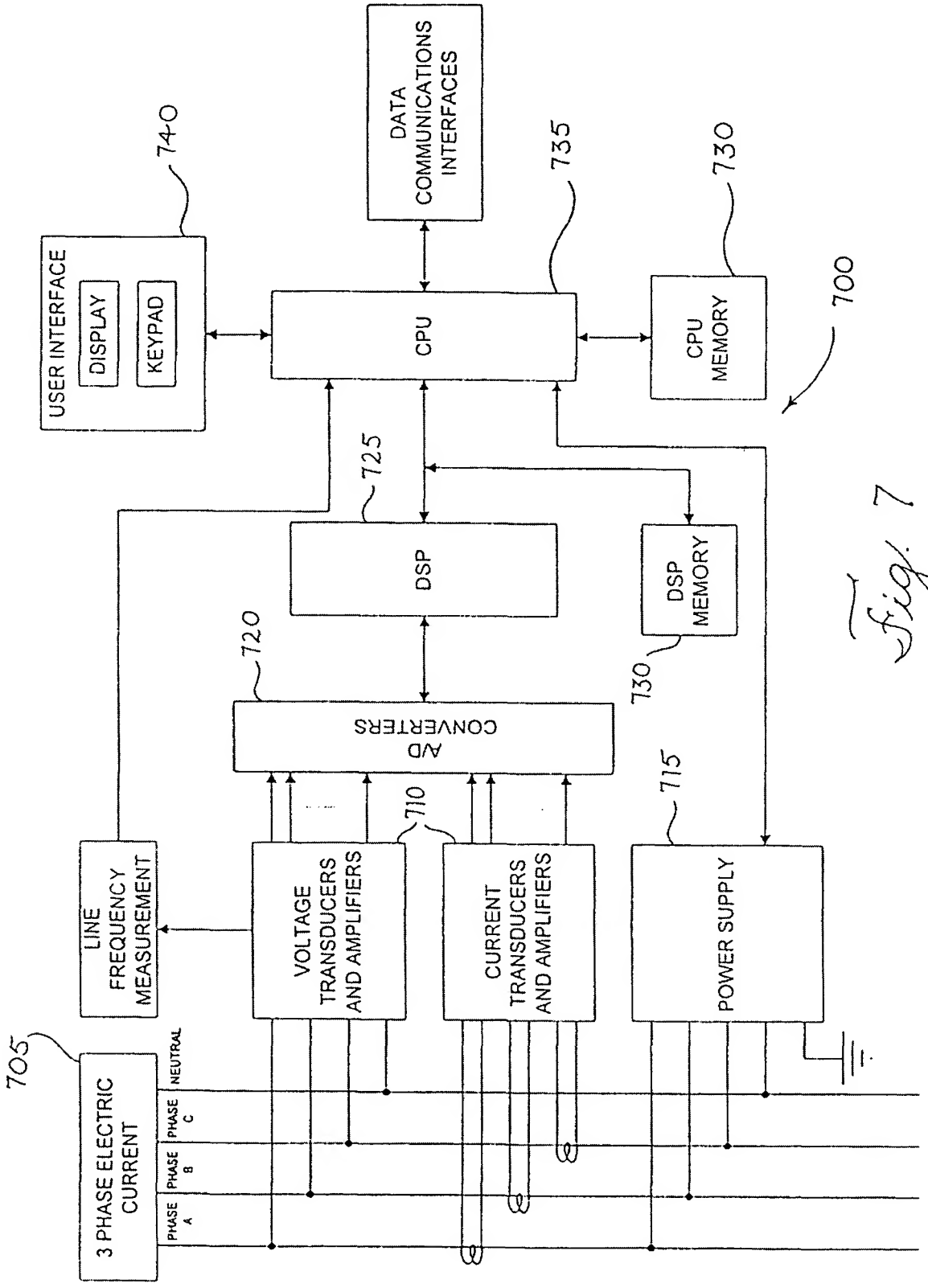

DATA COMMUNICATIONS INTERFACES
740
735
730
USER INTERFACE
DISPLAY
KEYPAD
CPU
CPU MEMORY
700
725
DSP
DSP MEMORY
720
730
A/D CONVERTERS
715
710
LINE FREQUENCY MEASUREMENT
VOLTAGE TRANSDUCERS AND AMPLIFIERS
CURRENT TRANSDUCERS AND AMPLIFIERS
POWER SUPPLY
705
3 PHASE ELECTRIC CURRENT
NEUTRAL
PHASE C
PHASE B
PHASE A

Fig. 7

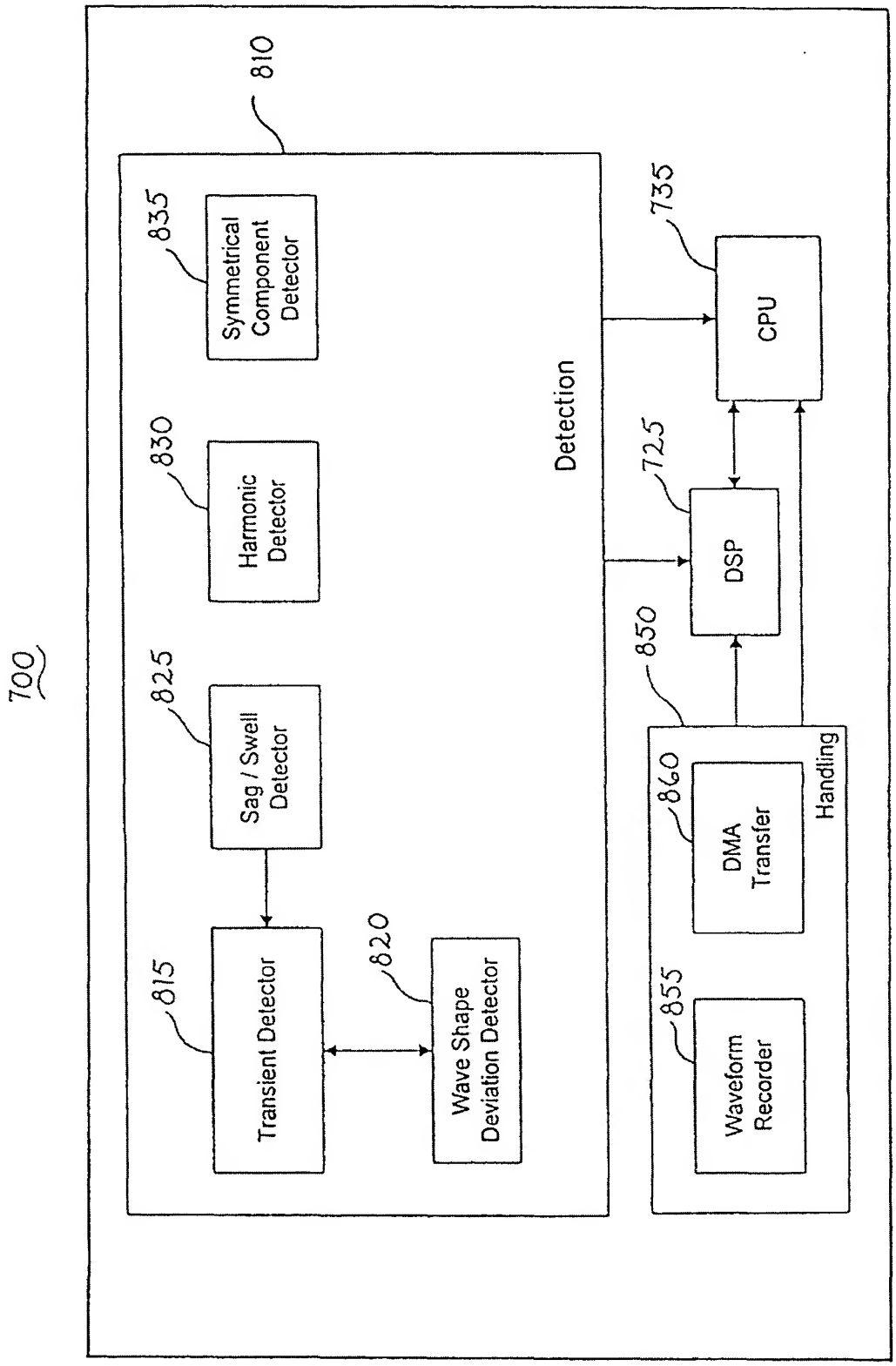

700
810
Detection
835
Symmetrical Component Detector
830
Harmonic Detector
825
Sag / Swell Detector
815
Transient Detector
820
Wave Shape Deviation Detector
735
CPU
725
DSP
850
Handling
860
DMA Transfer
855
Waveform Recorder

Fig. 8

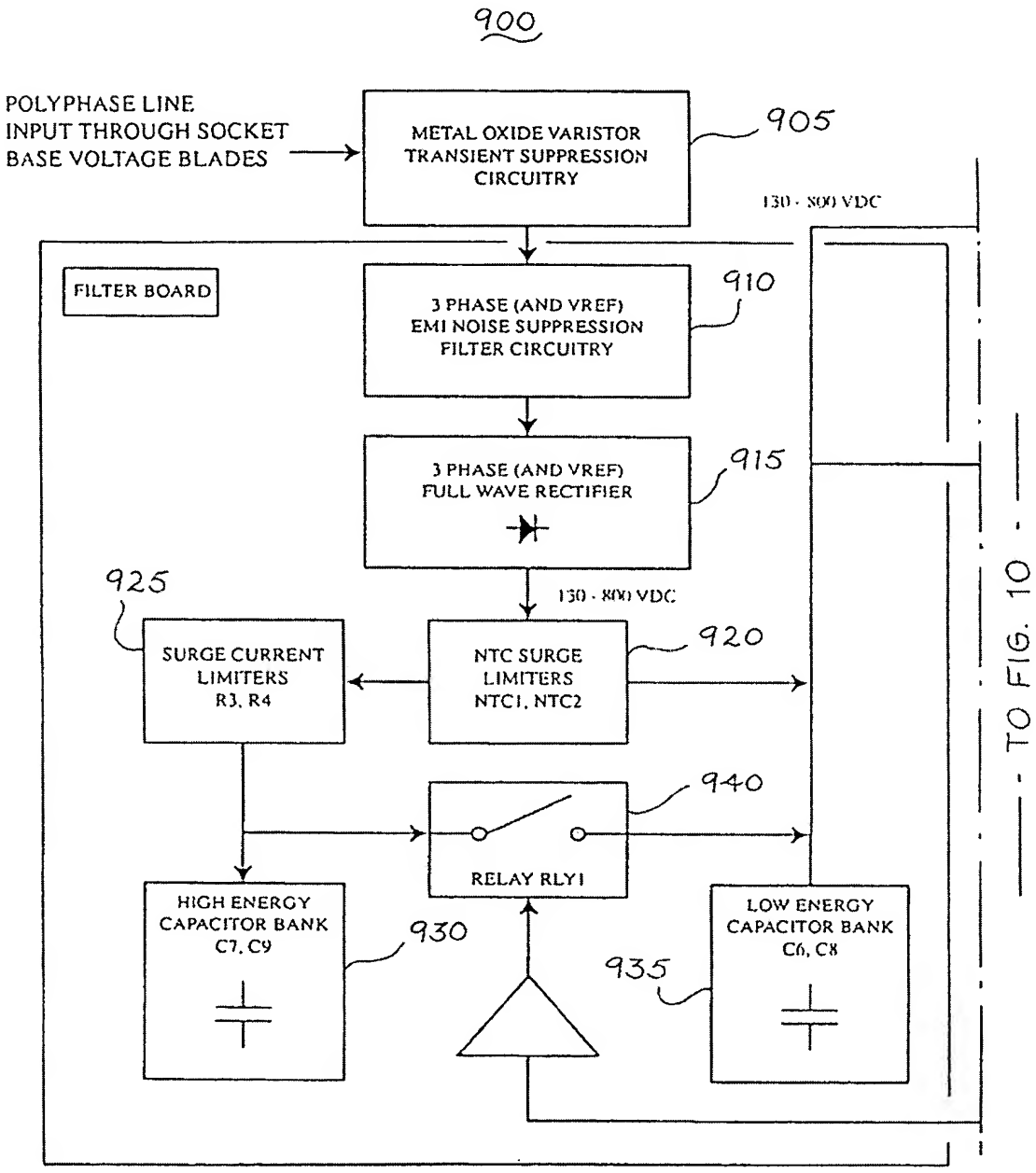

900
POLYPHASE LINE
INPUT THROUGH SOCKET
BASE VOLTAGE BLADES
METAL OXIDE VARISTOR
TRANSIENT SUPPRESSION
CIRCUITRY
905
130 - 800 VDC
FILTER BOARD
3 PHASE (AND VREF)
EMI NOISE SUPPRESSION
FILTER CIRCUITRY
910
3 PHASE (AND VREF)
FULL WAVE RECTIFIER
915
925
130 - 800 VDC
SURGE CURRENT
LIMITERS
R3, R4
NTC SURGE
LIMITERS
NTC1, NTC2
920
940
RELAY RLY1
HIGH ENERGY
CAPACITOR BANK
C7, C9
930
935
LOW ENERGY
CAPACITOR BANK
C6, C8
- TO FIG. 10 -

Fig. 9

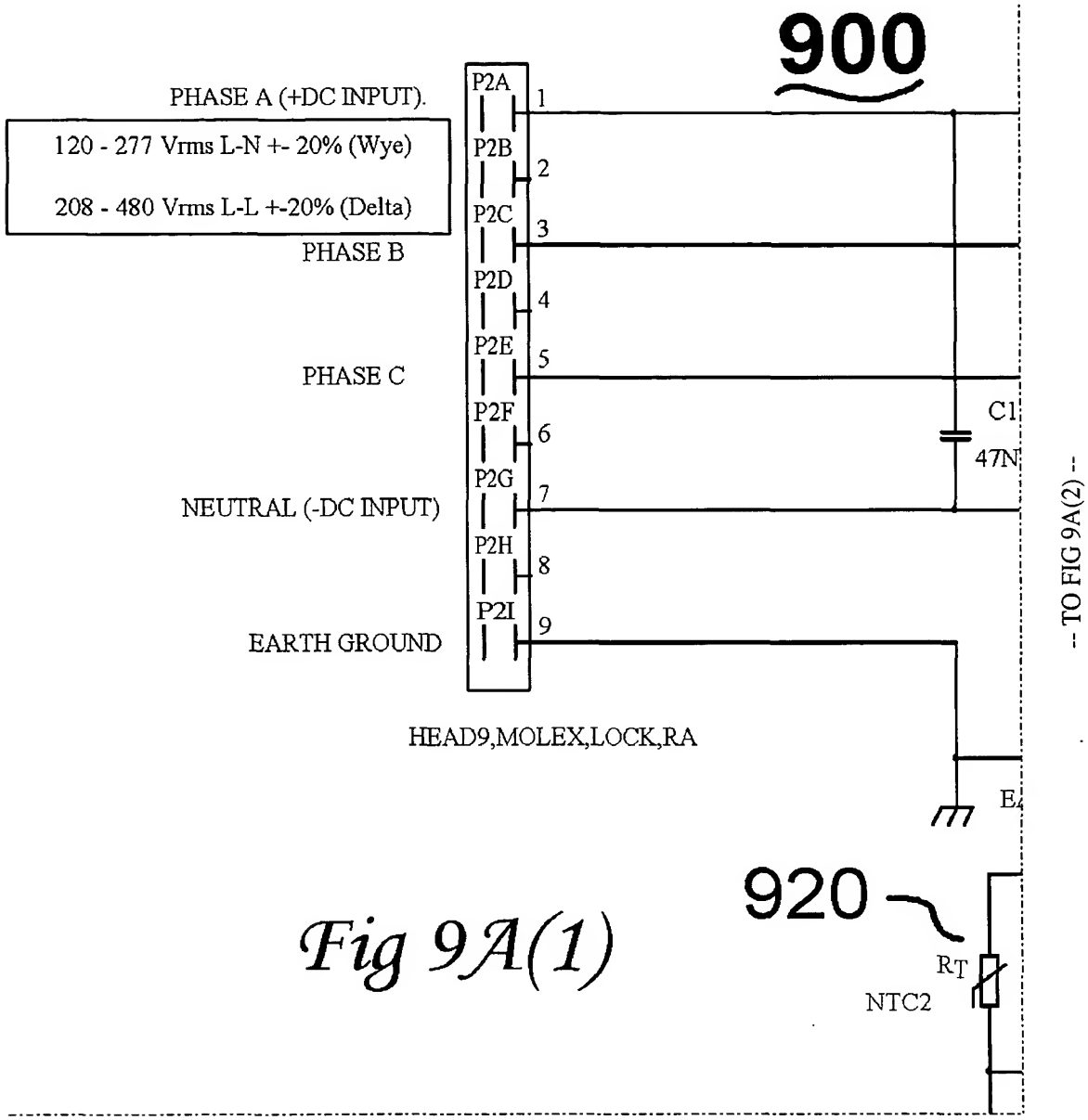
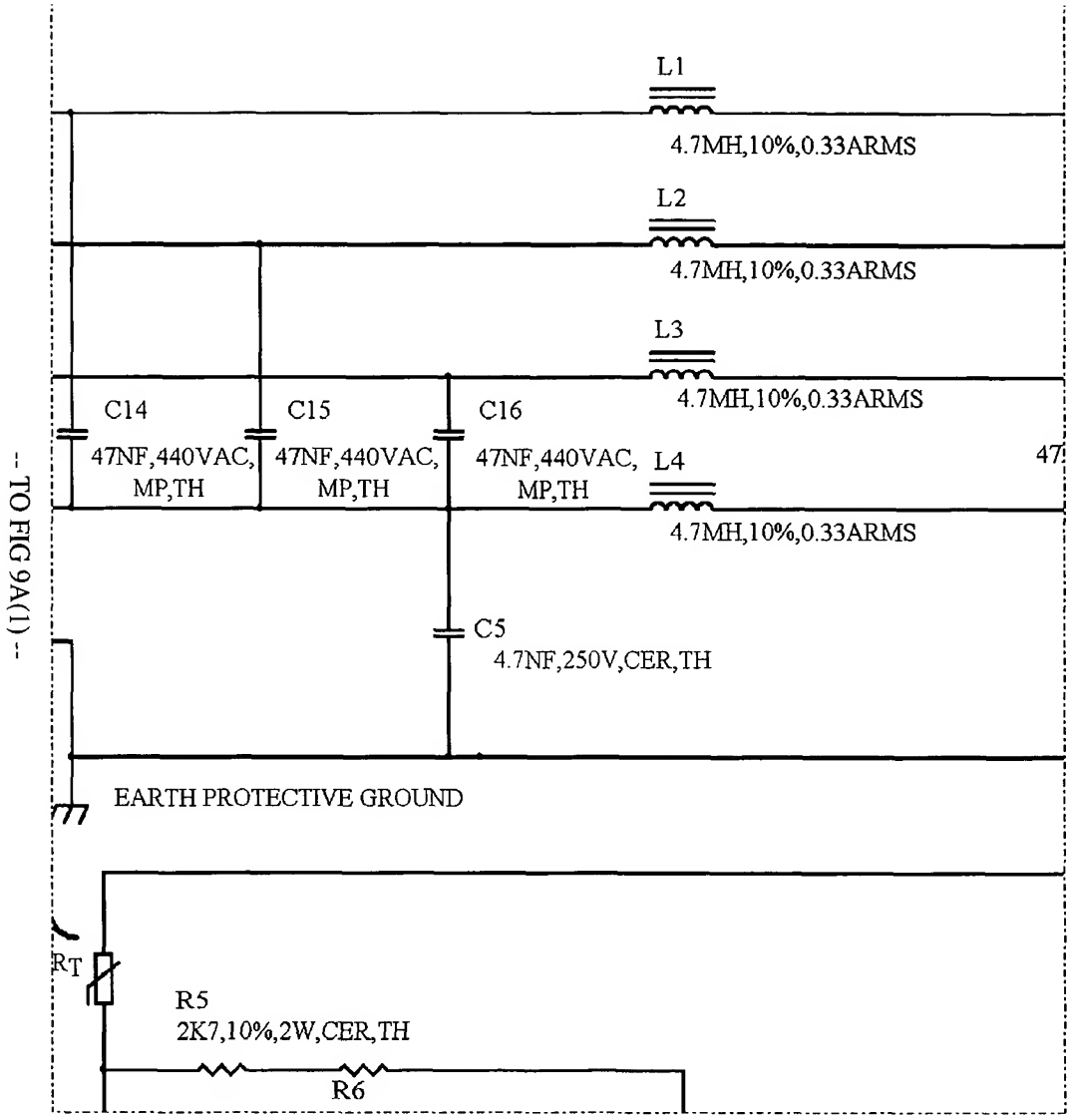


Fig 9A(1)

-- TO FIG 9A(5) --

Fig. 9A(2) (12/58)



-- TO FIG 9A(6) --

Fig. 9A(3) (13/58)

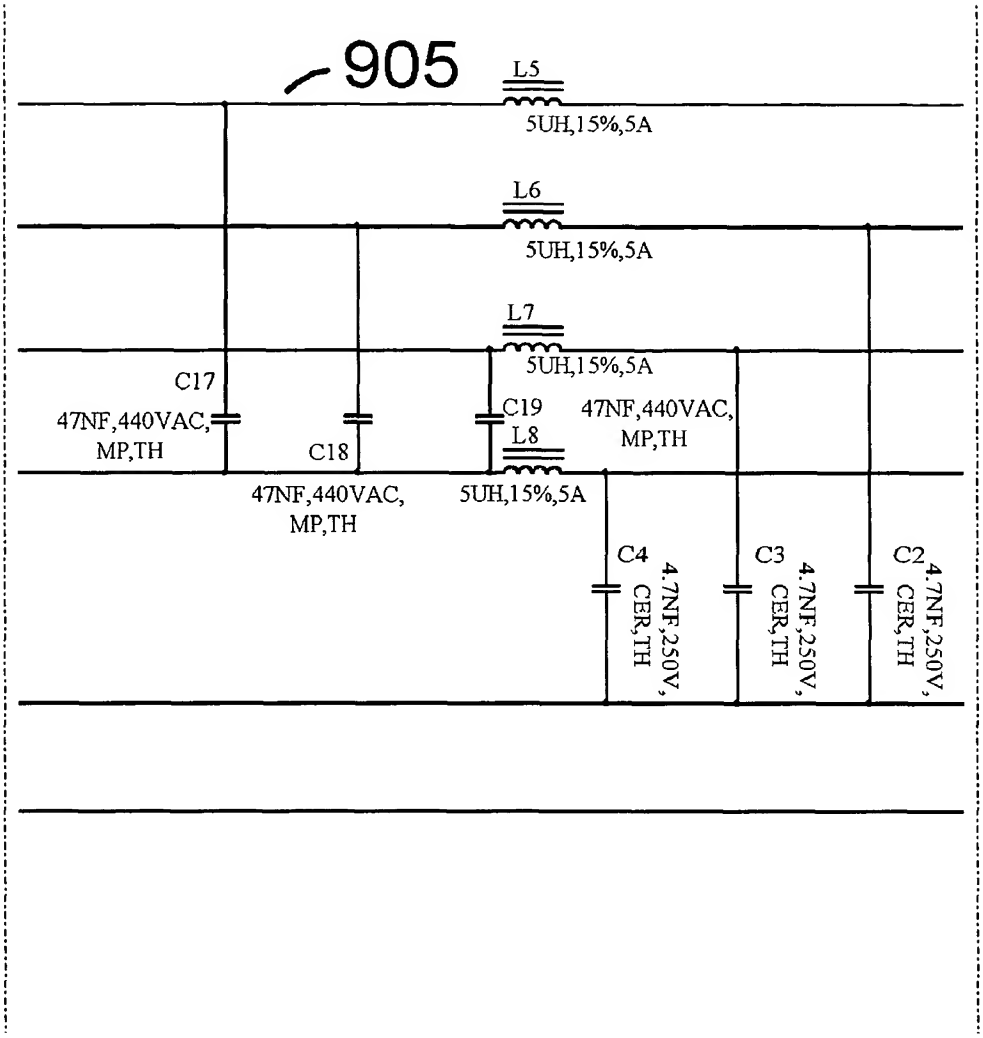

905
L5
5UH,15%,5A
L6
5UH,15%,5A
L7
5UH,15%,5A
C17
47NF,440VAC,
MP,TH
C18
47NF,440VAC,
MP,TH
C19
47NF,440VAC,
MP,TH
L8
5UH,15%,5A
C4
4.7NF,250V,
CER,TH
C3
4.7NF,250V,
CER,TH
C2
4.7NF,250V,
CER,TH
-- TO FIG 9A(2) --
-- TO FIG 9A(4) --

Fig. 9A(4) (14/58)

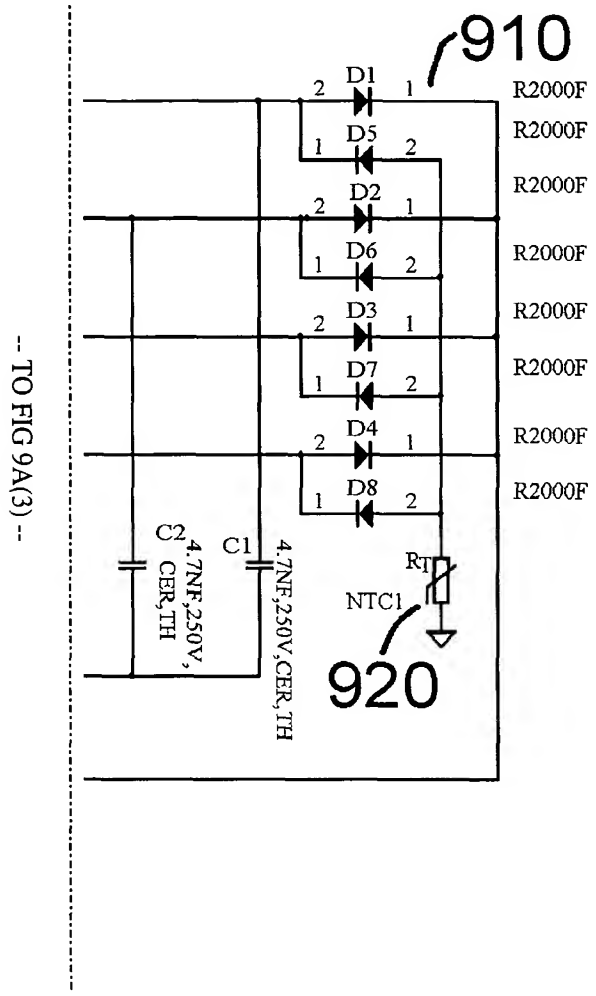
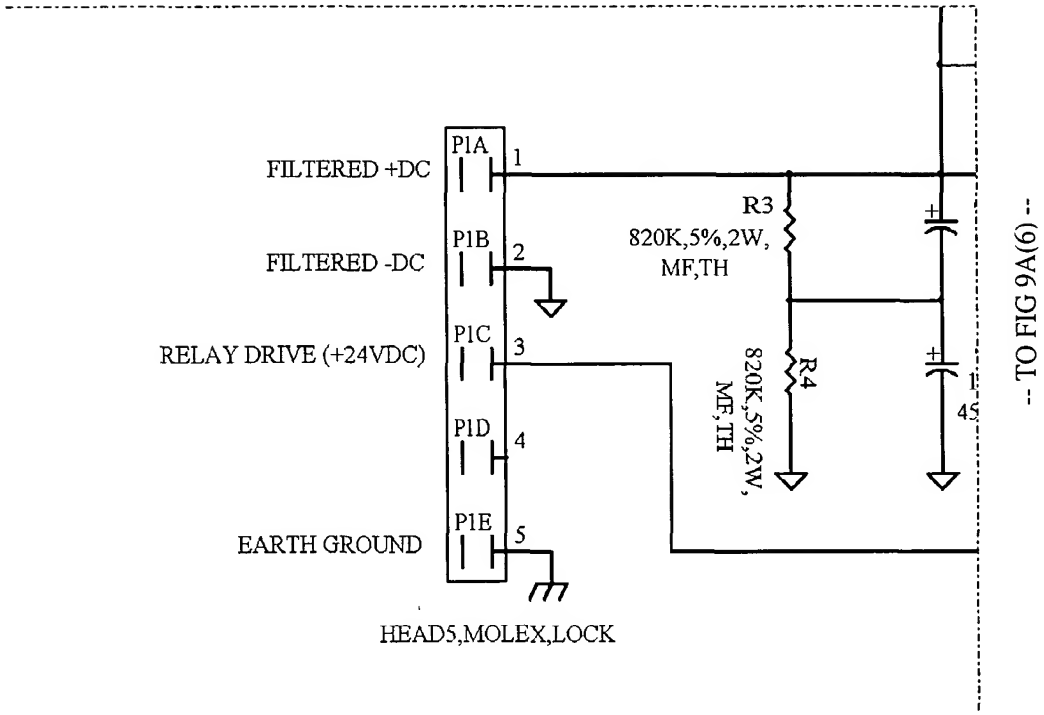

910
D1
D5
D2
D6
D3
D7
D4
D8
R2000F
R2000F
R2000F
R2000F
R2000F
R2000F
R2000F
R2000F
C2
4.7NF,250V,
CER,TH
C1
4.7NF,250V,CER,TH
RT
NTC1
920
-- TO FIG 9A(3) --

Fig. 9A(5) (15/58)

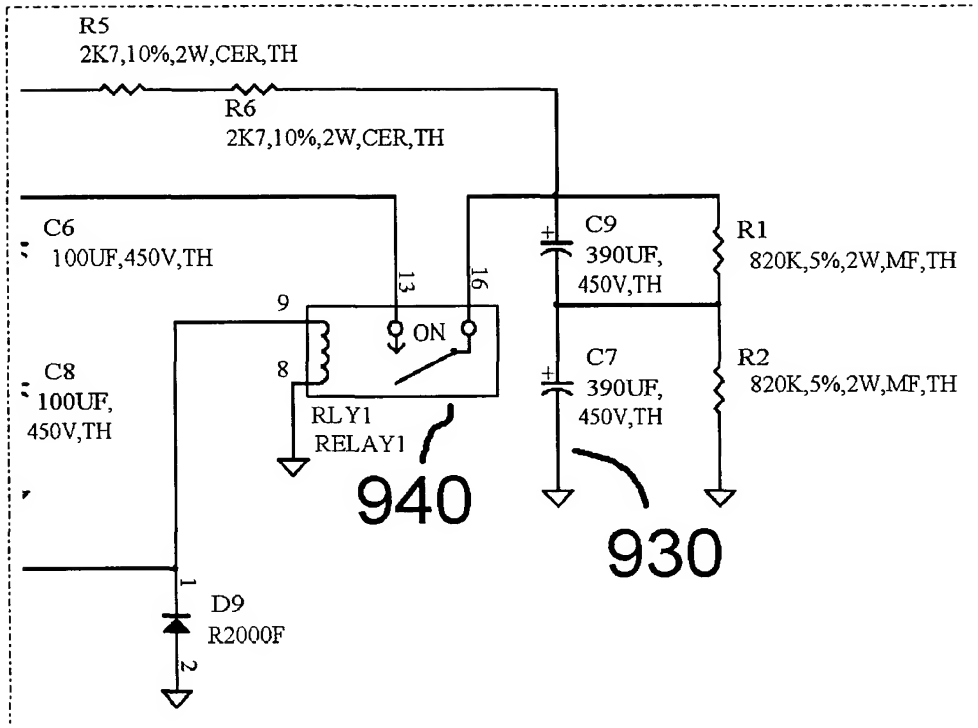
-- TO FIG 9A(1) --



-- TO FIG 9A(6) --

Fig. 9A(6) (16/58)

-- TO FIG 9A(2) --



-- TO FIG 9A(5) --

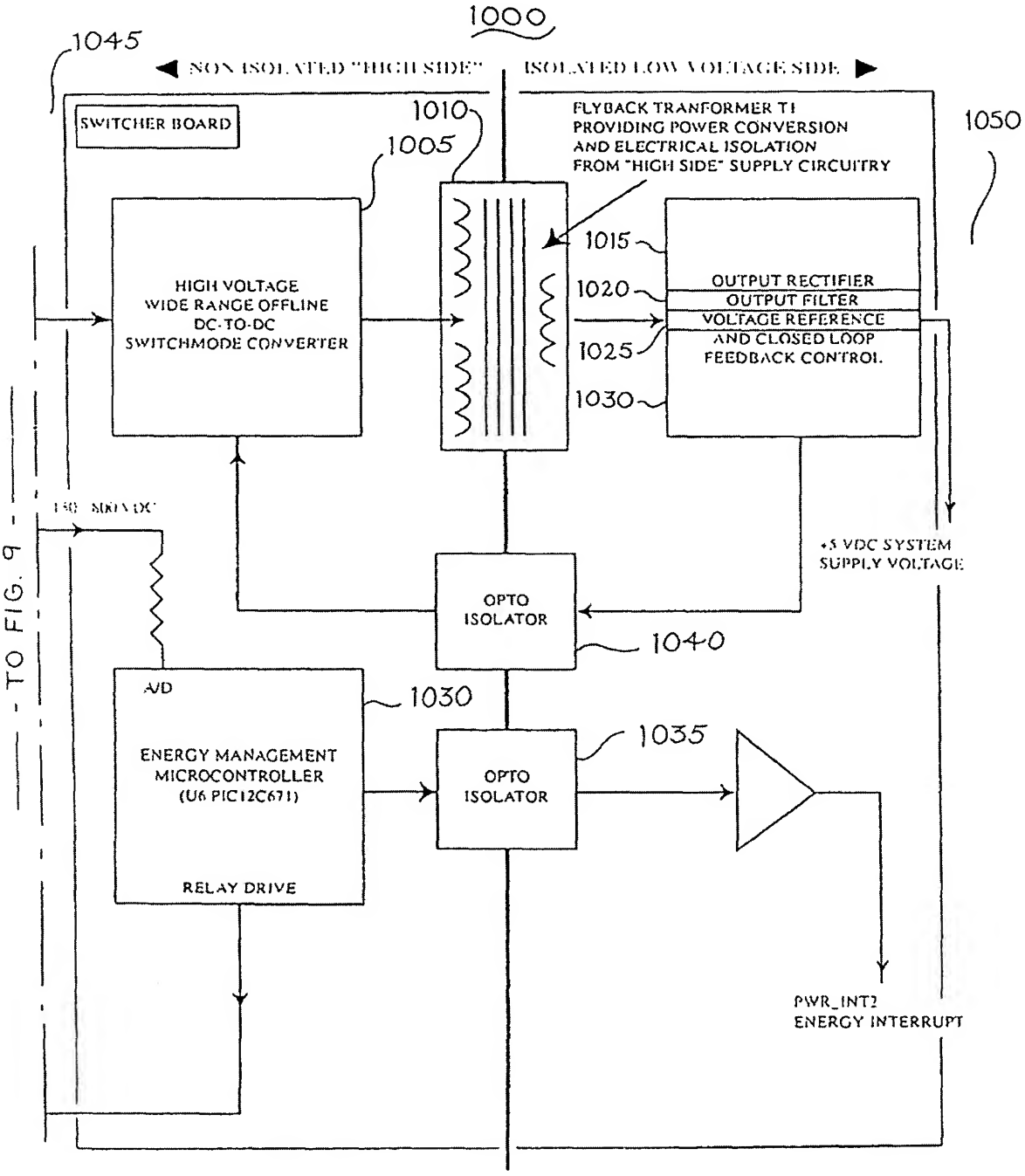

1000
1045
NON ISOLATED "HIGH SIDE"
ISOLATED LOW VOLTAGE SIDE
SWITCHER BOARD
1010
1005
FLYBACK TRANFORMER T1
PROVIDING POWER CONVERSION
AND ELECTRICAL ISOLATION
FROM "HIGH SIDE" SUPPLY CIRCUITRY
1050
1015
1020
1025
1030
HIGH VOLTAGE
WIDE RANGE OFFLINE
DC-TO-DC
SWITCHMODE CONVERTER
OUTPUT RECTIFIER
OUTPUT FILTER
VOLTAGE REFERENCE
AND CLOSED LOOP
FEEDBACK CONTROL
- TO FIG. 9 -
+5 VDC SYSTEM
SUPPLY VOLTAGE
OPTO
ISOLATOR
1040
A/D
1030
ENERGY MANAGEMENT
MICROCONTROLLER
(U6 PIC12C671)
1035
OPTO
ISOLATOR
RELAY DRIVE
PWR_INT2
ENERGY INTERRUPT

Fig. 10

Fig. 10A(1) (17/58)

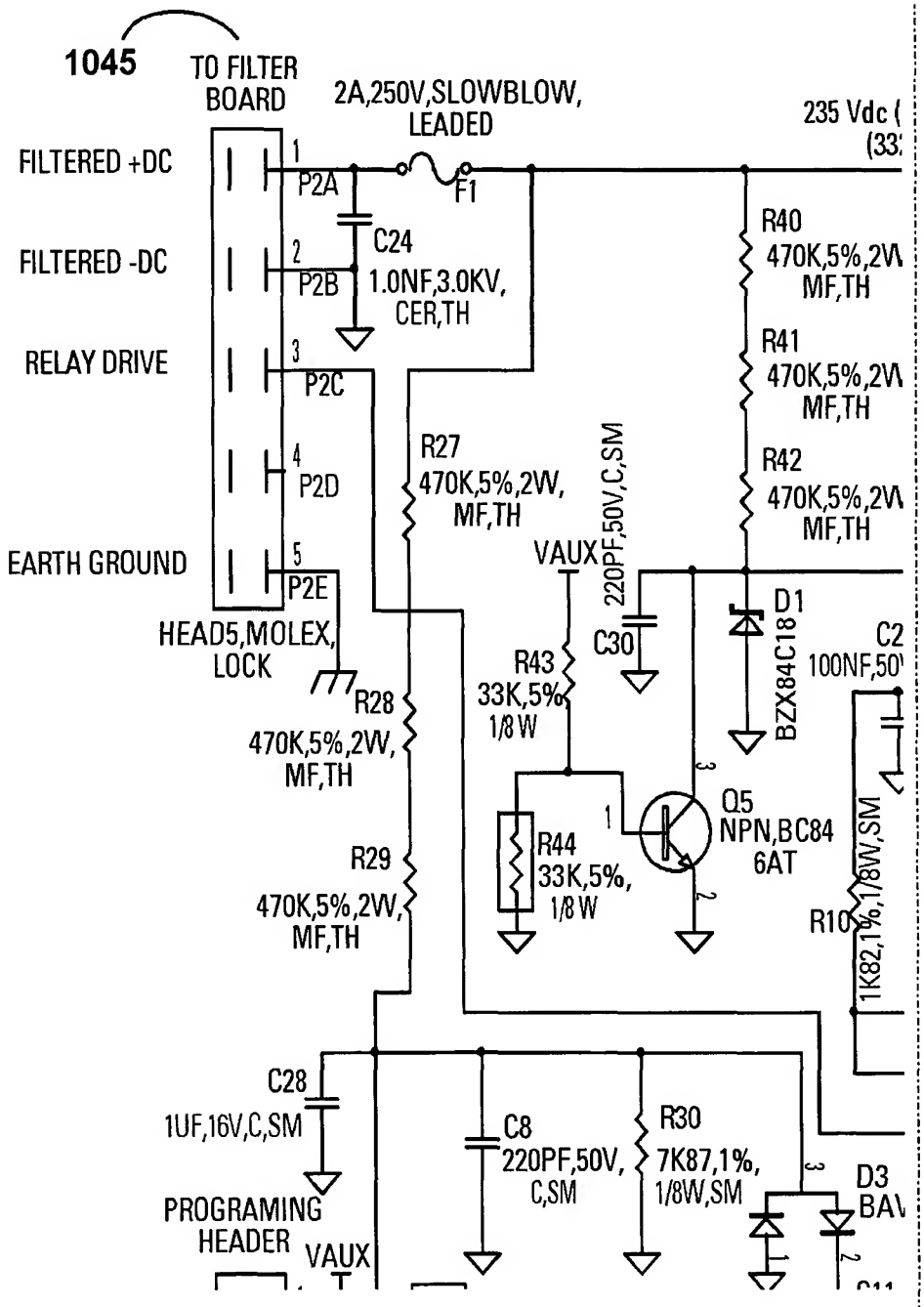
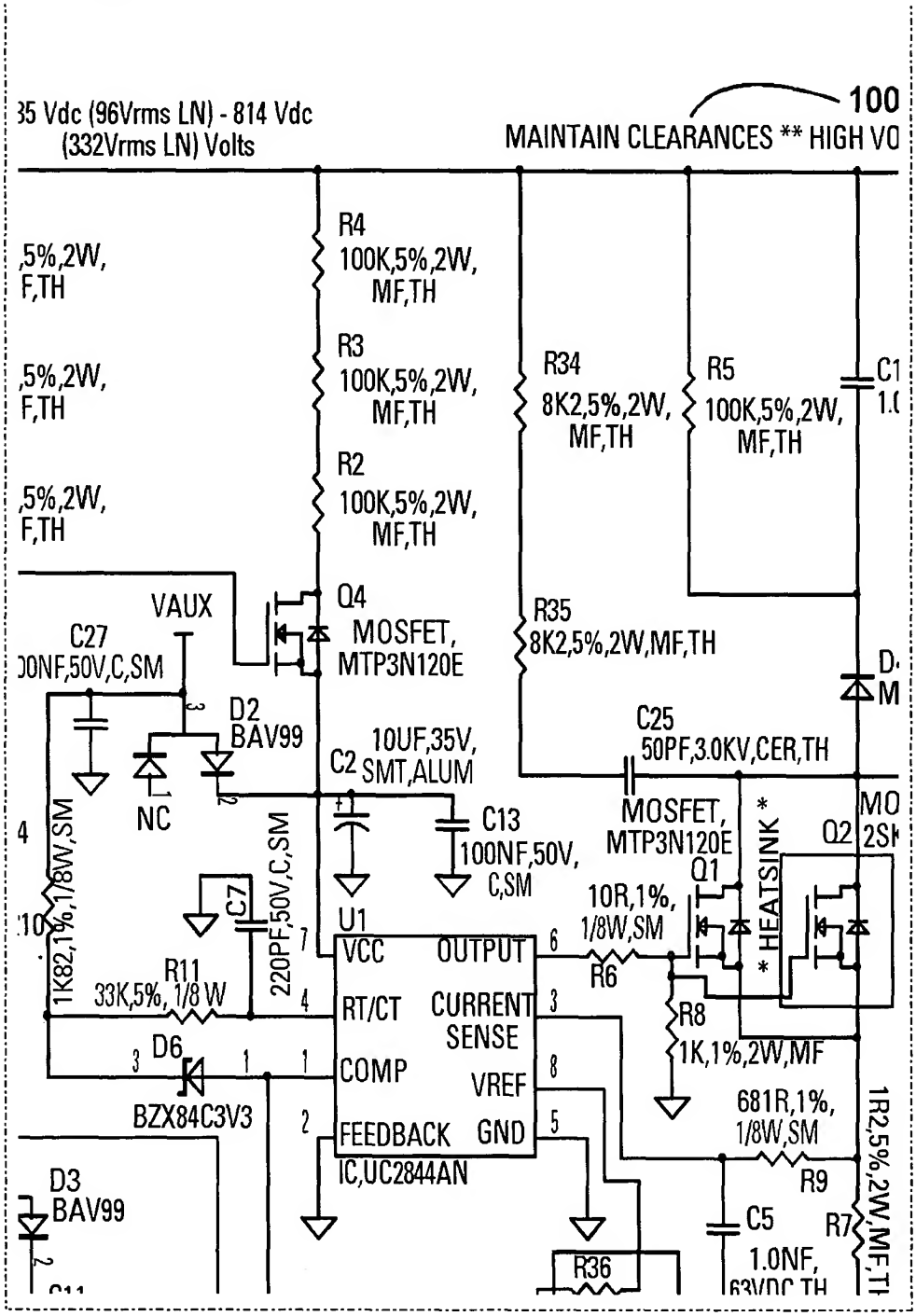


Fig. 10A(2) (18/58)



-- TO FIG 10A(6) -

Fig. 10A(3) (19/58)

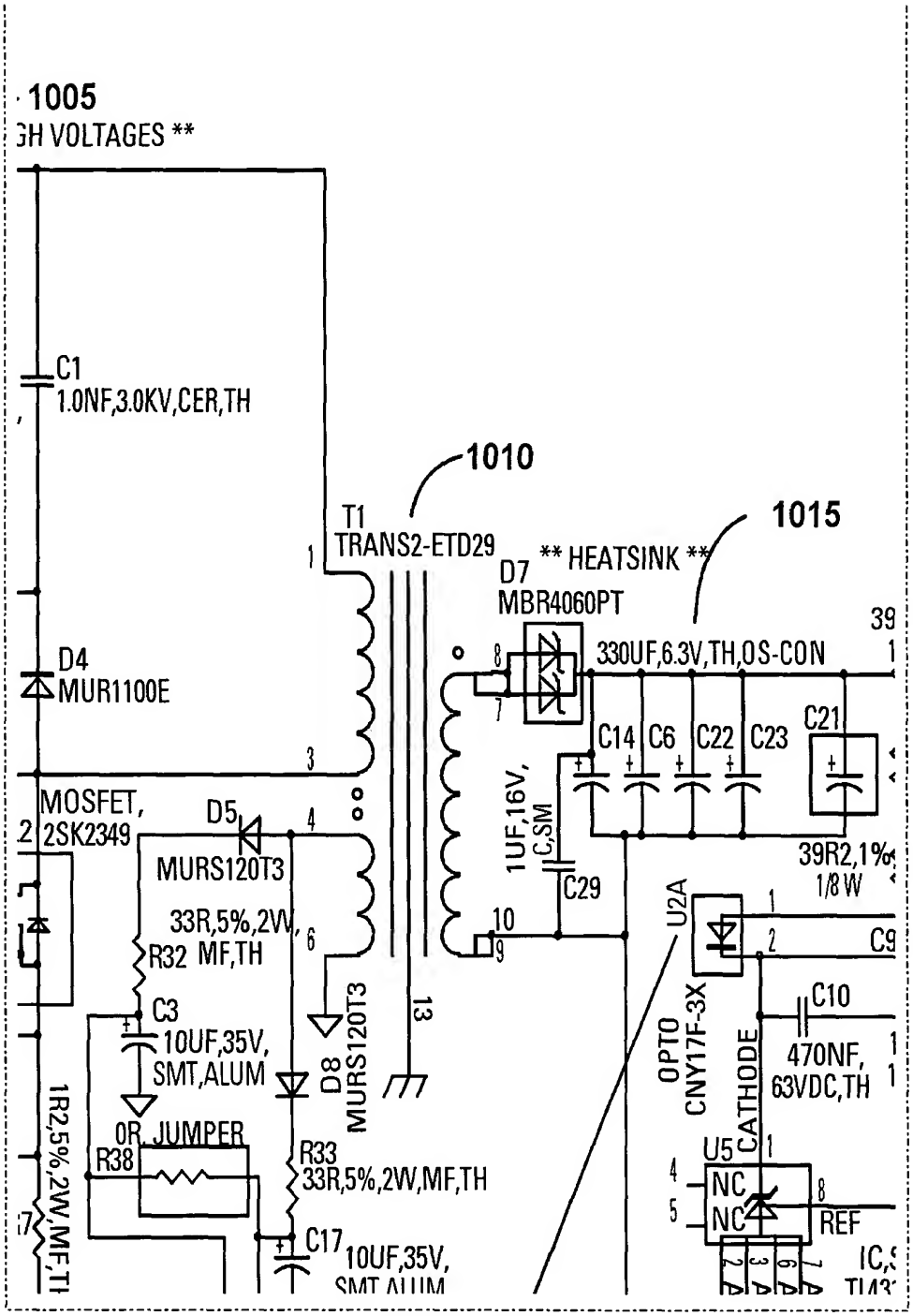
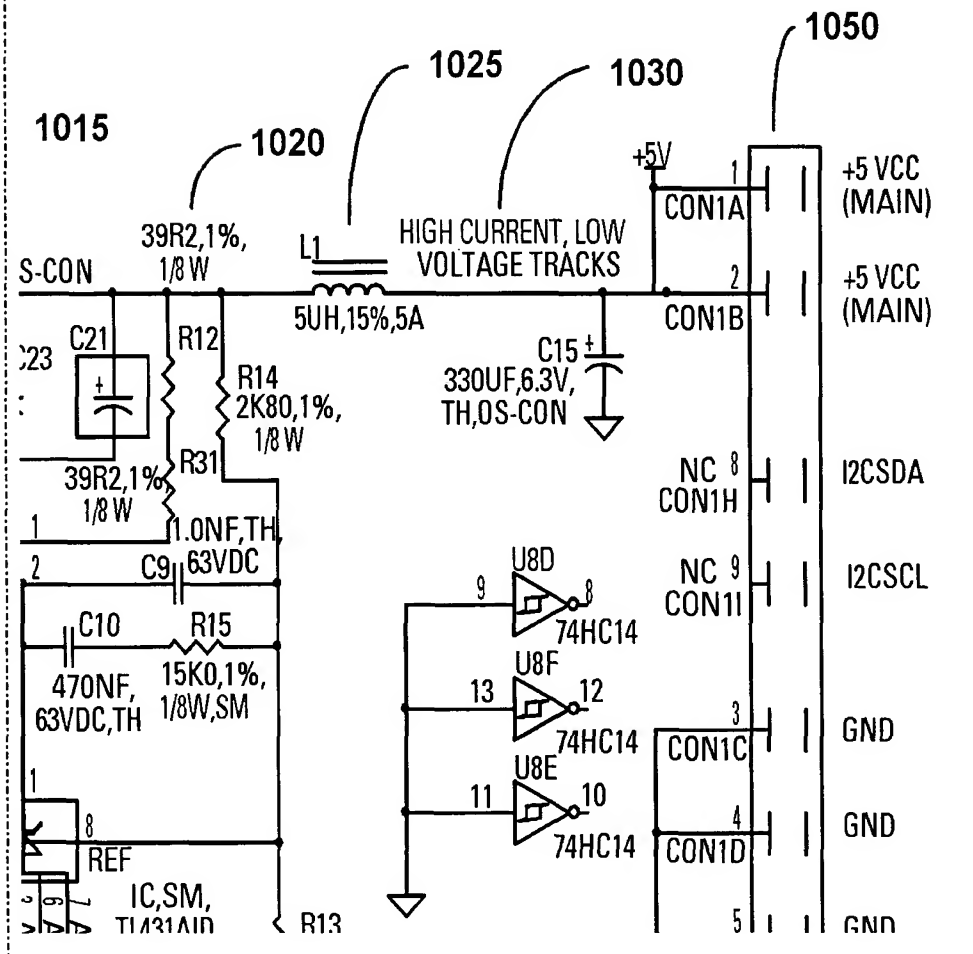


Fig. 10A(4) (20/58)

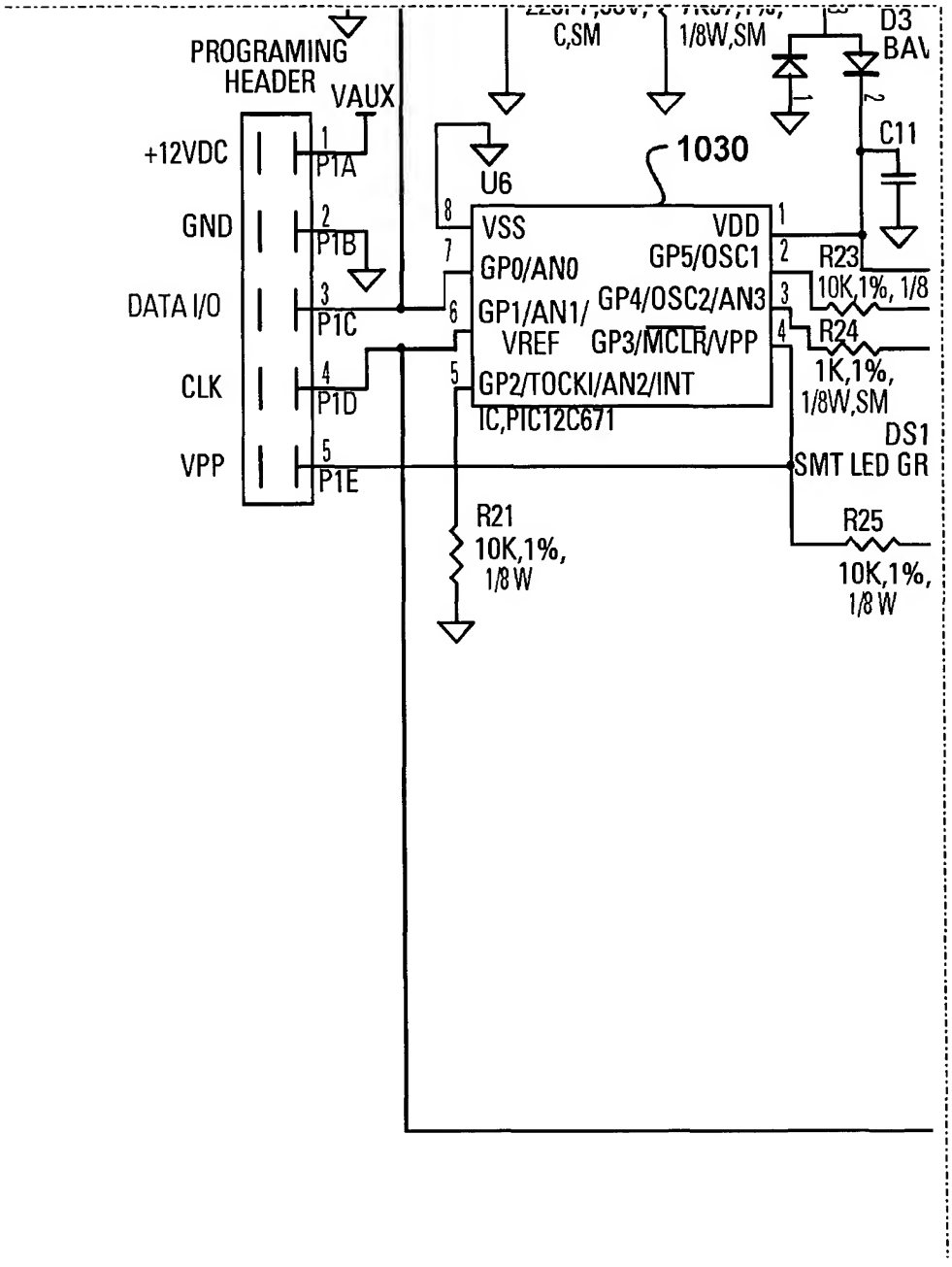


-- TO FIG 10A(3) --

-- TO FIG 10A(8) -

Fig. 10A(5) (21/58)

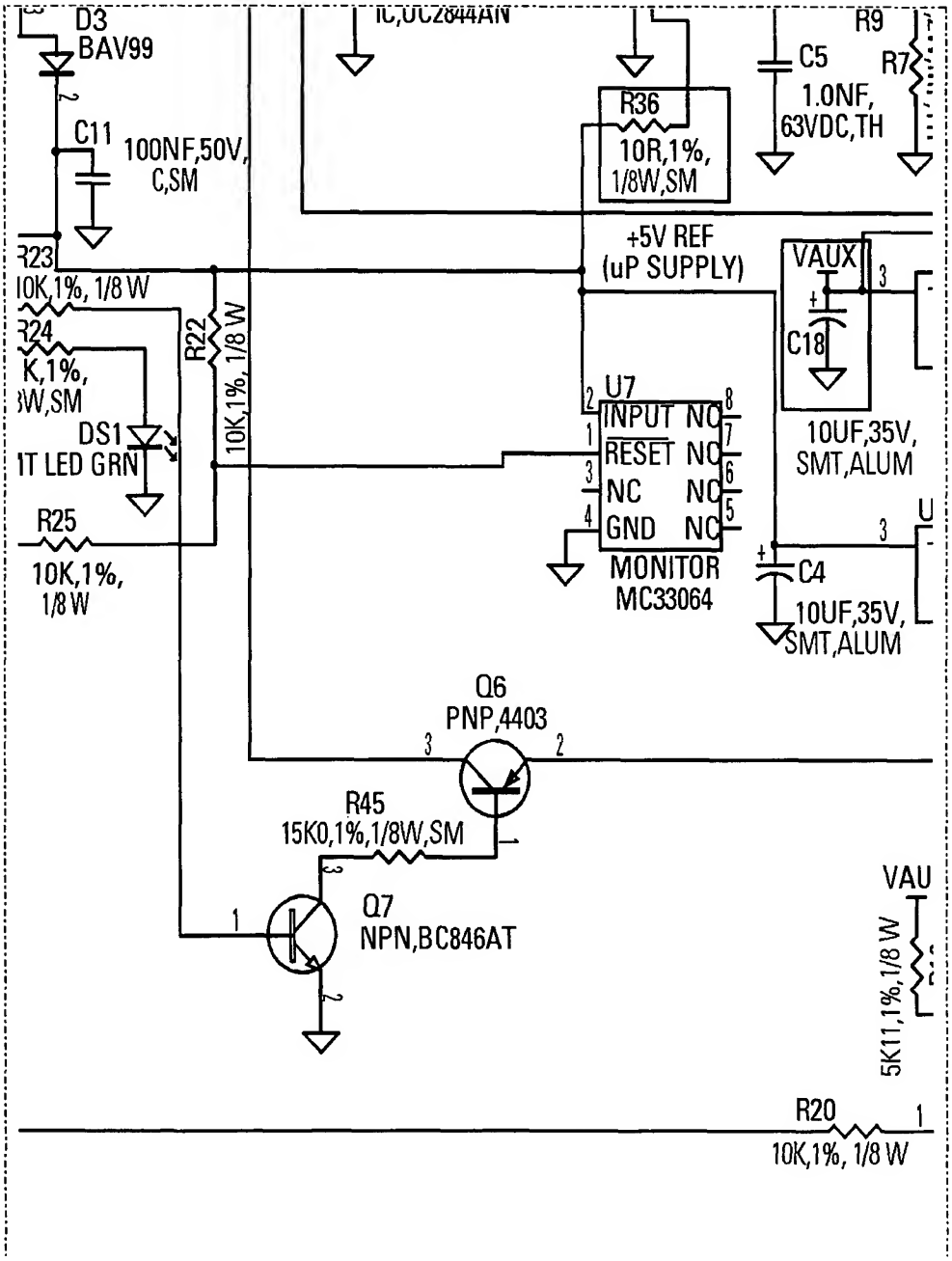
-- TO FIG 10A(1) -



-- TO FIG 10A(6) --

Fig. 10A(6) (22/58)

-- TO FIG 10A(2) -

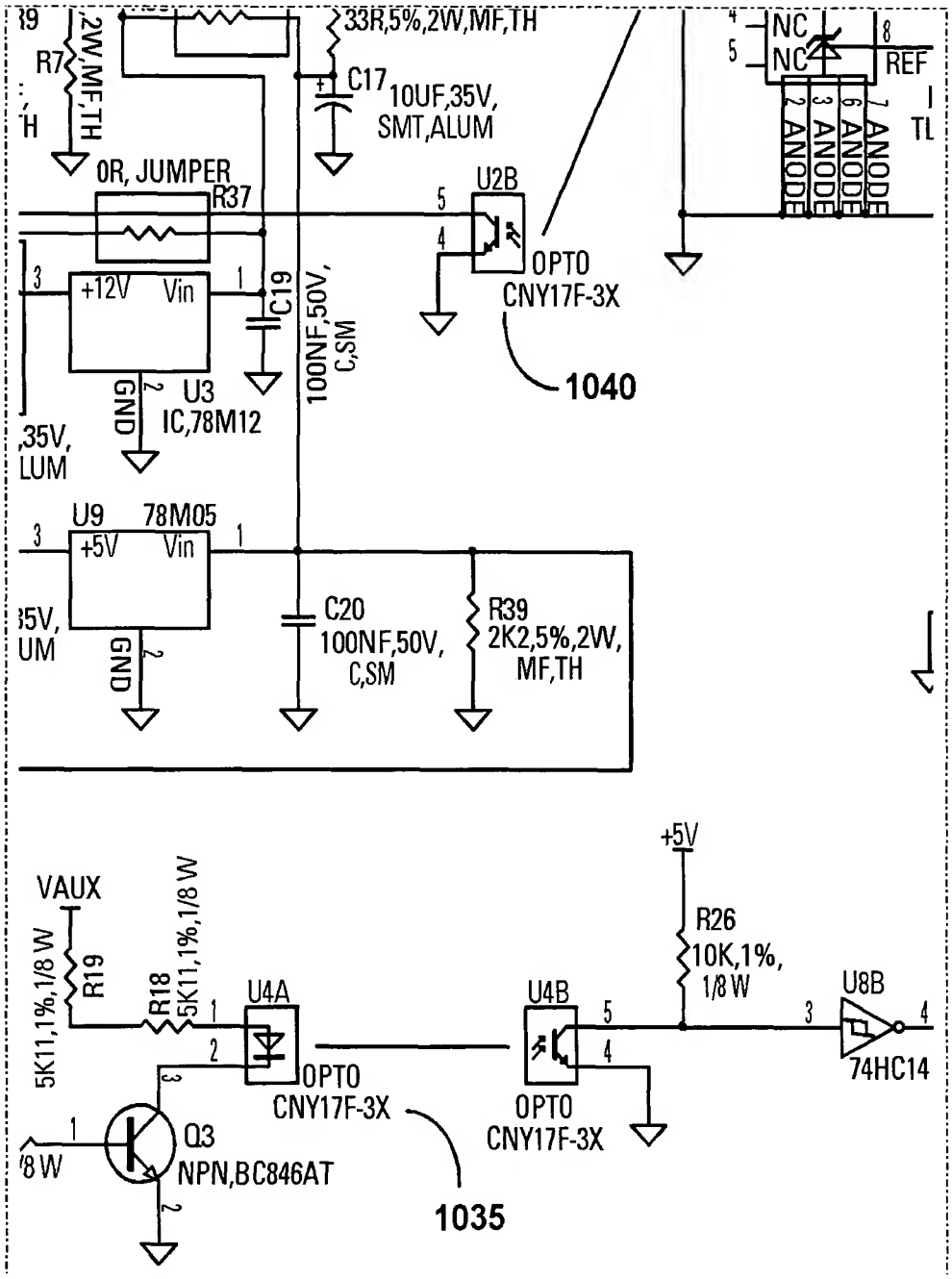


-- TO FIG 10A(5) --

-- TO FIG 10A(7) --

Fig. 10A(7) (23/58)

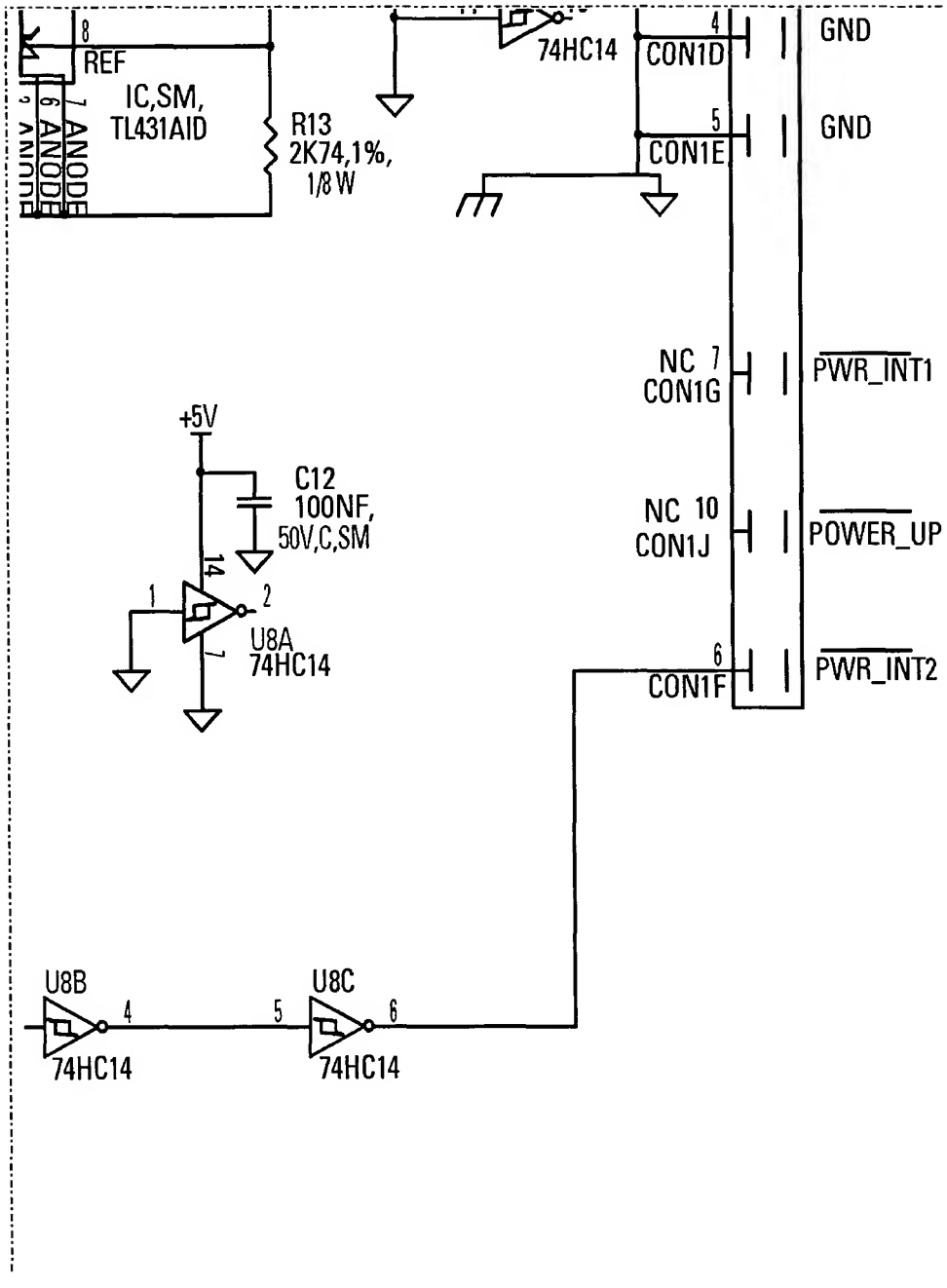
-- TO FIG 10A(3) -



-- TO FIG 10A(6) --

-- TO FIG 10A(8) --

Fig. 10A(8) (24/58)



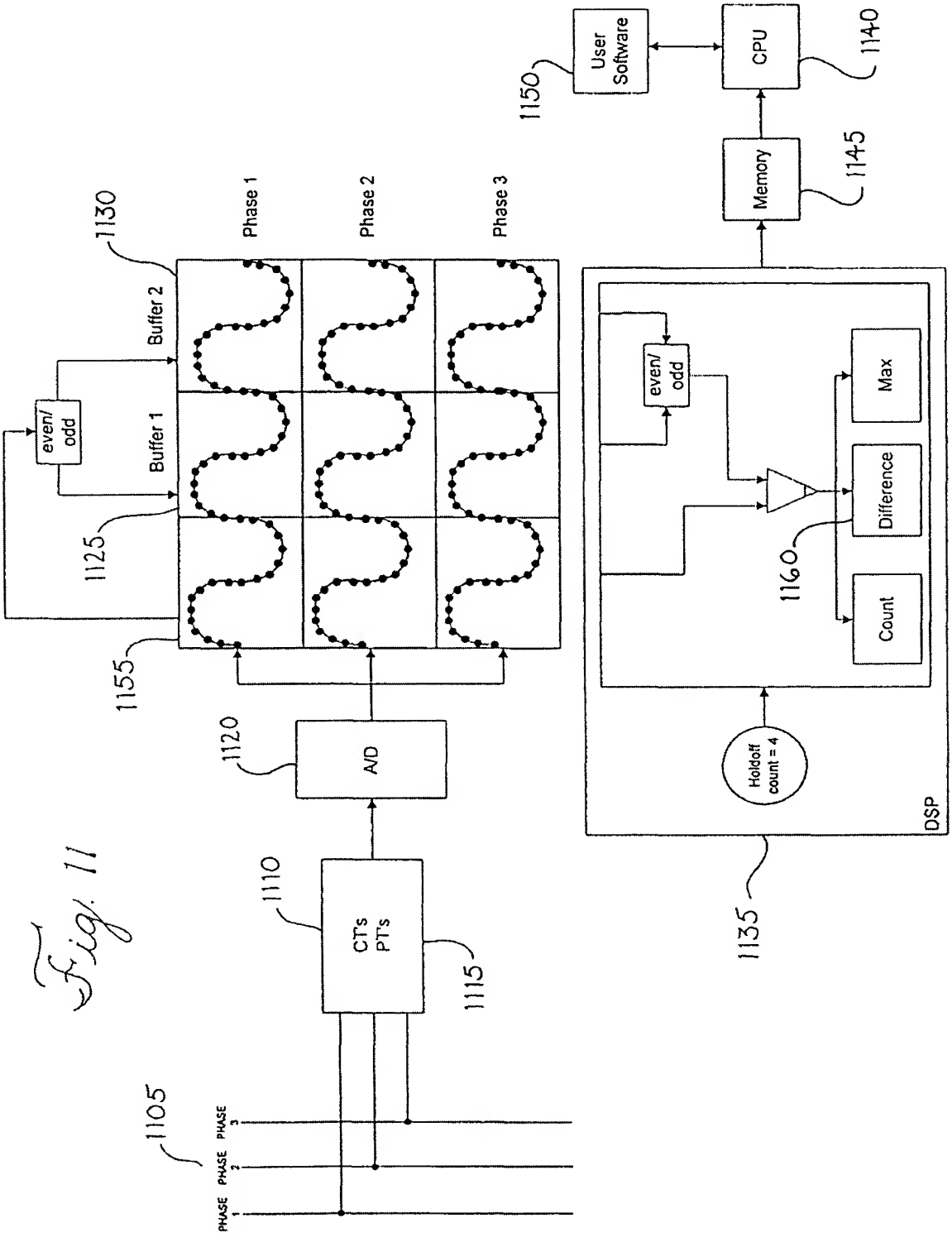

1105
PHASE 1
PHASE 2
PHASE 3
1110
CTs
PTs
1115
1120
A/D
1130
Buffer 1
Buffer 2
even/
odd
1125
1155
Phase 1
Phase 2
Phase 3
1135
DSP
Holdoff
count = 4
even/
odd
1160
Max
Difference
Count
1145
Memory
1140
CPU
1150
User
Software

Fig. 11

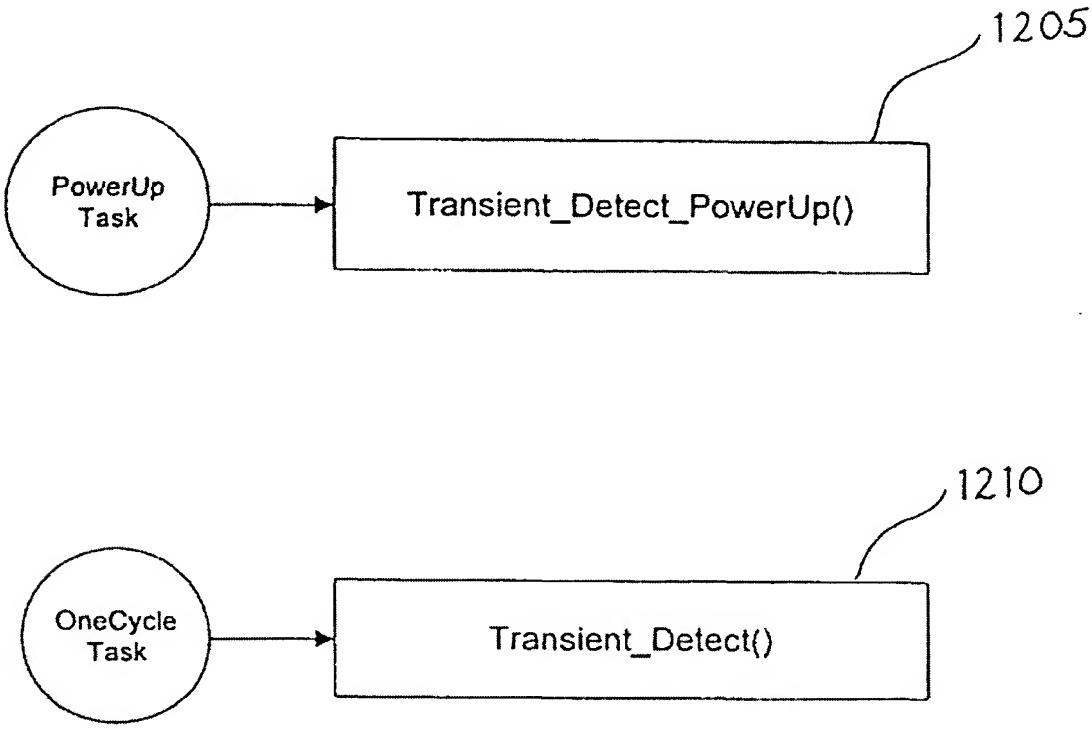

1205
PowerUp Task
Transient_Detect_PowerUp()
1210
OneCycle Task
Transient_Detect()

Fig. 12

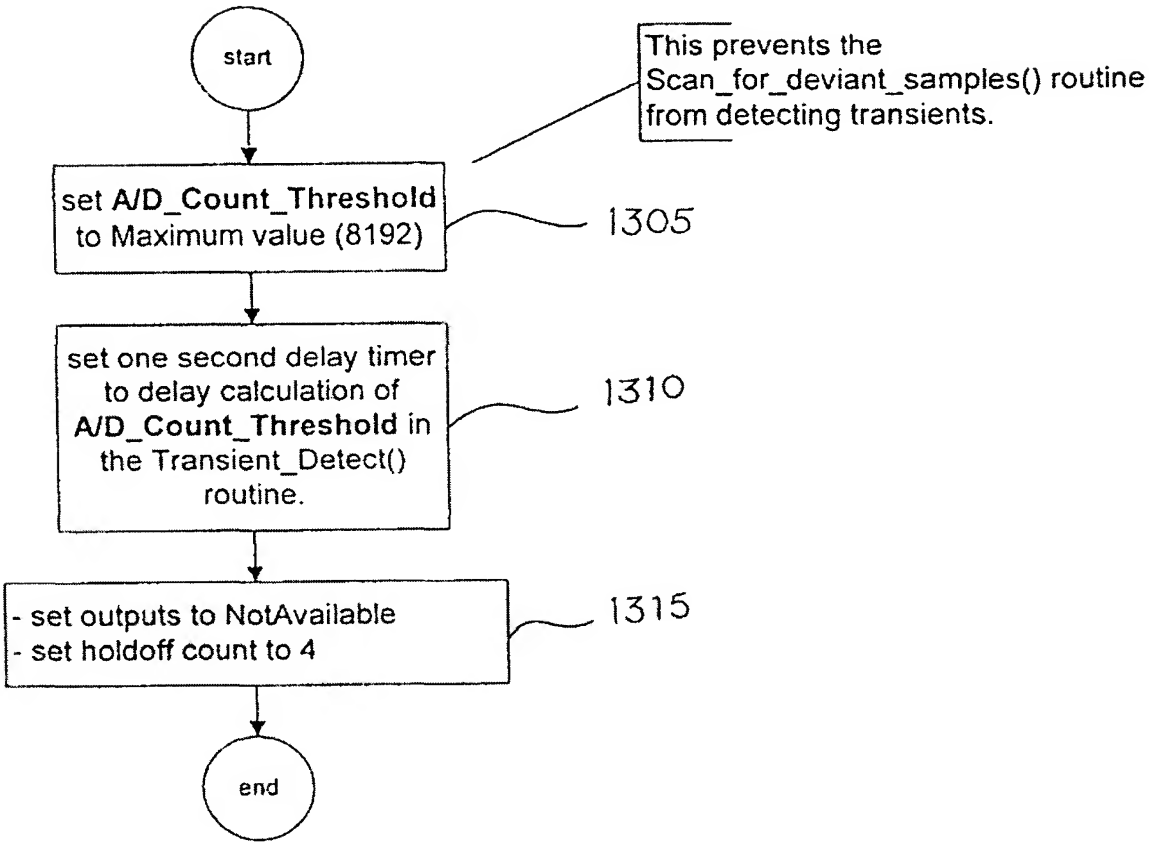

start
This prevents the Scan_for_deviant_samples() routine from detecting transients.
set A/D_Count_Threshold to Maximum value (8192)
1305
set one second delay timer to delay calculation of A/D_Count_Threshold in the Transient_Detect() routine.
1310
- set outputs to NotAvailable
- set holdoff count to 4
1315
end

Fig. 13

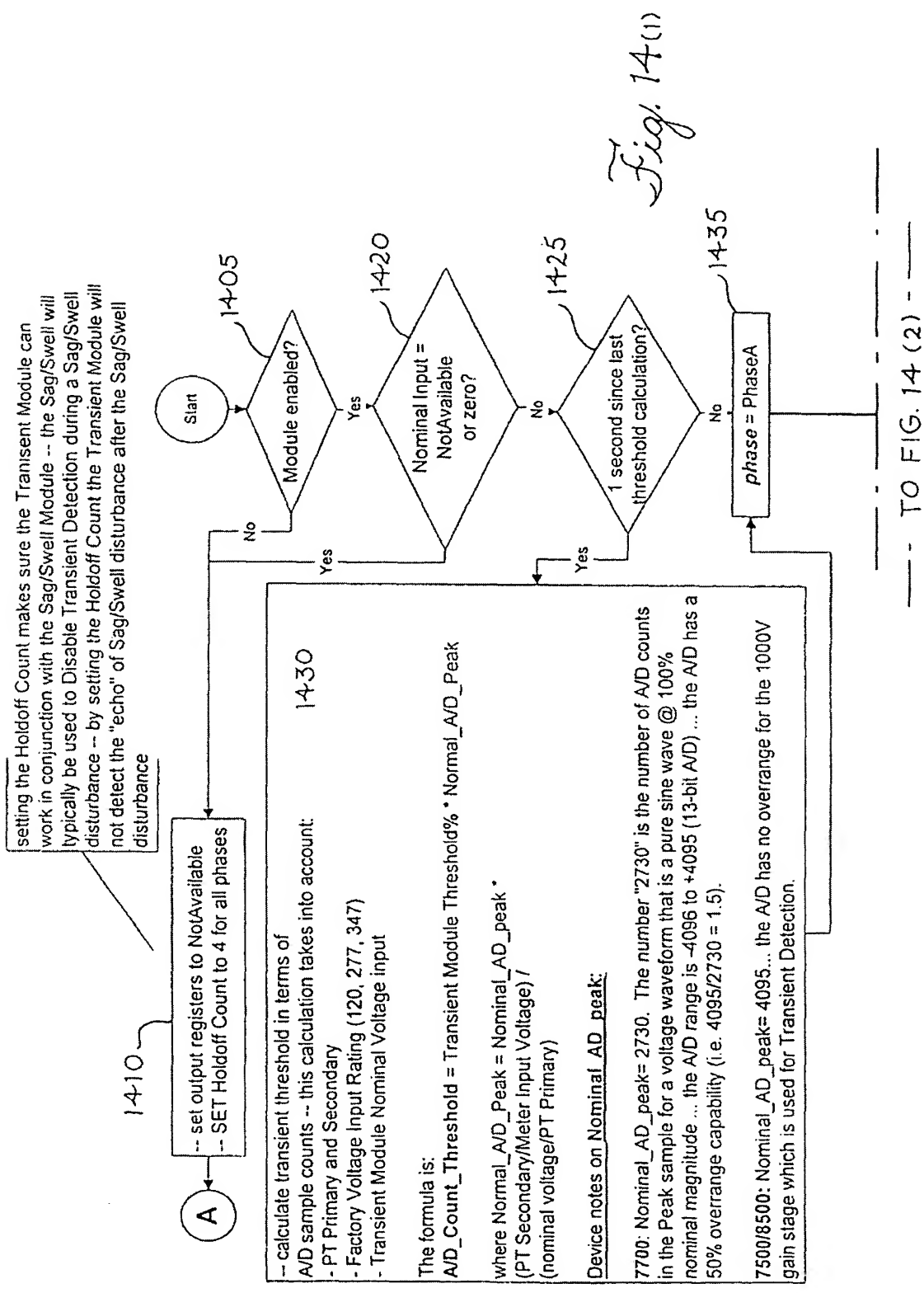

setting the Holdoff Count makes sure the Transient Module can work in conjunction with the Sag/Swell Module -- the Sag/Swell will typically be used to Disable Transient Detection during a Sag/Swell disturbance -- by setting the Holdoff Count the Transient Module will not detect the "echo" of Sag/Swell disturbance after the Sag/Swell disturbance
1410
A
-- set output registers to NotAvailable
-- SET Holdoff Count to 4 for all phases
-- calculate transient threshold in terms of A/D sample counts -- this calculation takes into account:
- PT Primary and Secondary
- Factory Voltage Input Rating (120, 277, 347)
- Transient Module Nominal Voltage input
1430
The formula is:
A/D_Count_Threshold = Transient Module Threshold% * Normal_A/D_Peak
where Normal_A/D_Peak = Nominal_AD_peak * (PT Secondary/Meter Input Voltage) / (nominal voltage/PT Primary)
Device notes on Nominal_AD_peak:
7700: Nominal_AD_peak= 2730. The number "2730" is the number of A/D counts in the Peak sample for a voltage waveform that is a pure sine wave @ 100% nominal magnitude ... the A/D range is -4096 to +4095 (13-bit A/D) ... the A/D has a 50% overrange capability (i.e. 4095/2730 = 1.5).
7500/8500: Nominal_AD_peak= 4095... the A/D has no overrange for the 1000V gain stage which is used for Transient Detection.
Start
1405
Module enabled?
No
Yes
1420
Nominal Input = NotAvailable or zero?
Yes
1425
1 second since last threshold calculation?
No
Yes
1435
phase = PhaseA
No
TO FIG. 14 (2)

Fig. 14(1)

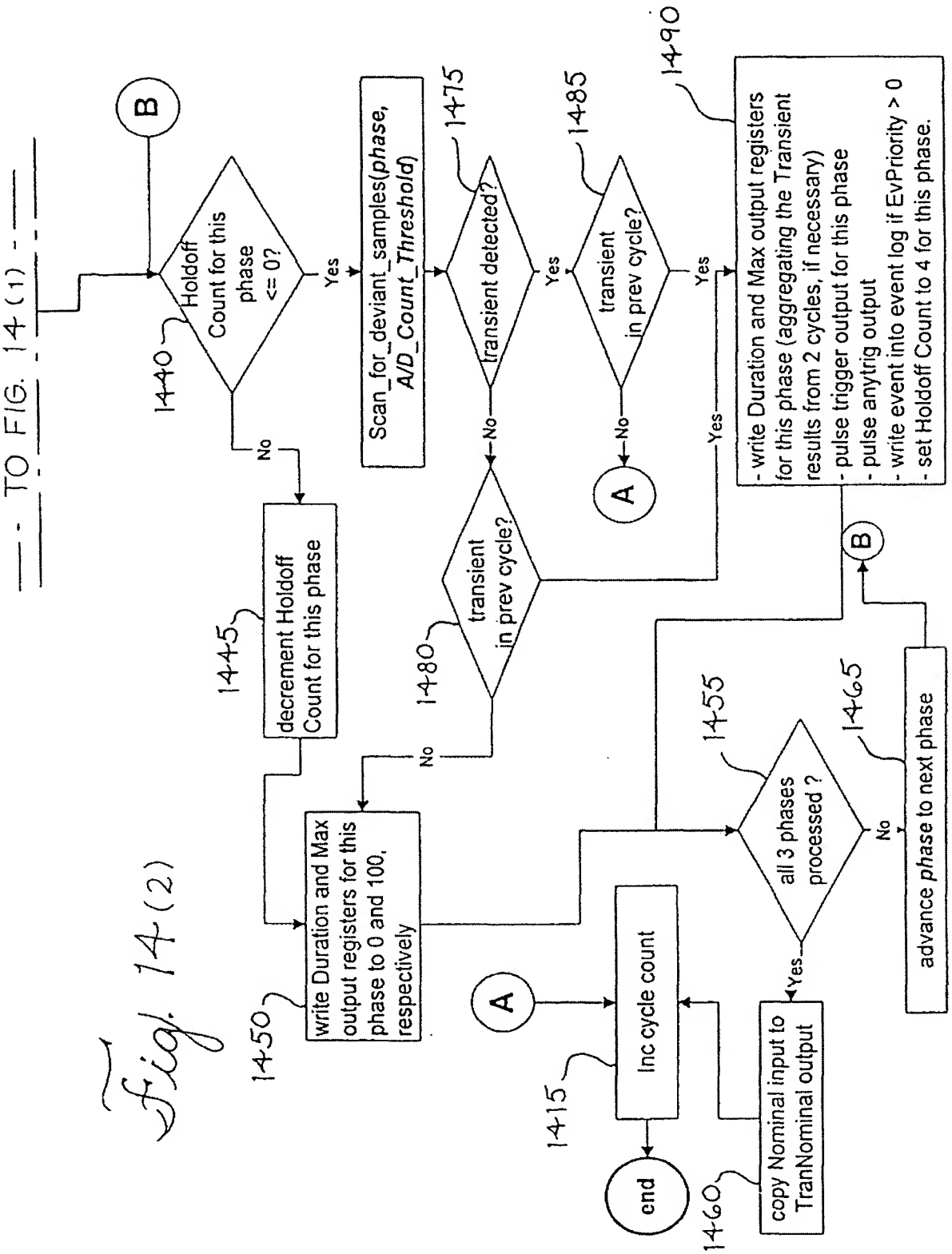
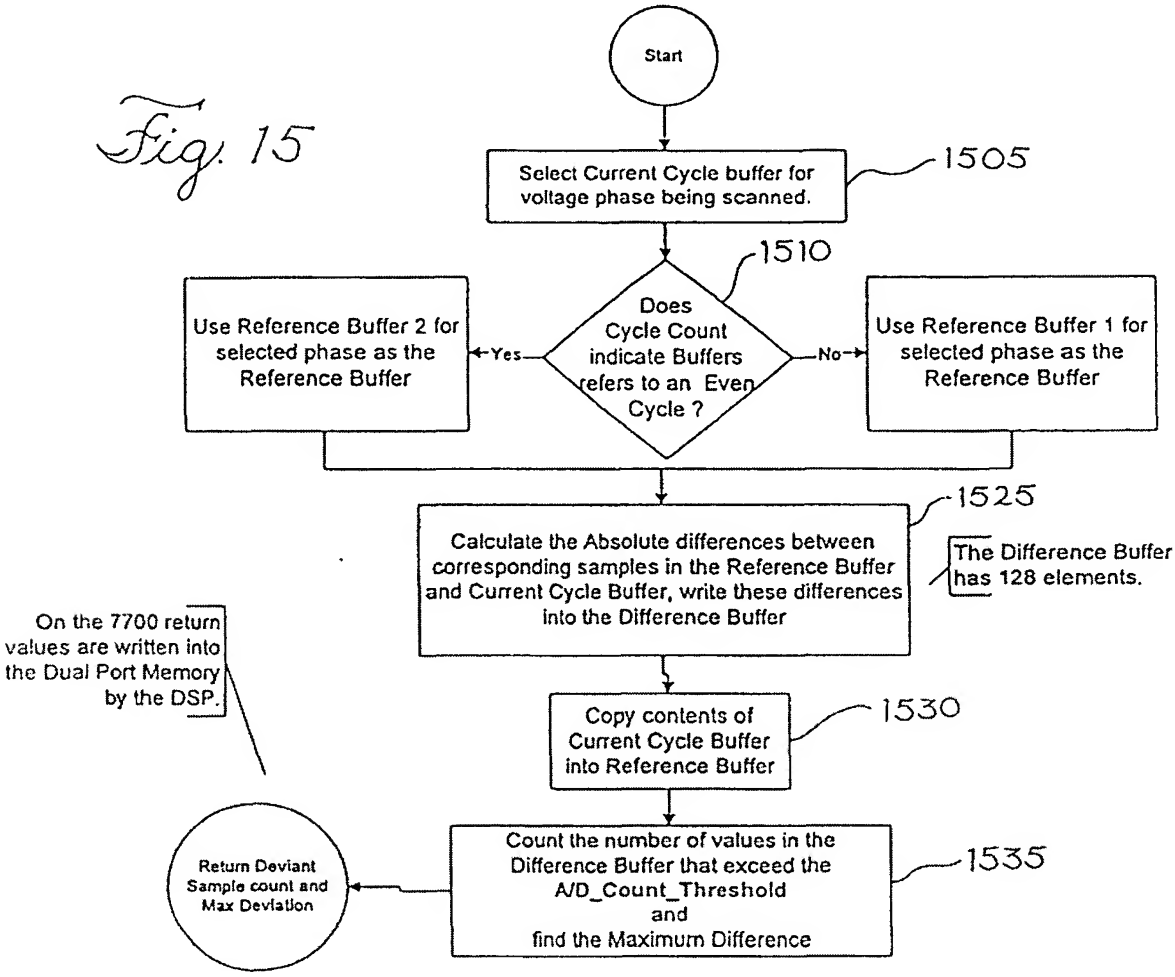
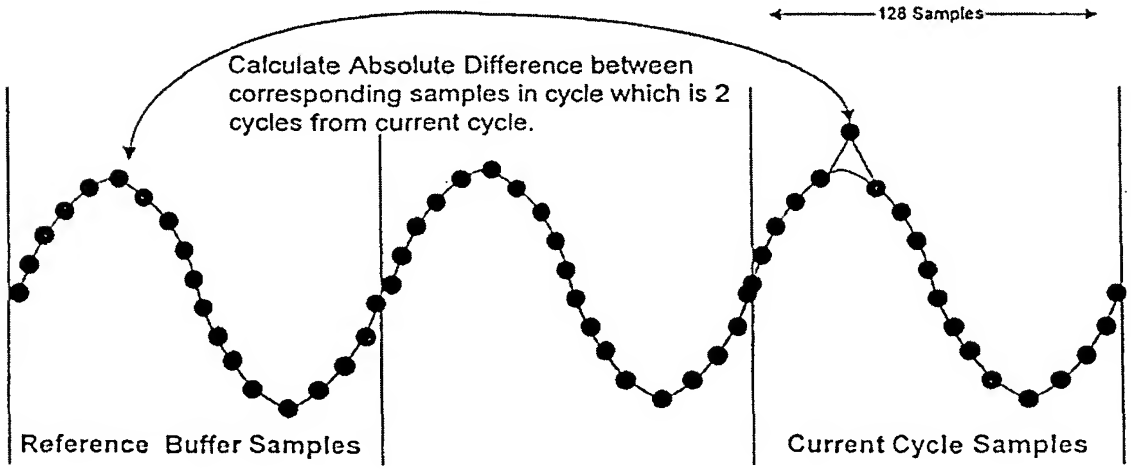

- TO FIG. 14 (1) -
B
Holdoff Count for this phase <= 0?
1440
Yes
No
Scan_for_deviant_samples(phase, A/D_Count_Threshold)
1475
Transient detected?
Yes
No
1485
transient in prev cycle?
Yes
No
A
1490
- write Duration and Max output registers for this phase (aggregating the Transient results from 2 cycles, if necessary)
- pulse trigger output for this phase
- pulse anytrig output
- write event into event log if EvPriority > 0
- set Holdoff Count to 4 for this phase.
1445
decrement Holdoff Count for this phase
1480
transient in prev cycle?
No
Yes
B
1455
all 3 phases processed ?
Yes
No
1465
advance phase to next phase
1450
write Duration and Max output registers for this phase to 0 and 100, respectively
A
1415
Inc cycle count
end
1460
copy Nominal input to TranNominal output

Fig. 14 (2)

Fig. 15


Start
Select Current Cycle buffer for voltage phase being scanned.
1505
1510
Does Cycle Count indicate Buffers refers to an Even Cycle ?
Yes
No
Use Reference Buffer 2 for selected phase as the Reference Buffer
Use Reference Buffer 1 for selected phase as the Reference Buffer
1525
Calculate the Absolute differences between corresponding samples in the Reference Buffer and Current Cycle Buffer, write these differences into the Difference Buffer
The Difference Buffer has 128 elements.
On the 7700 return values are written into the Dual Port Memory by the DSP.
Copy contents of Current Cycle Buffer into Reference Buffer
1530
Count the number of values in the Difference Buffer that exceed the A/D_Count_Threshold and find the Maximum Difference
1535
Return Deviant Sample count and Max Deviation


128 Samples
Calculate Absolute Difference between corresponding samples in cycle which is 2 cycles from current cycle.
Reference Buffer Samples
Current Cycle Samples

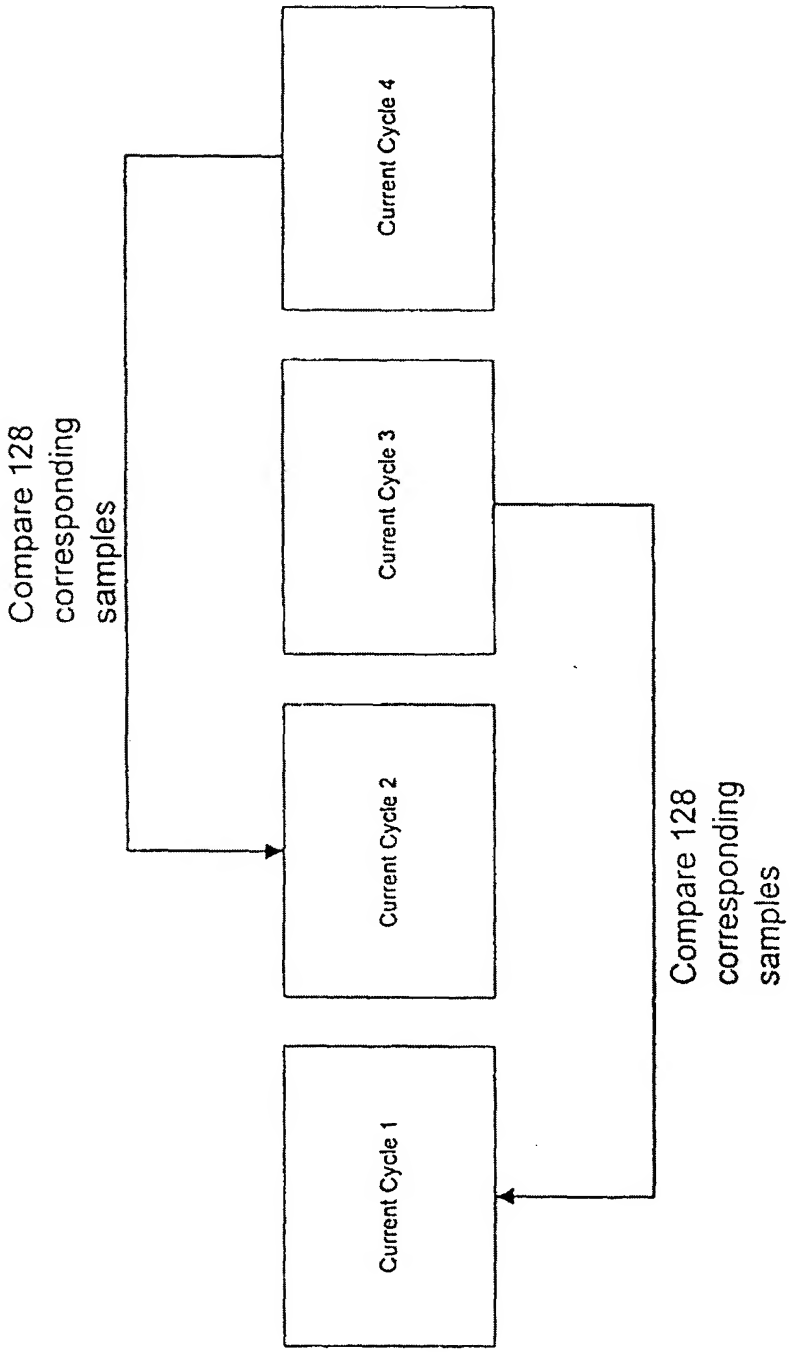

Current Cycle 4
Current Cycle 3
Current Cycle 2
Current Cycle 1
Compare 128 corresponding samples
Compare 128 corresponding samples
Difference Buffer (contains 1 cycle of differences)
Reference Buffer 2 (contains 1 cycle of samples)
Reference Buffer 1 (contains 1 cycle of samples)

Fig. 16

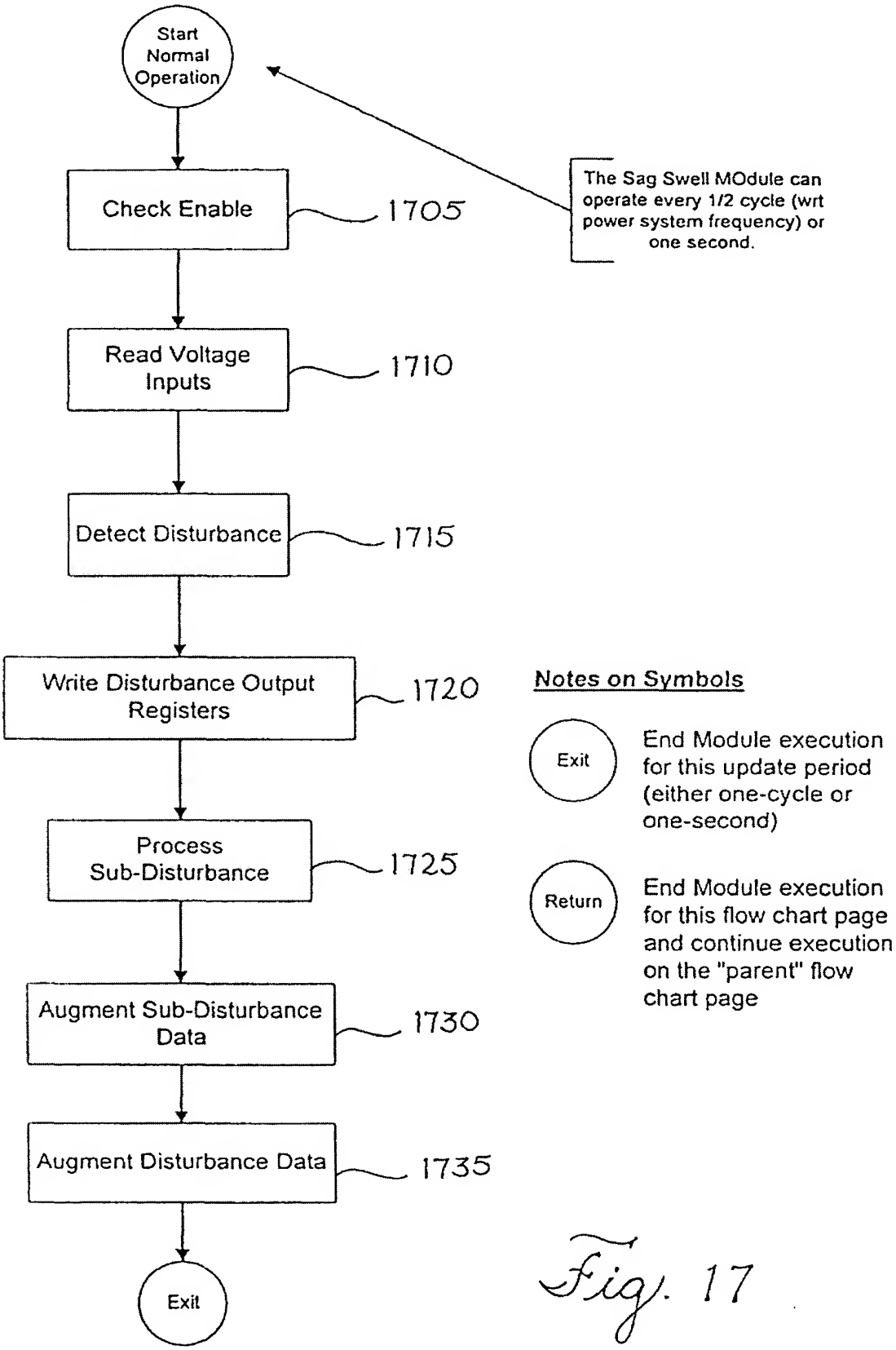

Start Normal Operation
Check Enable
1705
The Sag Swell MOdule can operate every 1/2 cycle (wrt power system frequency) or one second.
Read Voltage Inputs
1710
Detect Disturbance
1715
Write Disturbance Output Registers
1720
Process Sub-Disturbance
1725
Augment Sub-Disturbance Data
1730
Augment Disturbance Data
1735
Exit
Notes on Symbols
Exit
End Module execution for this update period (either one-cycle or one-second)
Return
End Module execution for this flow chart page and continue execution on the "parent" flow chart page

Fig. 17

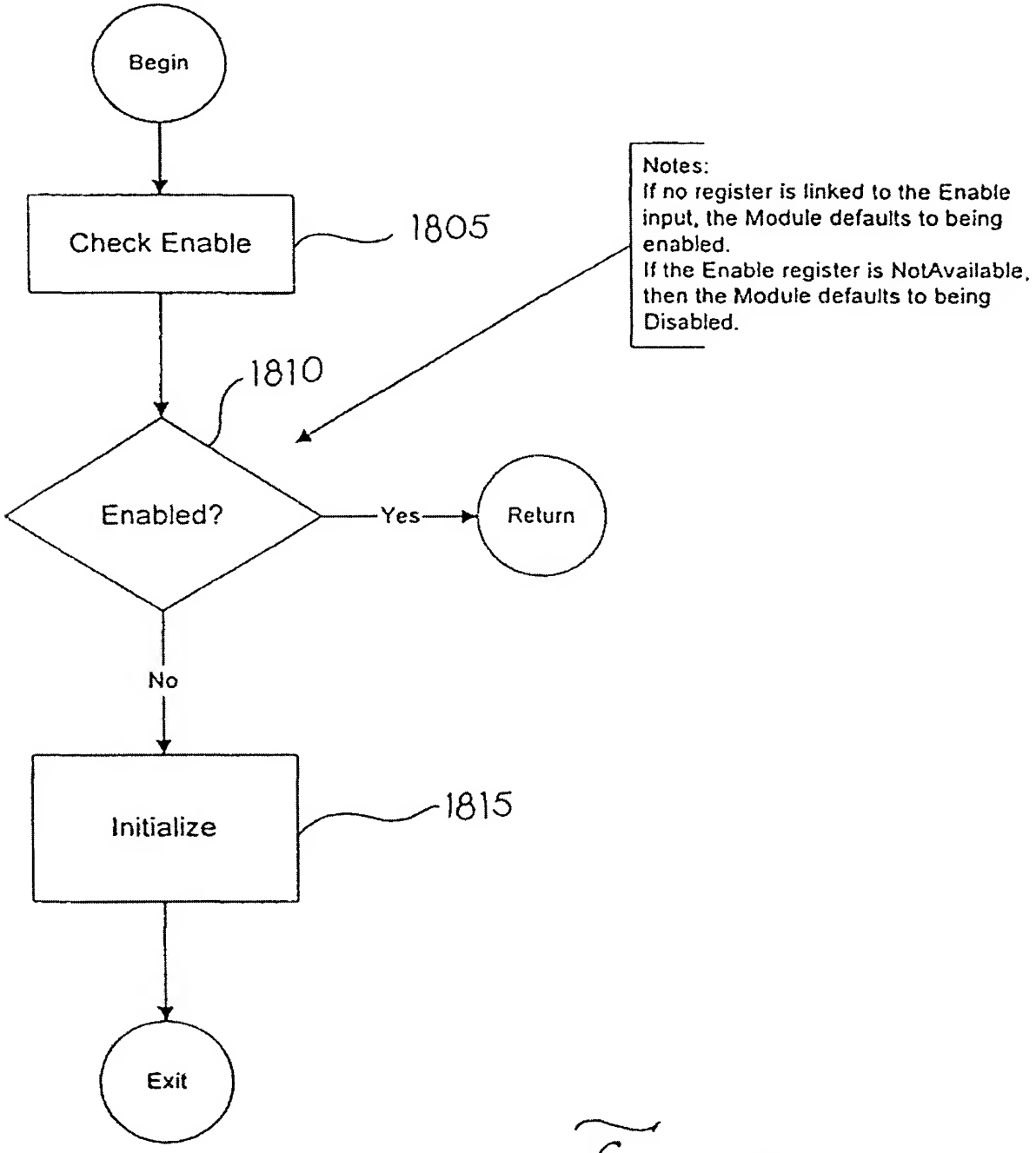

Begin
Check Enable
1805
Notes:
If no register is linked to the Enable input, the Module defaults to being enabled.
If the Enable register is NotAvailable, then the Module defaults to being Disabled.
1810
Enabled?
Yes
Return
No
Initialize
1815
Exit

Fig. 18

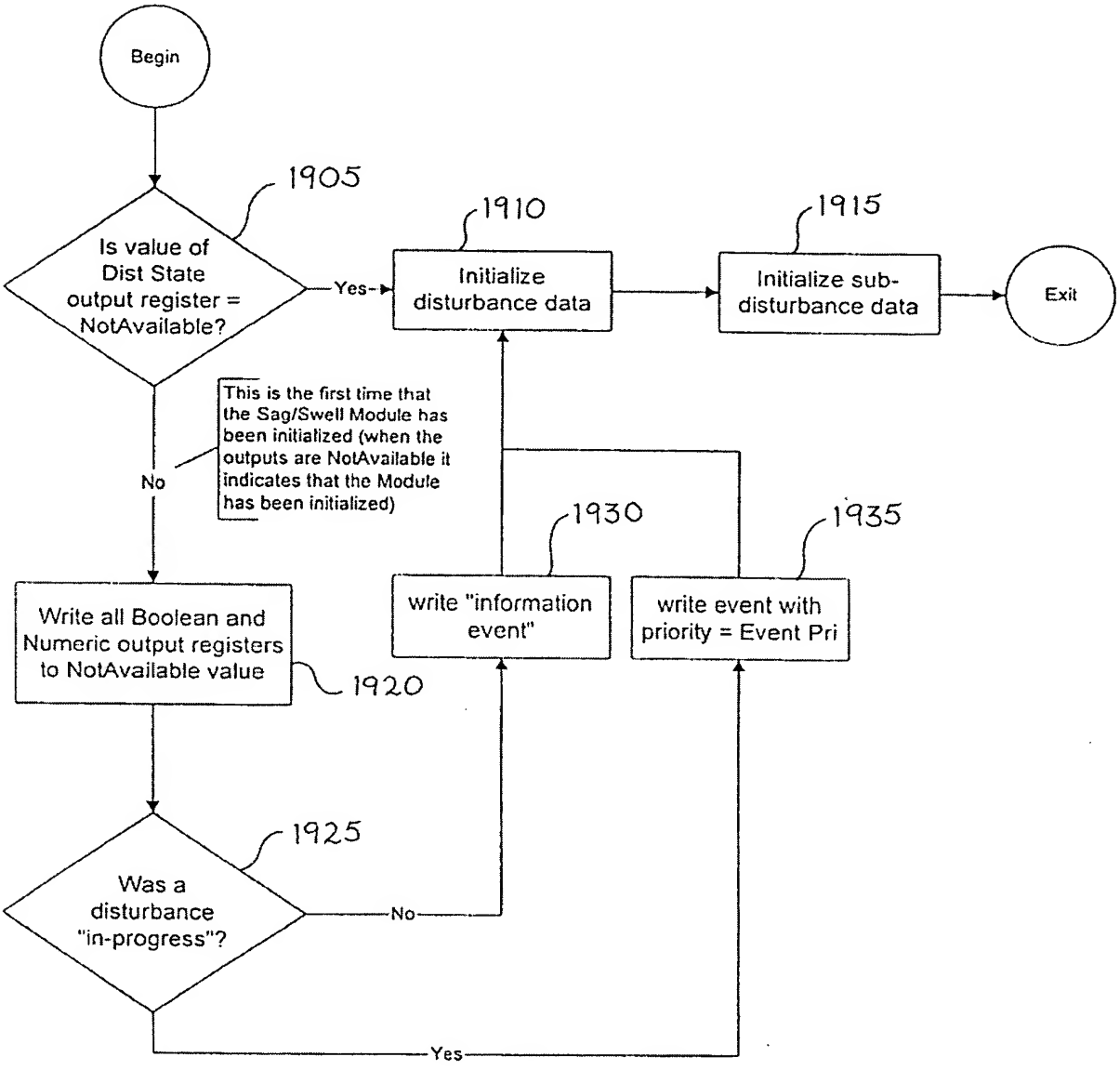

Begin
1905
Is value of Dist State output register = NotAvailable?
Yes
1910
Initialize disturbance data
1915
Initialize sub-disturbance data
Exit
No
This is the first time that the Sag/Swell Module has been initialized (when the outputs are NotAvailable it indicates that the Module has been initialized)
1930
1935
write "information event"
write event with priority = Event Pri
Write all Boolean and Numeric output registers to NotAvailable value
1920
1925
Was a disturbance "in-progress"?
No
Yes

Fig. 19

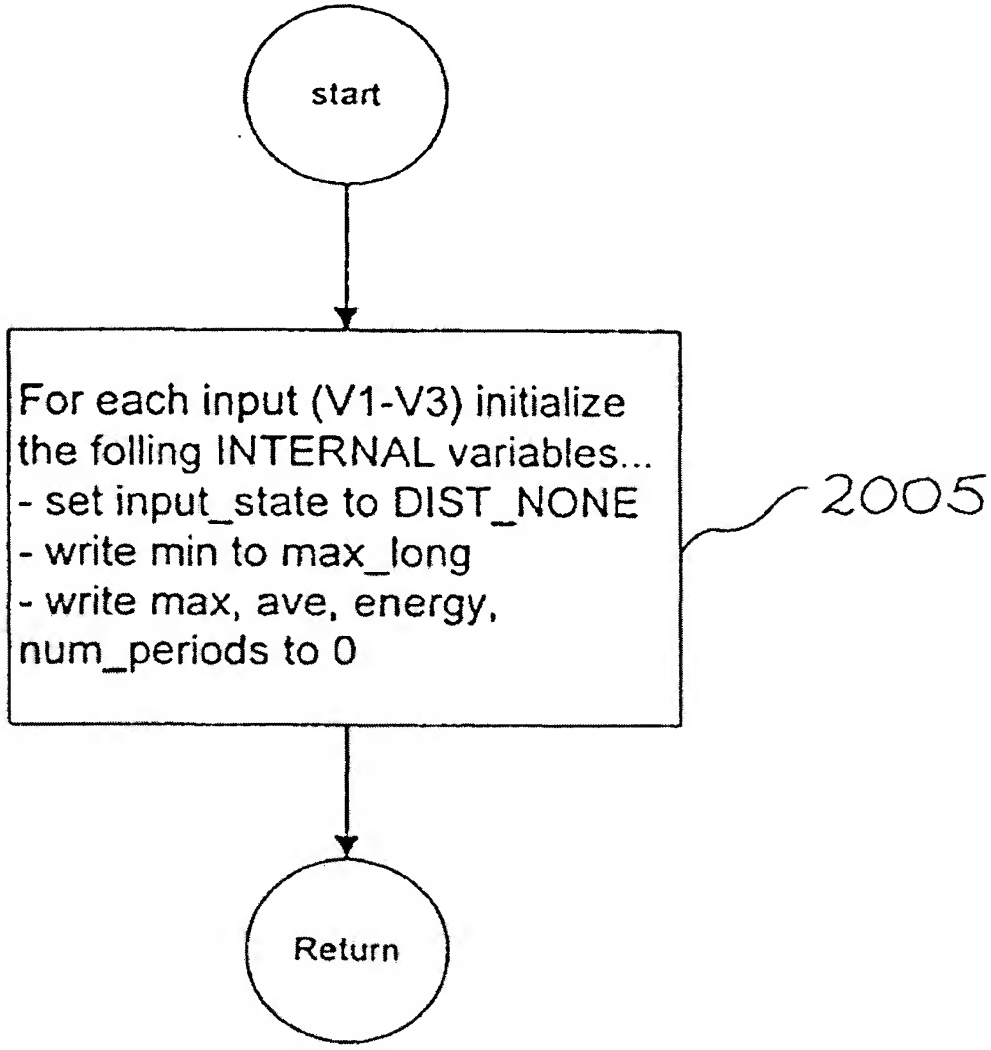

start
For each input (V1-V3) initialize the folling INTERNAL variables...
- set input_state to DIST_NONE
- write min to max_long
- write max, ave, energy, num_periods to 0
2005
Return

Fig. 20

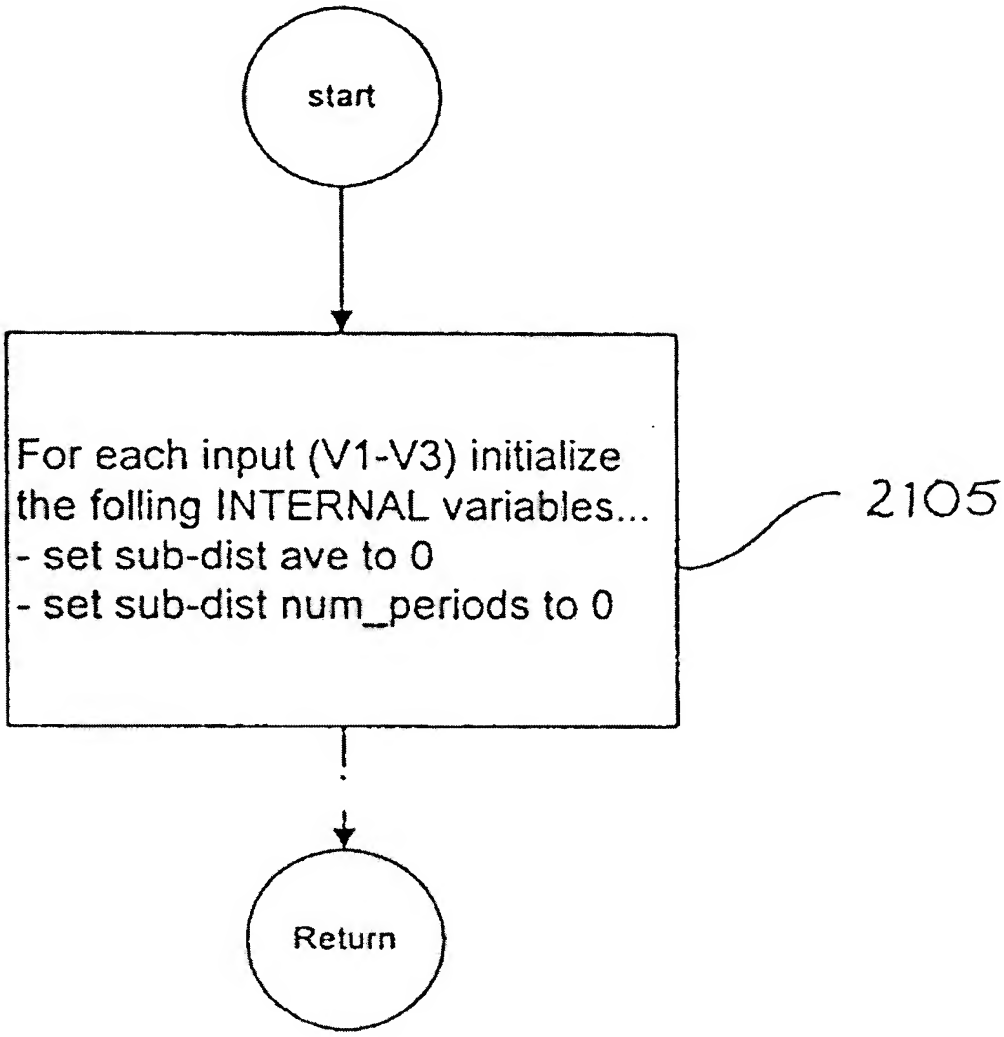

start
For each input (V1-V3) initialize
the folling INTERNAL variables...
- set sub-dist ave to 0
- set sub-dist num_periods to 0
2105
Return

Fig. 21

Fig. 22

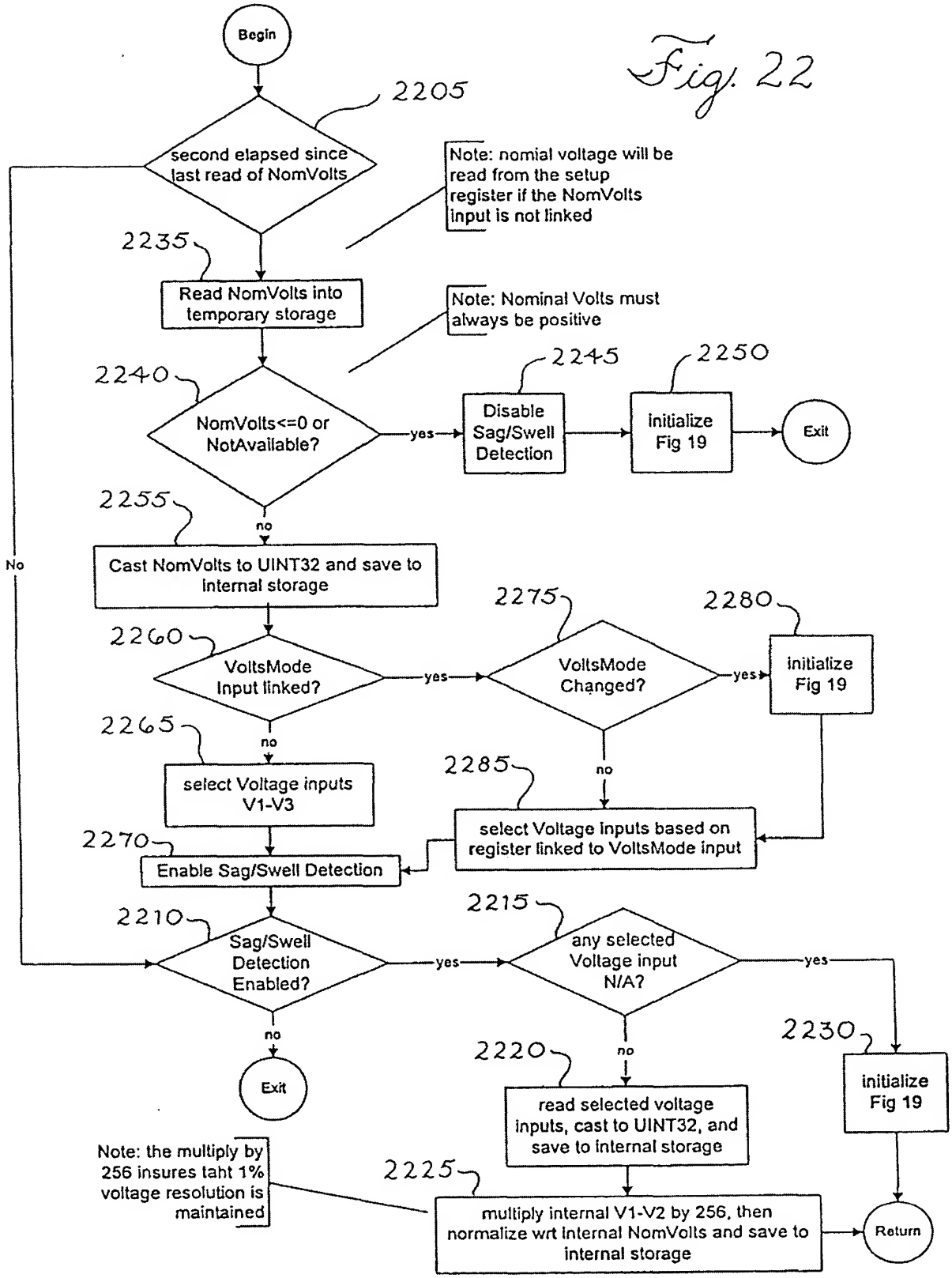

Begin
2205
second elapsed since last read of NomVolts
Note: nomial voltage will be read from the setup register if the NomVolts input is not linked
2235
Read NomVolts into temporary storage
Note: Nominal Volts must always be positive
2240
NomVolts<=0 or NotAvailable?
yes
2245
Disable Sag/Swell Detection
2250
initialize Fig 19
Exit
no
2255
Cast NomVolts to UINT32 and save to internal storage
No
2260
VoltsMode Input linked?
yes
2275
VoltsMode Changed?
yes
2280
initialize Fig 19
no
2265
select Voltage inputs V1-V3
2285
select Voltage inputs based on register linked to VoltsMode input
2270
Enable Sag/Swell Detection
2210
Sag/Swell Detection Enabled?
yes
2215
any selected Voltage input N/A?
yes
2230
initialize Fig 19
no
Exit
2220
read selected voltage inputs, cast to UINT32, and save to internal storage
Note: the multiply by 256 insures taht 1% voltage resolution is maintained
2225
multiply internal V1-V2 by 256, then normalize wrt Internal NomVolts and save to internal storage
Return

Fig. 23

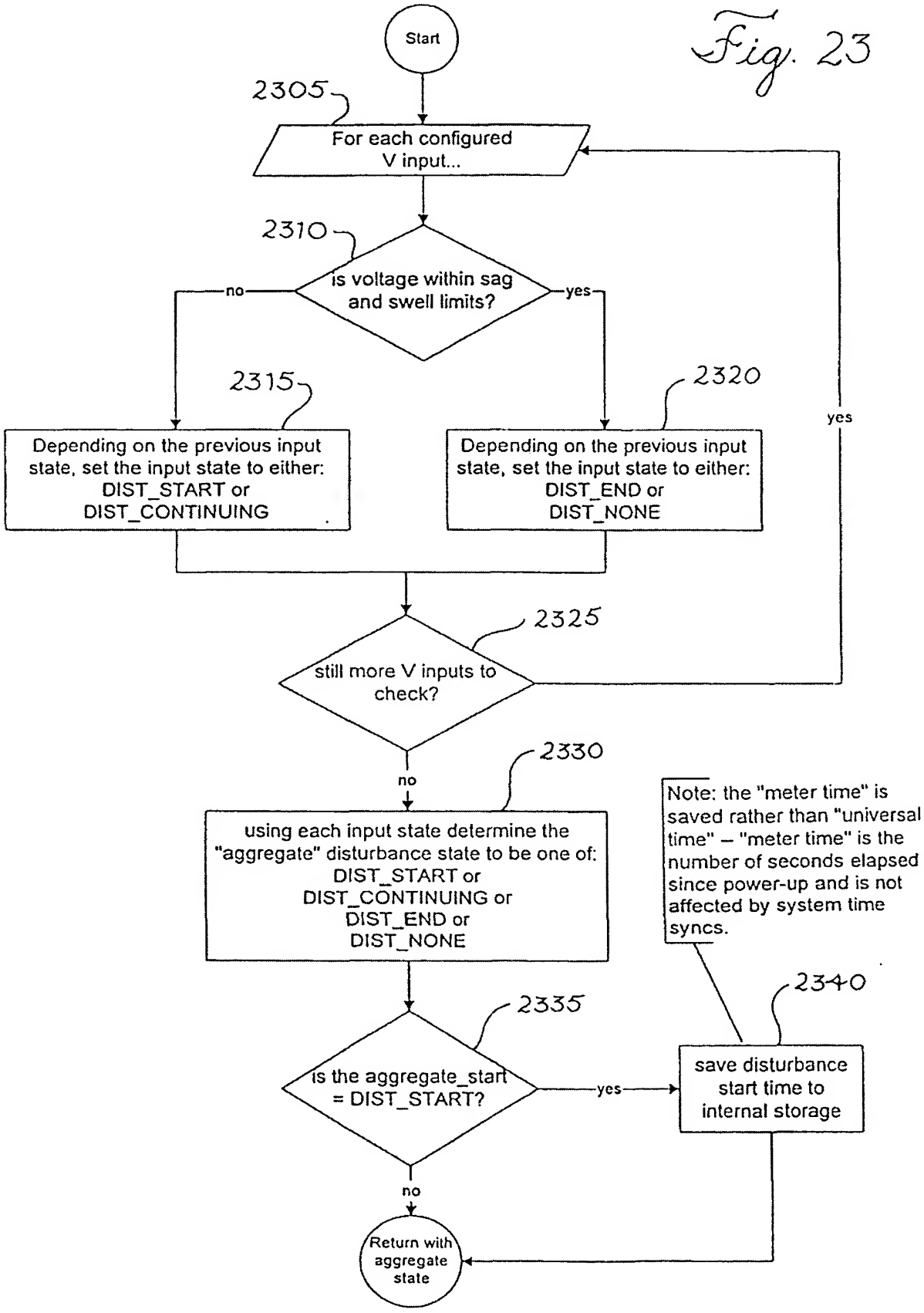

Start
2305
For each configured V input...
2310
is voltage within sag and swell limits?
no
yes
2315
Depending on the previous input state, set the input state to either: DIST_START or DIST_CONTINUING
2320
Depending on the previous input state, set the input state to either: DIST_END or DIST_NONE
yes
2325
still more V inputs to check?
no
2330
using each input state determine the "aggregate" disturbance state to be one of: DIST_START or DIST_CONTINUING or DIST_END or DIST_NONE
Note: the "meter time" is saved rather than "universal time" – "meter time" is the number of seconds elapsed since power-up and is not affected by system time syncs.
2335
is the aggregate_start = DIST_START?
yes
2340
save disturbance start time to internal storage
no
Return with aggregate state

Fig. 24

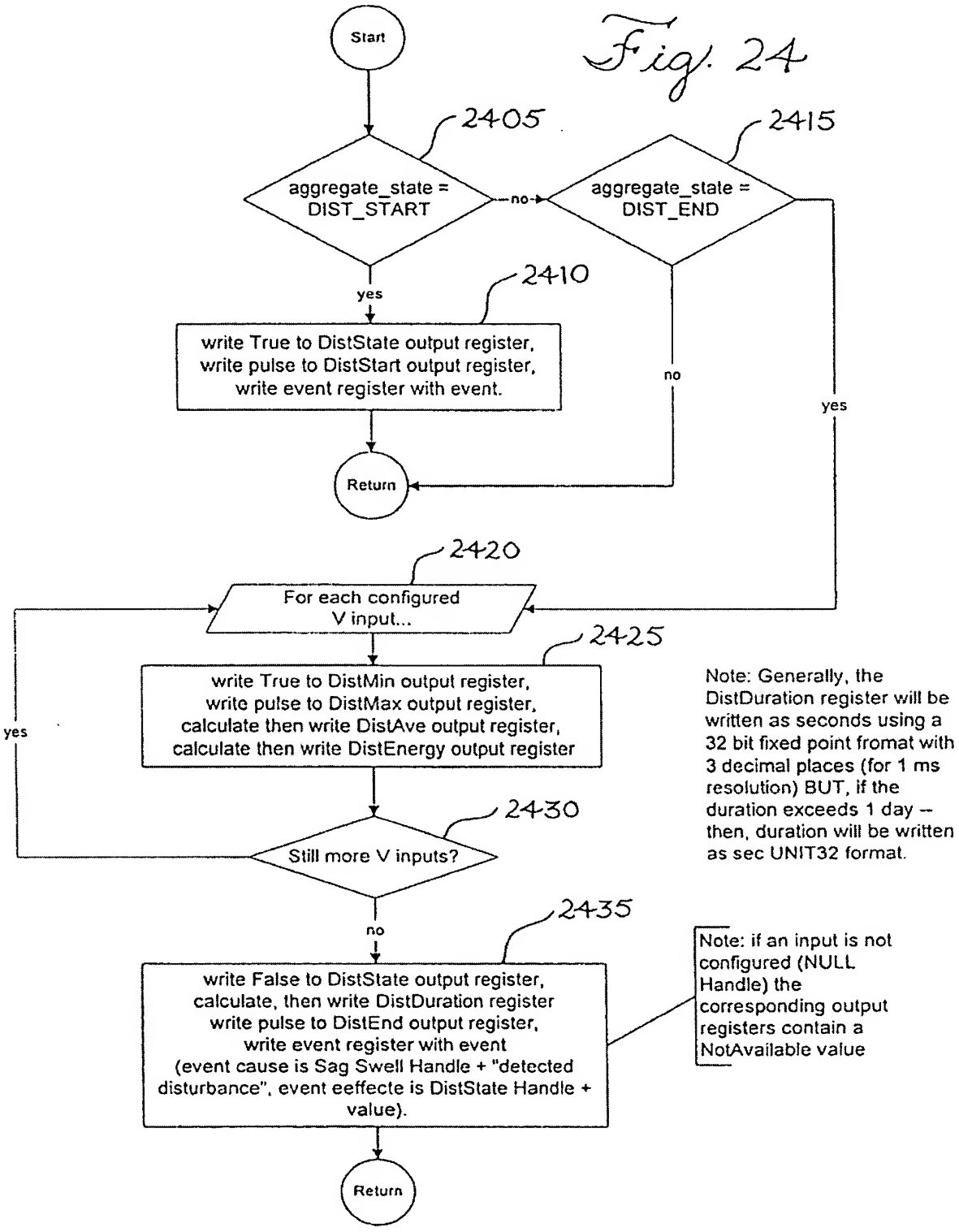
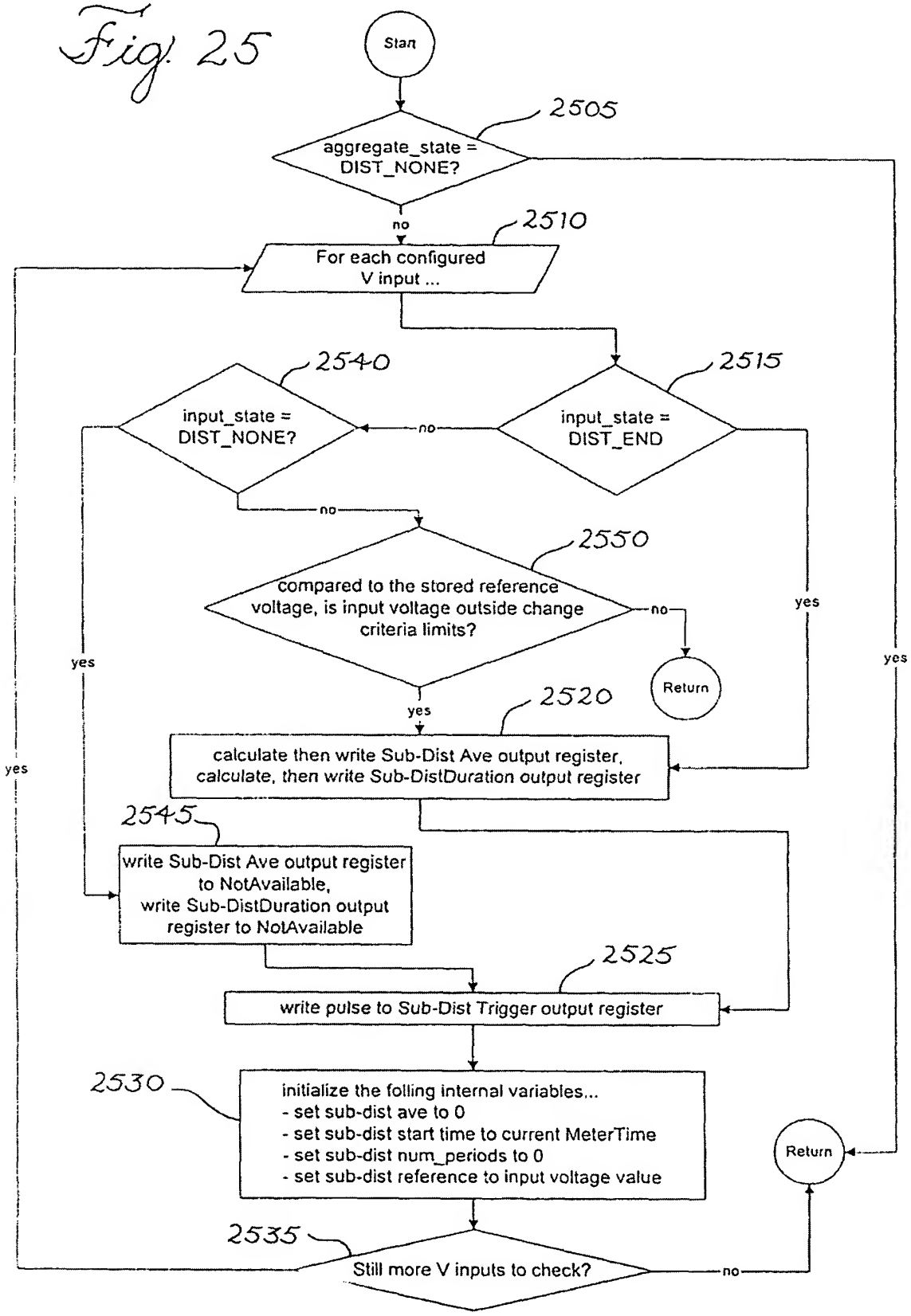

Start
2405
aggregate_state = DIST_START
no
2415
aggregate_state = DIST_END
yes
2410
write True to DistState output register, write pulse to DistStart output register, write event register with event.
no
yes
Return
2420
For each configured V input...
2425
write True to DistMin output register, write pulse to DistMax output register, calculate then write DistAve output register, calculate then write DistEnergy output register
yes
2430
Still more V inputs?
no
2435
write False to DistState output register, calculate, then write DistDuration register write pulse to DistEnd output register, write event register with event (event cause is Sag Swell Handle + "detected disturbance", event eeffecte is DistState Handle + value).
Return
Note: Generally, the DistDuration register will be written as seconds using a 32 bit fixed point fromat with 3 decimal places (for 1 ms resolution) BUT, if the duration exceeds 1 day -- then, duration will be written as sec UNIT32 format.
Note: if an input is not configured (NULL Handle) the corresponding output registers contain a NotAvailable value

Fig. 25


Start
2505
aggregate_state = DIST_NONE?
no
2510
For each configured V input ...
2540
input_state = DIST_NONE?
no
2515
input_state = DIST_END
yes
no
2550
compared to the stored reference voltage, is input voltage outside change criteria limits?
no
Return
yes
yes
2520
calculate then write Sub-Dist Ave output register, calculate, then write Sub-DistDuration output register
yes
2545
write Sub-Dist Ave output register to NotAvailable, write Sub-DistDuration output register to NotAvailable
2525
write pulse to Sub-Dist Trigger output register
2530
initialize the folling internal variables...
- set sub-dist ave to 0
- set sub-dist start time to current MeterTime
- set sub-dist num_periods to 0
- set sub-dist reference to input voltage value
Return
2535
Still more V inputs to check?
no
yes

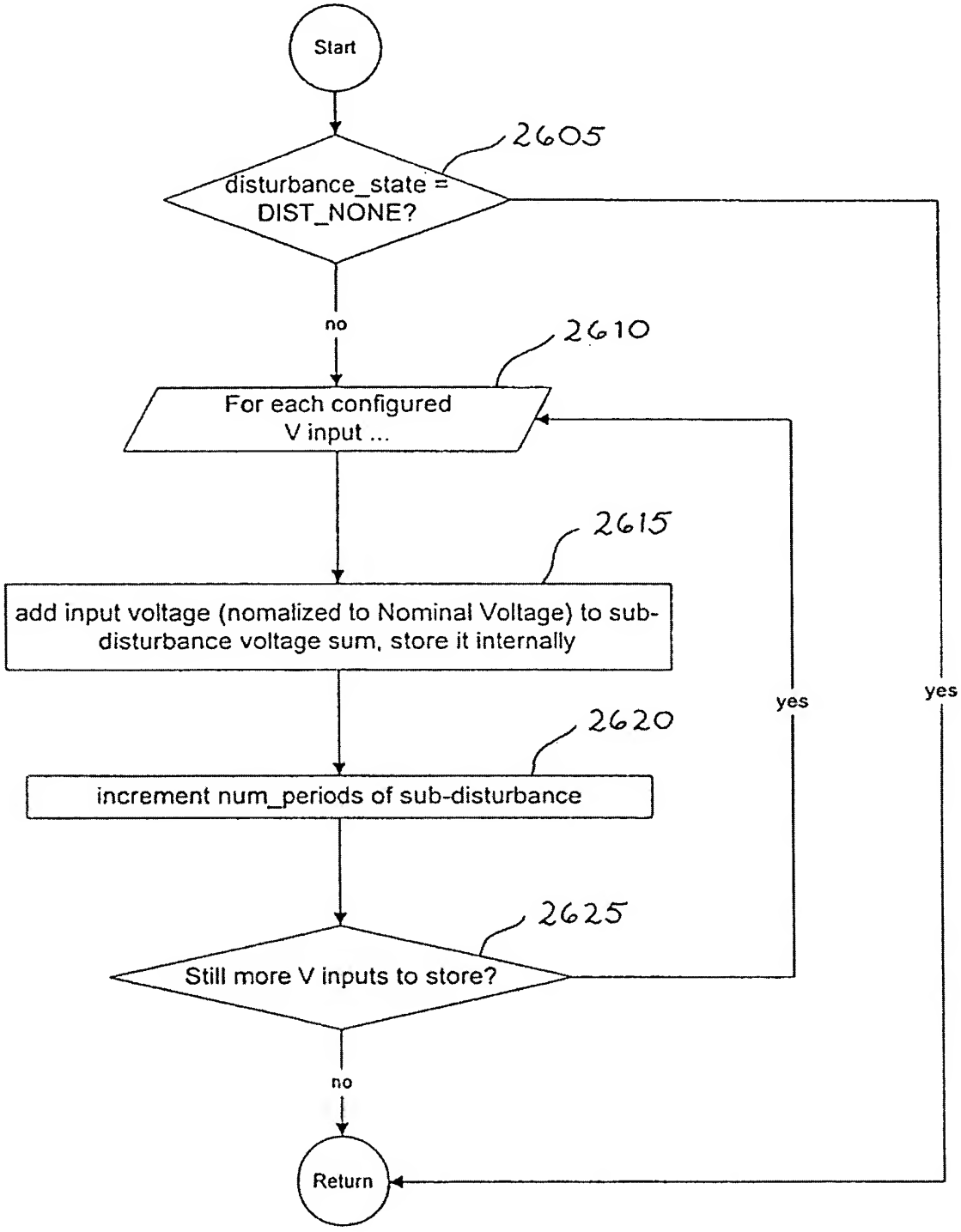
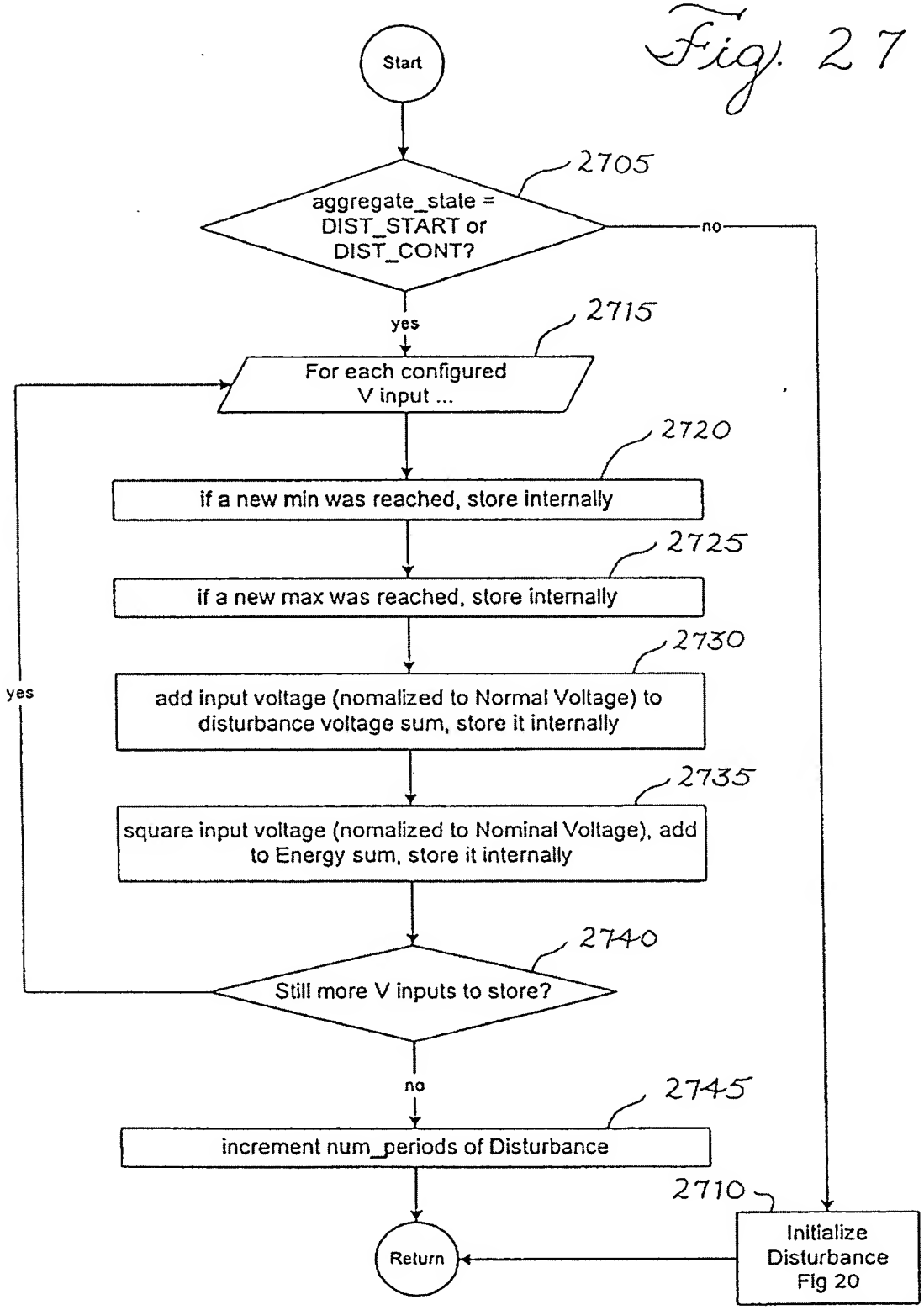

Start
2605
disturbance_state = DIST_NONE?
yes
no
2610
For each configured V input ...
2615
add input voltage (nomalized to Nominal Voltage) to sub-disturbance voltage sum, store it internally
2620
increment num_periods of sub-disturbance
2625
Still more V inputs to store?
yes
no
Return

Fig. 26

Fig. 27


Start
2705
aggregate_state = DIST_START or DIST_CONT?
no
yes
2715
For each configured V input ...
2720
if a new min was reached, store internally
2725
if a new max was reached, store internally
2730
add input voltage (nomalized to Normal Voltage) to disturbance voltage sum, store it internally
2735
square input voltage (nomalized to Nominal Voltage), add to Energy sum, store it internally
2740
Still more V inputs to store?
yes
no
2745
increment num_periods of Disturbance
2710
Initialize Disturbance Fig 20
Return

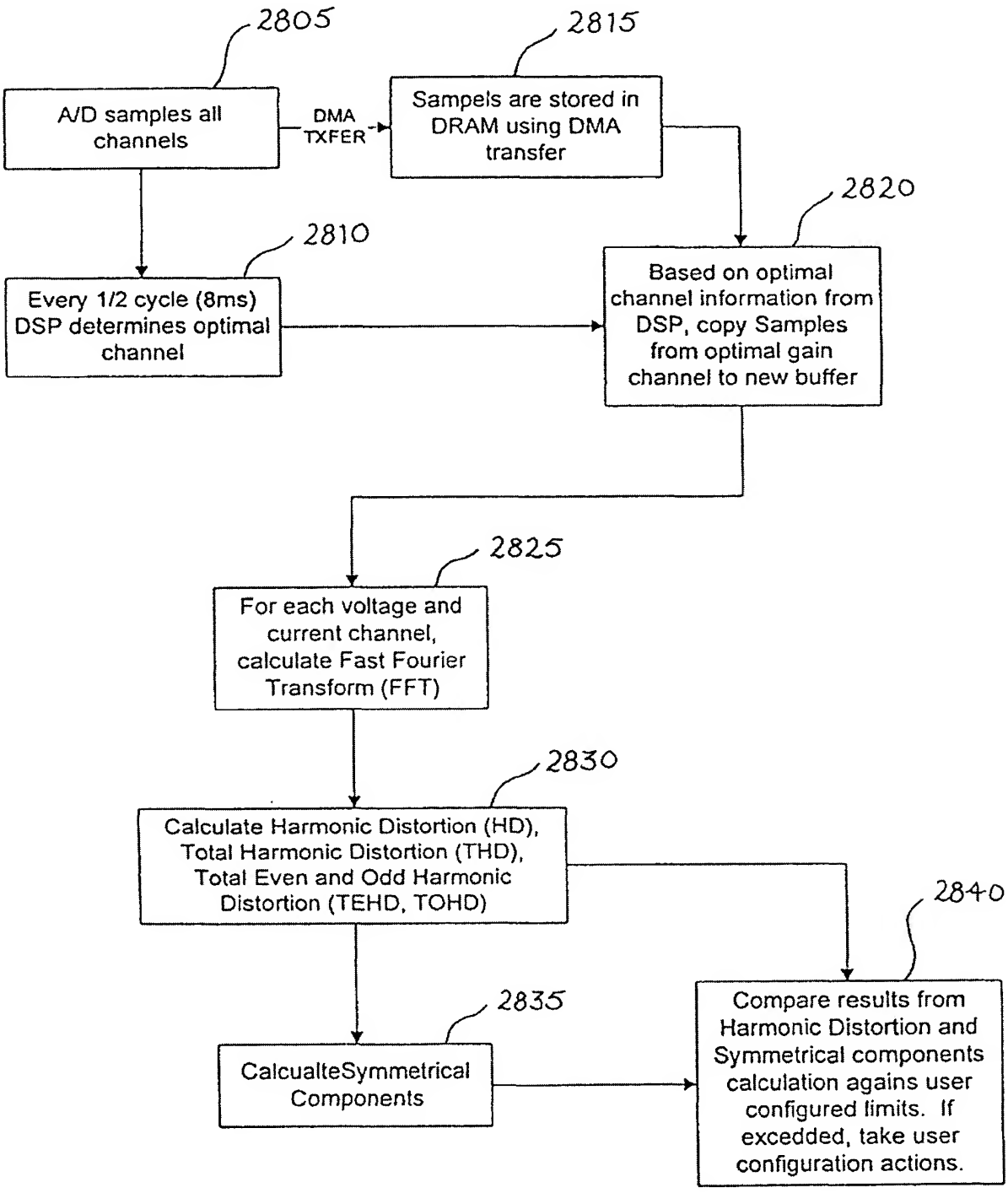
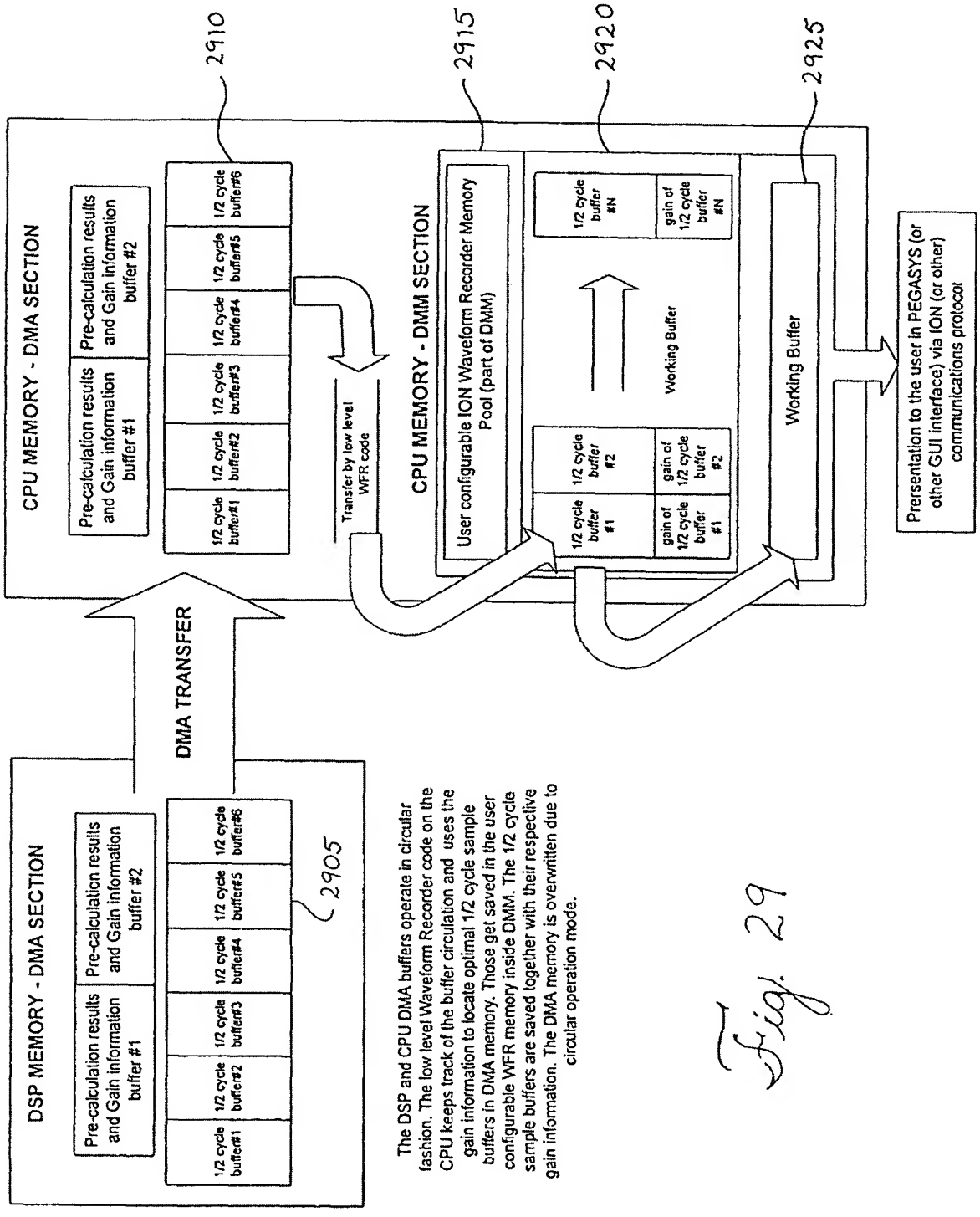

2805
A/D samples all channels
DMA TXFER
2815
Sampels are stored in DRAM using DMA transfer
2820
2810
Every 1/2 cycle (8ms) DSP determines optimal channel
Based on optimal channel information from DSP, copy Samples from optimal gain channel to new buffer
2825
For each voltage and current channel, calculate Fast Fourier Transform (FFT)
2830
Calculate Harmonic Distortion (HD), Total Harmonic Distortion (THD), Total Even and Odd Harmonic Distortion (TEHD, TOHD)
2840
2835
CalcualteSymmetrical Components
Compare results from Harmonic Distortion and Symmetrical components calculation agains user configured limits. If excedded, take user configuration actions.

Fig. 28



The DSP and CPU DMA buffers operate in circular fashion. The low level Waveform Recorder code on the CPU keeps track of the buffer circulation and uses the gain information to locate optimal 1/2 cycle sample buffers in DMA memory. Those get saved in the user configurable WFR memory inside DMM. The 1/2 cycle sample buffers are saved together with their respective gain information. The DMA memory is overwritten due to circular operation mode.

Fig. 29

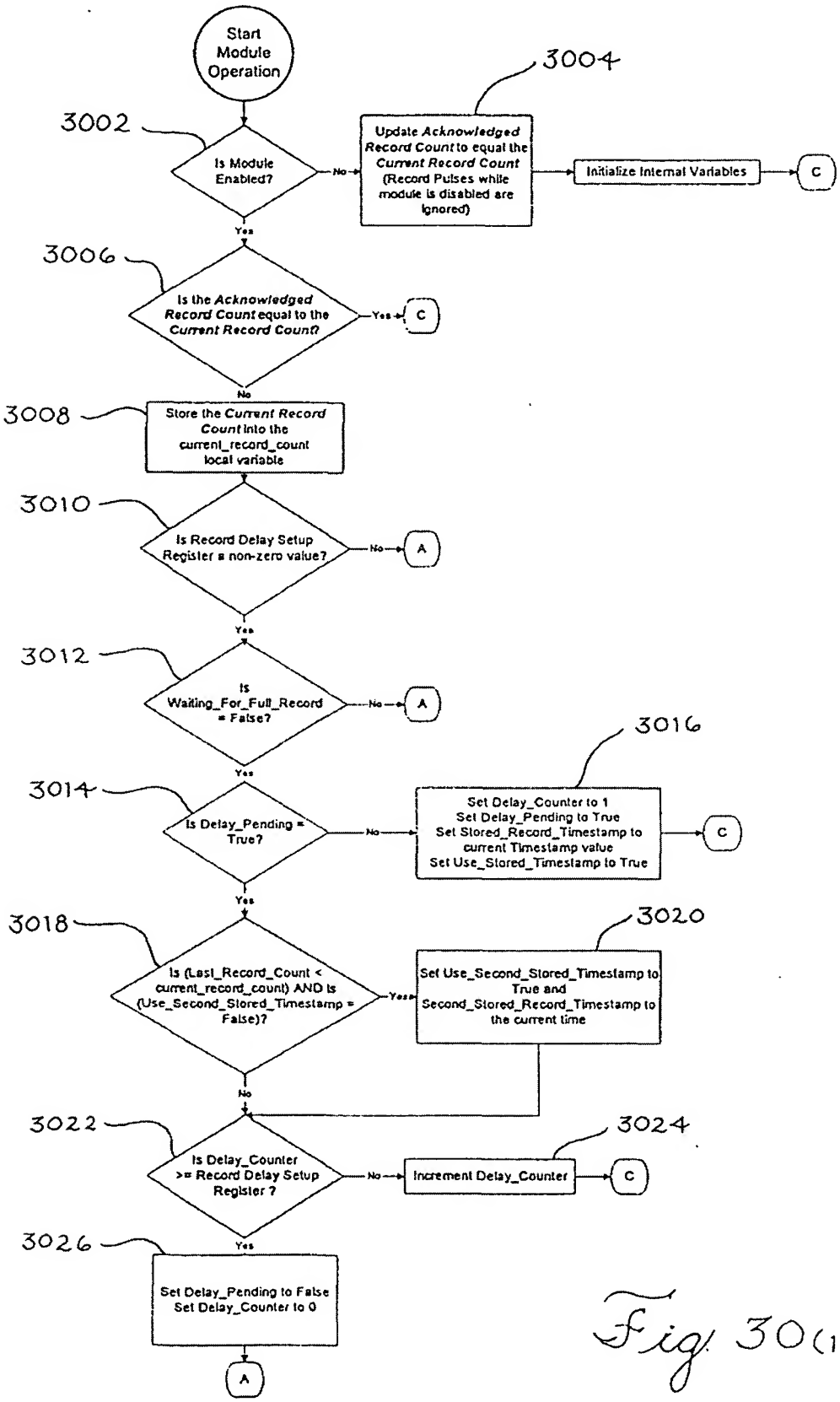

Start Module Operation
3002
Is Module Enabled?
No
3004
Update Acknowledged Record Count to equal the Current Record Count (Record Pulses while module is disabled are ignored)
Initialize Internal Variables
C
Yes
3006
Is the Acknowledged Record Count equal to the Current Record Count?
Yes
C
No
3008
Store the Current Record Count into the current_record_count local variable
3010
Is Record Delay Setup Register = non-zero value?
No
A
Yes
3012
Is Waiting_For_Full_Record = False?
No
A
Yes
3016
3014
Is Delay_Pending = True?
No
Set Delay_Counter to 1
Set Delay_Pending to True
Set Stored_Record_Timestamp to current Timestamp value
Set Use_Stored_Timestamp to True
C
Yes
3018
3020
Is (Last_Record_Count < current_record_count) AND Is (Use_Second_Stored_Timestamp = False)?
Yes
Set Use_Second_Stored_Timestamp to True and Second_Stored_Record_Timestamp to the current time
No
3022
3024
Is Delay_Counter >= Record Delay Setup Register ?
No
Increment Delay_Counter
C
Yes
3026
Set Delay_Pending to False
Set Delay_Counter to 0
A

Fig. 30(1)

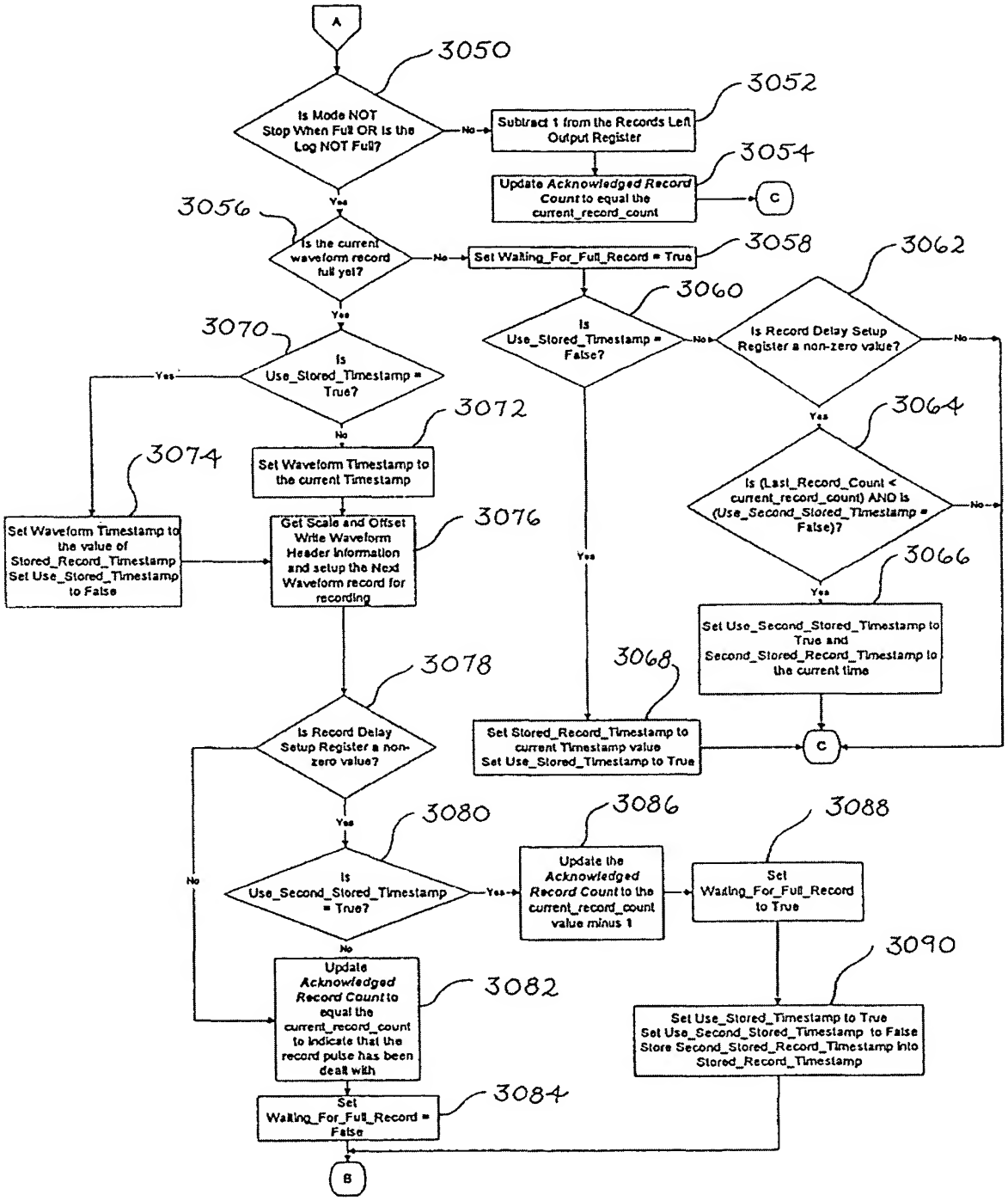

A
3050
Is Mode NOT Stop When Full OR Is the Log NOT Full?
No
3052
Subtract 1 from the Records Left Output Register
3054
Update Acknowledged Record Count to equal the current_record_count
C
Yes
3056
Is the current waveform record full yet?
No
3058
Set Waiting_For_Full_Record = True
3060
Is Use_Stored_Timestamp = False?
No
3062
Is Record Delay Setup Register a non-zero value?
No
Yes
3064
Is (Last_Record_Count < current_record_count) AND Is (Use_Second_Stored_Timestamp = False)?
No
Yes
3066
Set Use_Second_Stored_Timestamp to True and Second_Stored_Record_Timestamp to the current time
3068
Set Stored_Record_Timestamp to current Timestamp value
Set Use_Stored_Timestamp to True
C
Yes
3070
Is Use_Stored_Timestamp = True?
Yes
No
3072
Set Waveform Timestamp to the current Timestamp
3074
Set Waveform Timestamp to the value of Stored_Record_Timestamp
Set Use_Stored_Timestamp to False
3076
Get Scale and Offset
Write Waveform Header information and setup the Next Waveform record for recording
3078
Is Record Delay Setup Register a non-zero value?
Yes
No
3080
Is Use_Second_Stored_Timestamp = True?
Yes
No
3086
Update the Acknowledged Record Count to the current_record_count value minus 1
3088
Set Waiting_For_Full_Record to True
3090
Set Use_Stored_Timestamp to True
Set Use_Second_Stored_Timestamp to False
Store Second_Stored_Record_Timestamp into Stored_Record_Timestamp
3082
Update Acknowledged Record Count to equal the current_record_count to indicate that the record pulse has been dealt with
3084
Set Waiting_For_Full_Record = False
B

Fig. 30 (2)

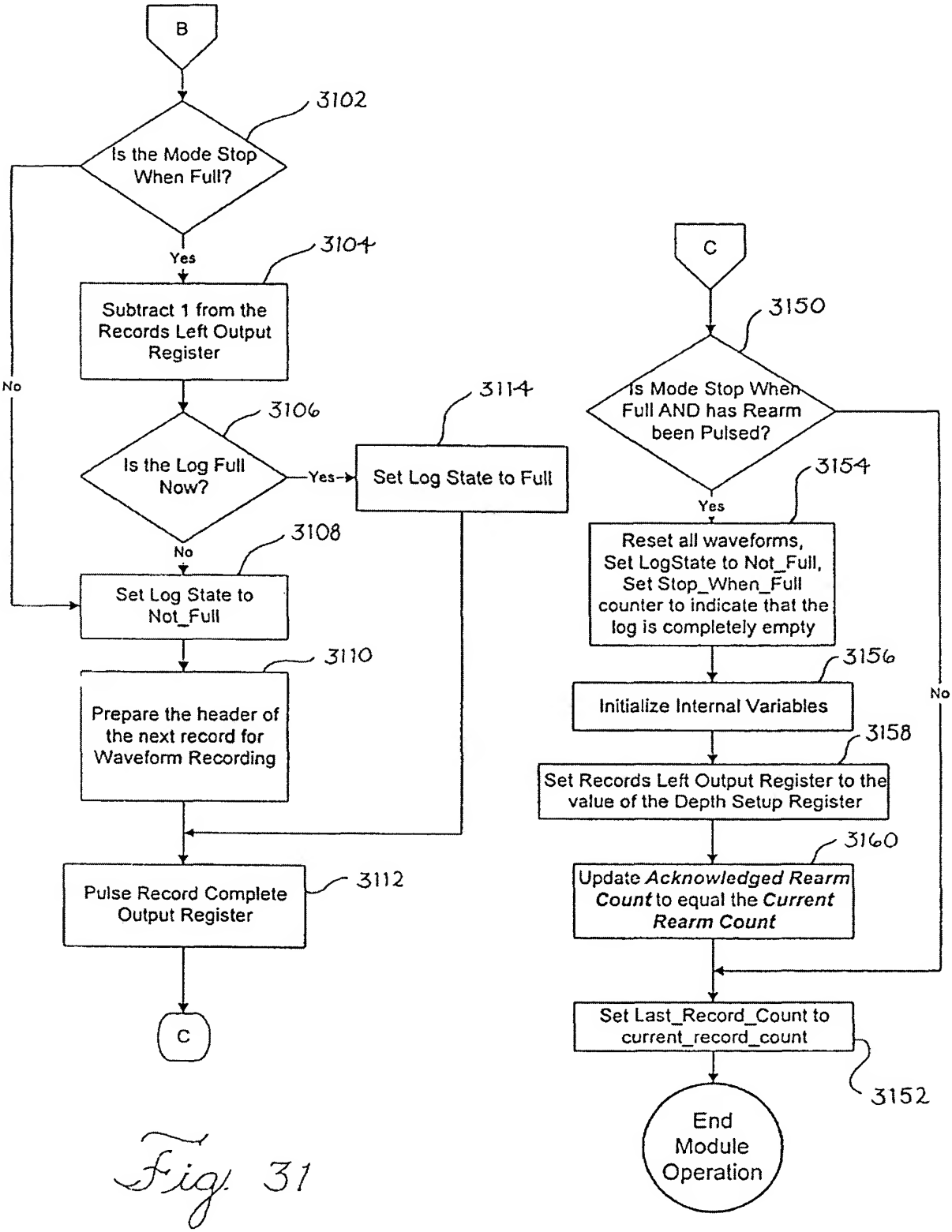

B
3102
Is the Mode Stop When Full?
Yes
No
3104
Subtract 1 from the Records Left Output Register
3106
Is the Log Full Now?
Yes
No
3114
Set Log State to Full
3108
Set Log State to Not_Full
3110
Prepare the header of the next record for Waveform Recording
3112
Pulse Record Complete Output Register
C
C
3150
Is Mode Stop When Full AND has Rearm been Pulsed?
Yes
No
3154
Reset all waveforms, Set LogState to Not_Full, Set Stop_When_Full counter to indicate that the log is completely empty
3156
Initialize Internal Variables
3158
Set Records Left Output Register to the value of the Depth Setup Register
3160
Update *Acknowledged Rearm Count* to equal the *Current Rearm Count*
Set Last_Record_Count to current_record_count
3152
End Module Operation

Fig. 31

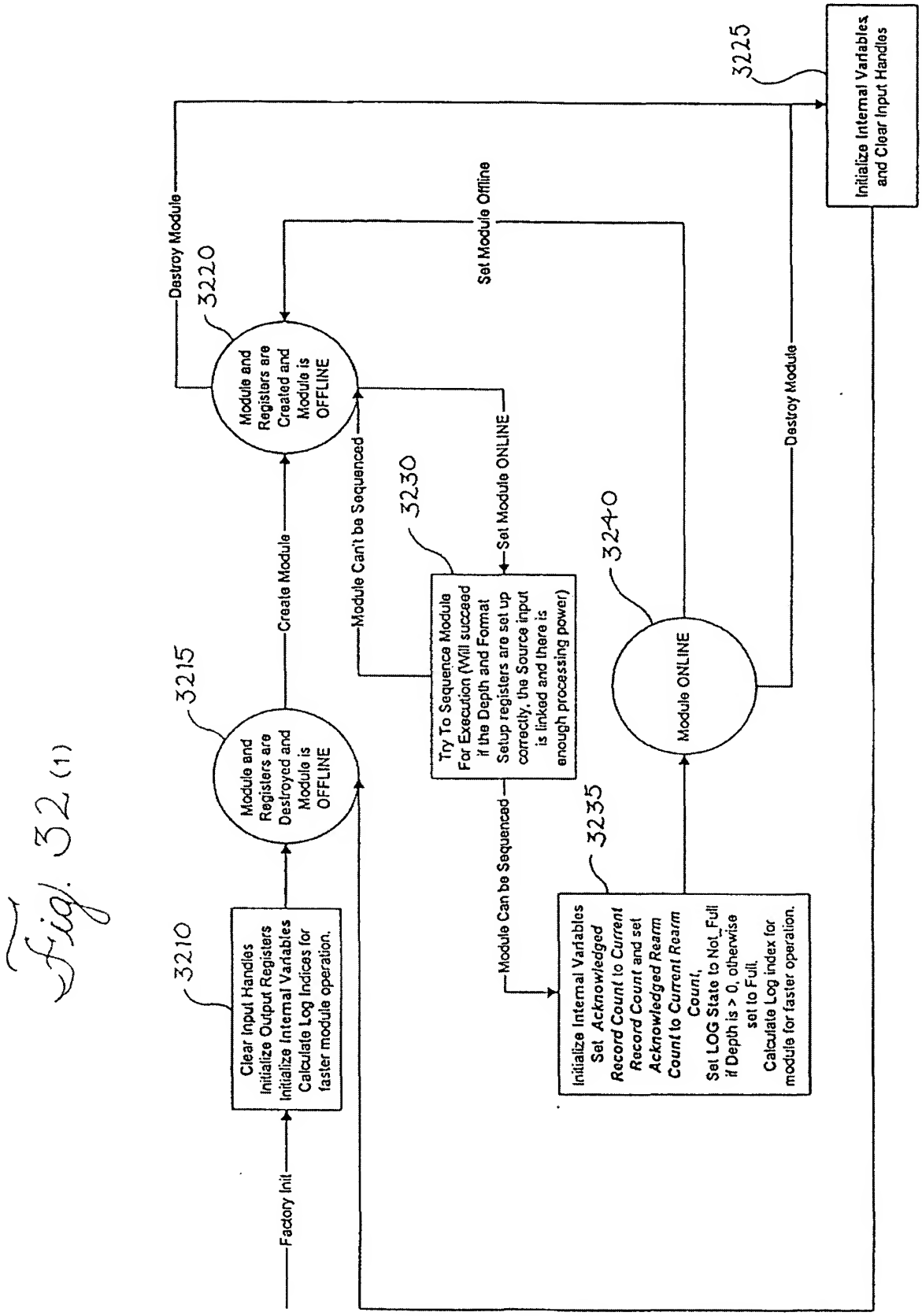

Factory Init
3210
Clear Input Handles
Initialize Output Registers
Initialize Internal Variables
Calculate Log Indices for faster module operation.
3215
Module and Registers are Destroyed and Module is OFFLINE
Create Module
3220
Module and Registers are Created and Module is OFFLINE
Destroy Module
Module Can't be Sequenced
3230
Try To Sequence Module For Execution (Will succeed if the Depth and Format Setup registers are set up correctly, the Source input is linked and there is enough processing power)
Set Module ONLINE
Set Module Offline
Module Can be Sequenced
3235
Initialize Internal Variables
Set Acknowledged Record Count to Current Record Count and set Acknowledged Rearm Count to Current Rearm Count,
Set LOG State to Not_Full if Depth is > 0, otherwise set to Full.
Calculate Log index for module for faster operation.
3240
Module ONLINE
Destroy Module
3225
Initialize Internal Variables and Clear Input Handles

Fig. 32 (1)

Fig. 32(2)

Internal Variables

Delay_Pending indicates whether a waveform Record Delay is currently active. Set to False on initialization of internal variables.

Delay_Counter indicates how many cycles the delay has been pending for. Set to 0 on initialization of internal variables.

Waiting_For_Full_Record indicates a record pulse has been detected, but the current waveform record is not full yet. Set to False on initialization of internal variables.

Use_Stored_Timestamp indicates that the next waveform to be stored should use Stored_Record_Timestamp instead of the current cycle timestamp. Set to False on initialization of internal variables.

Stored_Record_Timestamp indicates the timestamp to use for the next waveform, if Used_Stored_Timestamp is True. Never initialized since it will only be used when Use_Stored_Timestamp is True, which indicates that Stored_Record_Timestamp has been set.

Use_Second_Stored_Timestamp indicates that the next waveform to be stored should use Stored_Record_Timestamp and that the waveform following should use Second_Stored_Record_Timestamp instead of the current cycle timestamp. If it is True, then Use_Stored_Timestamp is also True. Set to False on initialization of internal variables.

Second_Stored_Record_Timestamp indicates the timestamp to use for the waveform following the next waveform, if Used_Second_Stored_Timestamp is True. It will only be set if Stored_Record_Timestamp has also been set. Never initialized since it will only be used when Use_Second_Stored_Timestamp is True, which indicates that Second_Stored_Record_Timestamp has been set.

Last_Record_Count indicates the Record count on last module execution. It is set to the current Record input count on initialization of internal variables.

Acknowledged Record Count indicates the Record pulse count that has been acknowledged already. If this value is equal to the number of pulses on the Record input, then the module does not need to store any new waveforms. This value is actually stored in the Input Handle structure for the Record input handle.

Acknowledged Rearm Count indicates the Rearm pulse count that has been acknowledged already. If this value is equal to the number of pulses on the Rearm input, then the Rearm input has not been pulsed. This value is actually stored in the Input Handle structure for the Rearm input handle.

Local Variables

Current Record Count indicates the pulse count in the register connected to the Record input link. If this value is greater than the Acknowledged Record Count then the module must store a new waveform. This value is copied into the current_record_count local variable at the start of the operate function.

Current Rearm Count indicates the pulse count in the register connected to the Rearm input link. If this value is greater than the Acknowledged Rearm Count then the module must rearm itself.

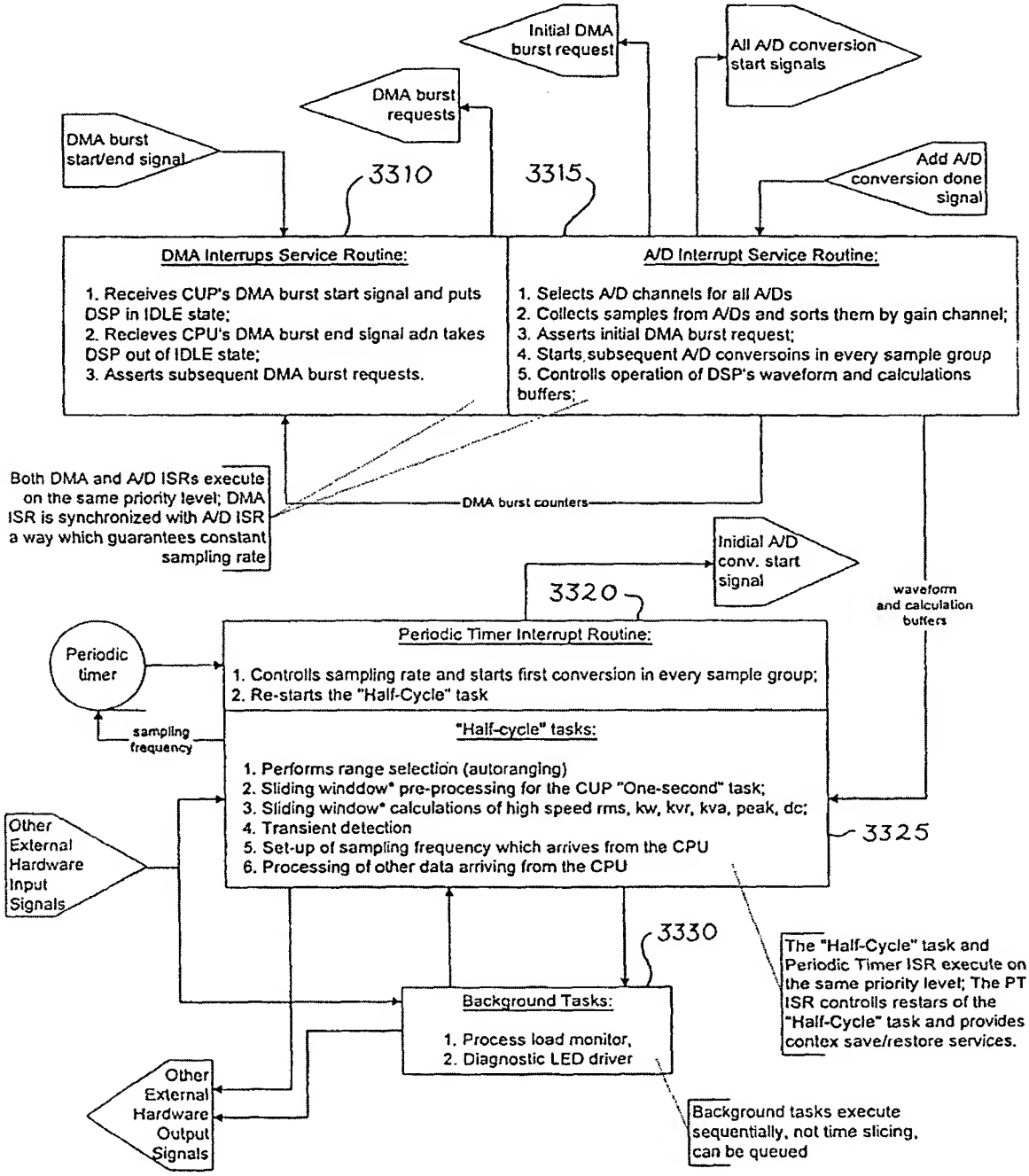

Initial DMA burst request
All A/D conversion start signals
DMA burst requests
DMA burst start/end signal
3310
3315
Add A/D conversion done signal
DMA Interrups Service Routine:
1. Receives CUP's DMA burst start signal and puts DSP in IDLE state;
2. Recieves CPU's DMA burst end signal adn takes DSP out of IDLE state;
3. Asserts subsequent DMA burst requests.
A/D Interrupt Service Routine:
1. Selects A/D channels for all A/Ds
2. Collects samples from A/Ds and sorts them by gain channel;
3. Asserts initial DMA burst request;
4. Starts subsequent A/D conversoins in every sample group
5. Controlls operation of DSP's waveform and calculations buffers;
Both DMA and A/D ISRs execute on the same priority level; DMA ISR is synchronized with A/D ISR a way which guarantees constant sampling rate
DMA burst counters
Inidial A/D conv. start signal
3320
waveform and calculation buffers
Periodic timer
Periodic Timer Interrupt Routine:
1. Controlls sampling rate and starts first conversion in every sample group;
2. Re-starts the "Half-Cycle" task
sampling frequency
"Half-cycle" tasks:
1. Performs range selection (autoranging)
2. Sliding winddow* pre-processing for the CUP "One-second" task;
3. Sliding window* calculations of high speed rms, kw, kvr, kva, peak, dc;
4. Transient detection
5. Set-up of sampling frequency which arrives from the CPU
6. Processing of other data arriving from the CPU
3325
Other External Hardware Input Signals
3330
The "Half-Cycle" task and Periodic Timer ISR execute on the same priority level; The PT ISR controlls restars of the "Half-Cycle" task and provides contex save/restore services.
Background Tasks:
1. Process load monitor,
2. Diagnostic LED driver
Other External Hardware Output Signals
Background tasks execute sequentially, not time slicing, can be queued

Fig. 33

Fig. 34

DMA Half-Cycle Activity Timeline

line half cycles	n-1	n	n+1	n+2	n+3	n+4	n+5
DSP ACTIVITY	A/D sample(n-1) & pre-process(n-3)(n-2)	A/D sample(n) & pre-process(n-2)(n-1)	A/D sample(n+1) & pre-process(n-1)(n)	A/D sample(n+2) & pre-process(n)(n+1)	A/D sample(n+3) & pre-process(n+1)(n+2)	A/D sample(n+4) & pre-process(n+2)(n+3)	A/D sample(n+5) & pre-process(n+3)(n+4)
DMA ACTIVITY	DMA transfer: samples(n-2) & pre-results(n-4)(n-3)	DMA transfer: samples(n-1) & pre-results(n-3)(n-2)	DMA transfer: samples(n) & pre-results(n-2)(n-1)	DMA transfer: samples(n+1) & pre-results(n-1)(n)	DMA transfer: samples(n+2) & pre-results(n)(n+1)	DMA transfer: samples(n+3) & pre-results(n+1)(n+2)	DMA transfer: samples(n+4) & qc_results(n+2)(n+3)
CPU ACTIVITY	process pre-results(n-5)(n-4) record waveform(n-5)	process pre-results(n-4)(n-3) record waveform(n-4)	process pre-results(n-3)(n-2) record waveform(n-3)	process pre-results(n-2)(n-1) record waveform(n-2)	process pre-results(n-1)(n) record waveform(n-1)	process pre-results(n)(n+1) record waveform(n)	process pre-results(n+1)(n+2) record waveform(n+1)

Waveform Recording is autoranged and delayed by 3 to 4 half cycles with respect to any real-time line event

Half Cycle calculation Results are delayed by 3 half cycles with respect to any real-time line event.

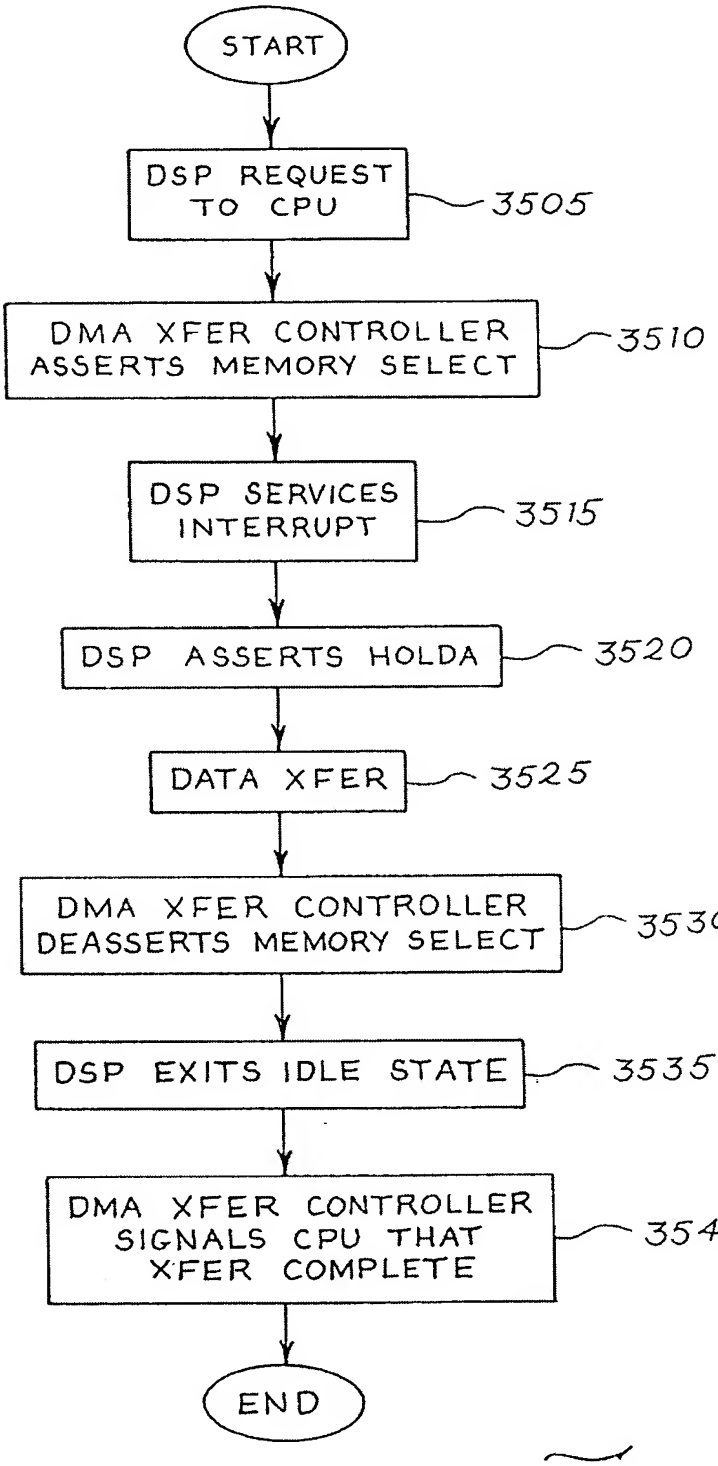

START
DSP REQUEST TO CPU
3505
DMA XFER CONTROLLER ASSERTS MEMORY SELECT
3510
DSP SERVICES INTERRUPT
3515
DSP ASSERTS HOLDA
3520
DATA XFER
3525
DMA XFER CONTROLLER DEASSERTS MEMORY SELECT
3530
DSP EXITS IDLE STATE
3535
DMA XFER CONTROLLER SIGNALS CPU THAT XFER COMPLETE
3540
END

Fig. 35

FIG. 36a

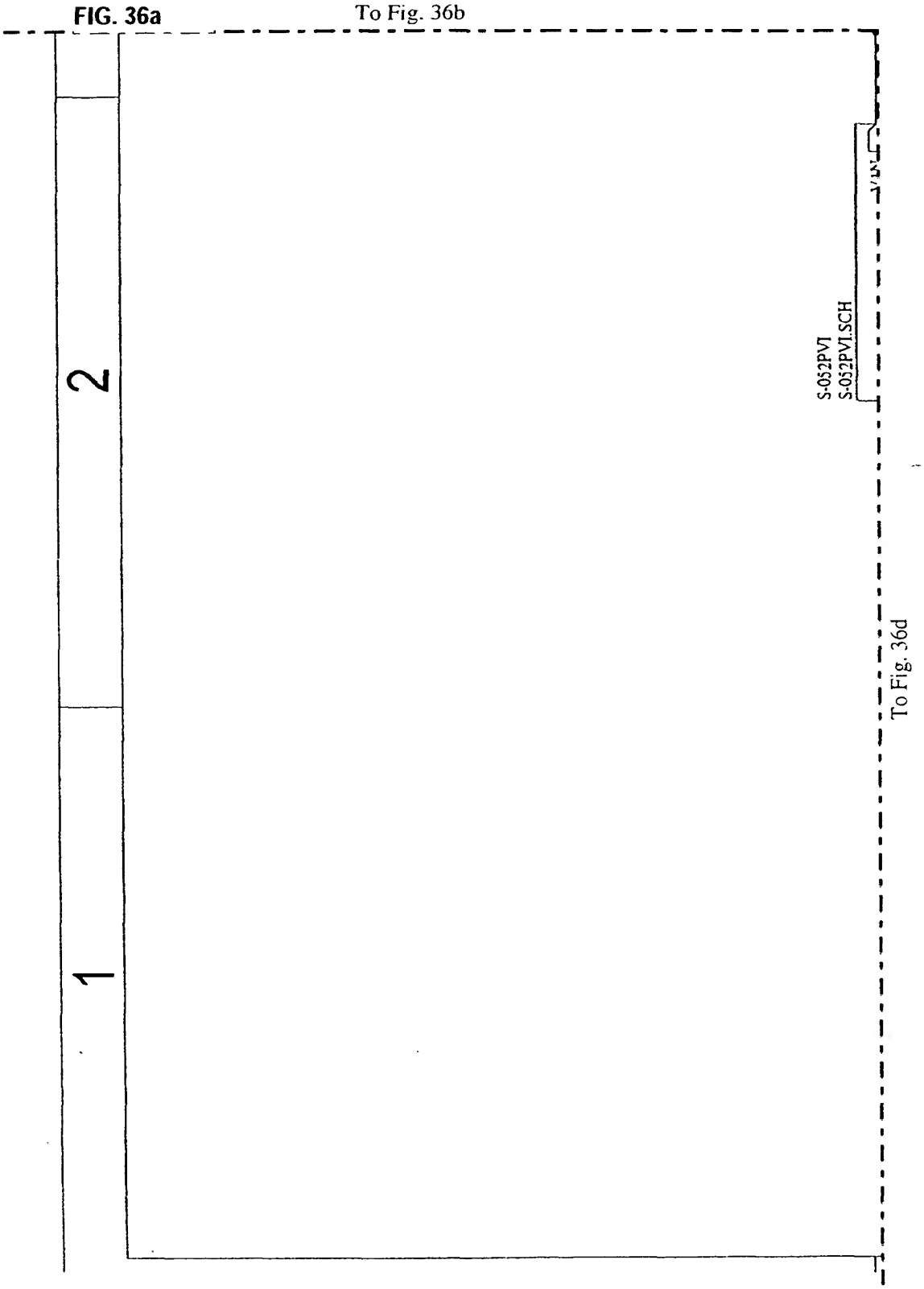


FIG. 36b

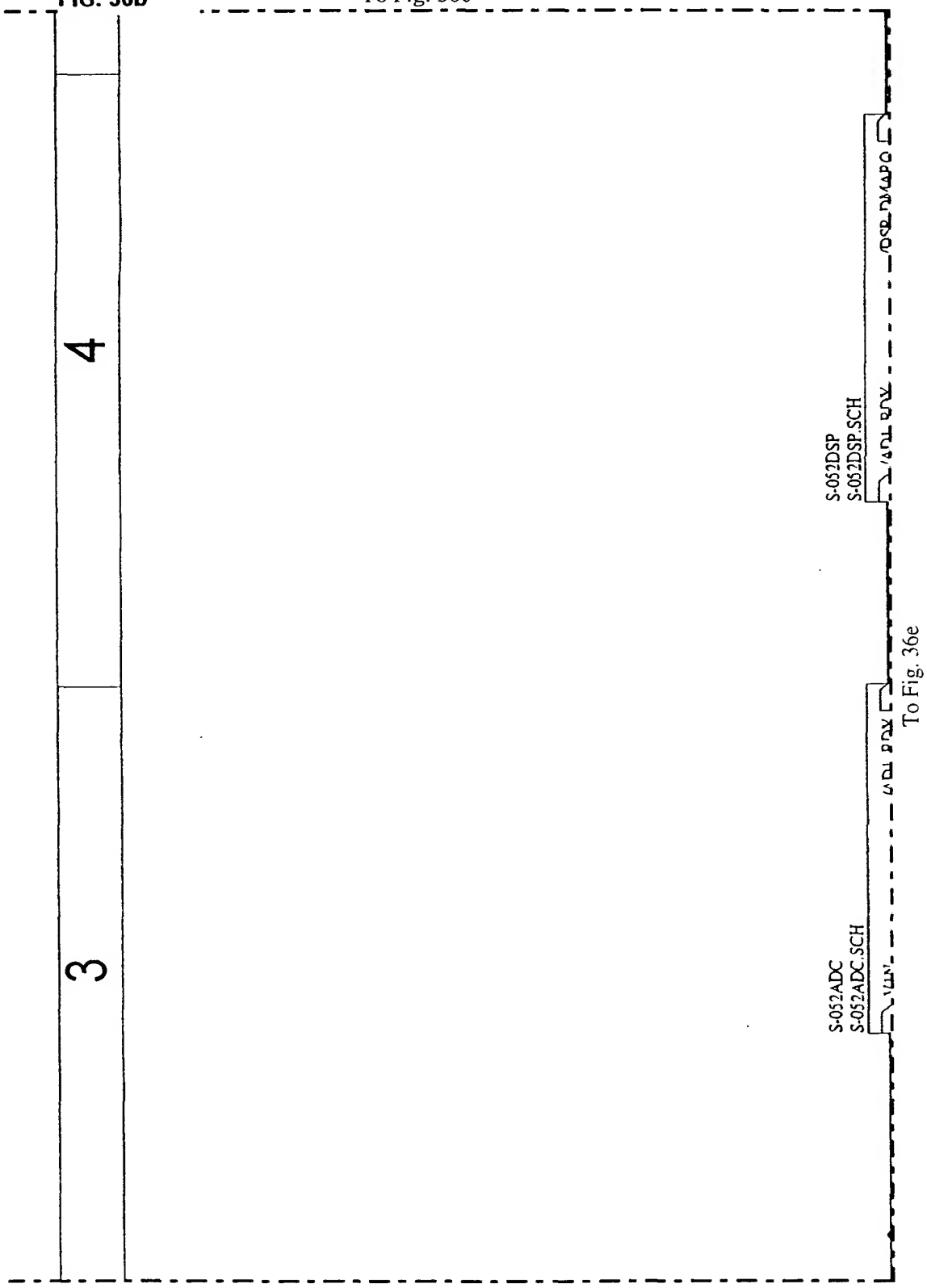

To Fig. 36c
4
3
S-052DSP
S-052DSP.SCH
S-052ADC
S-052ADC.SCH
To Fig. 36e
To Fig. 36a

FIG. 36c

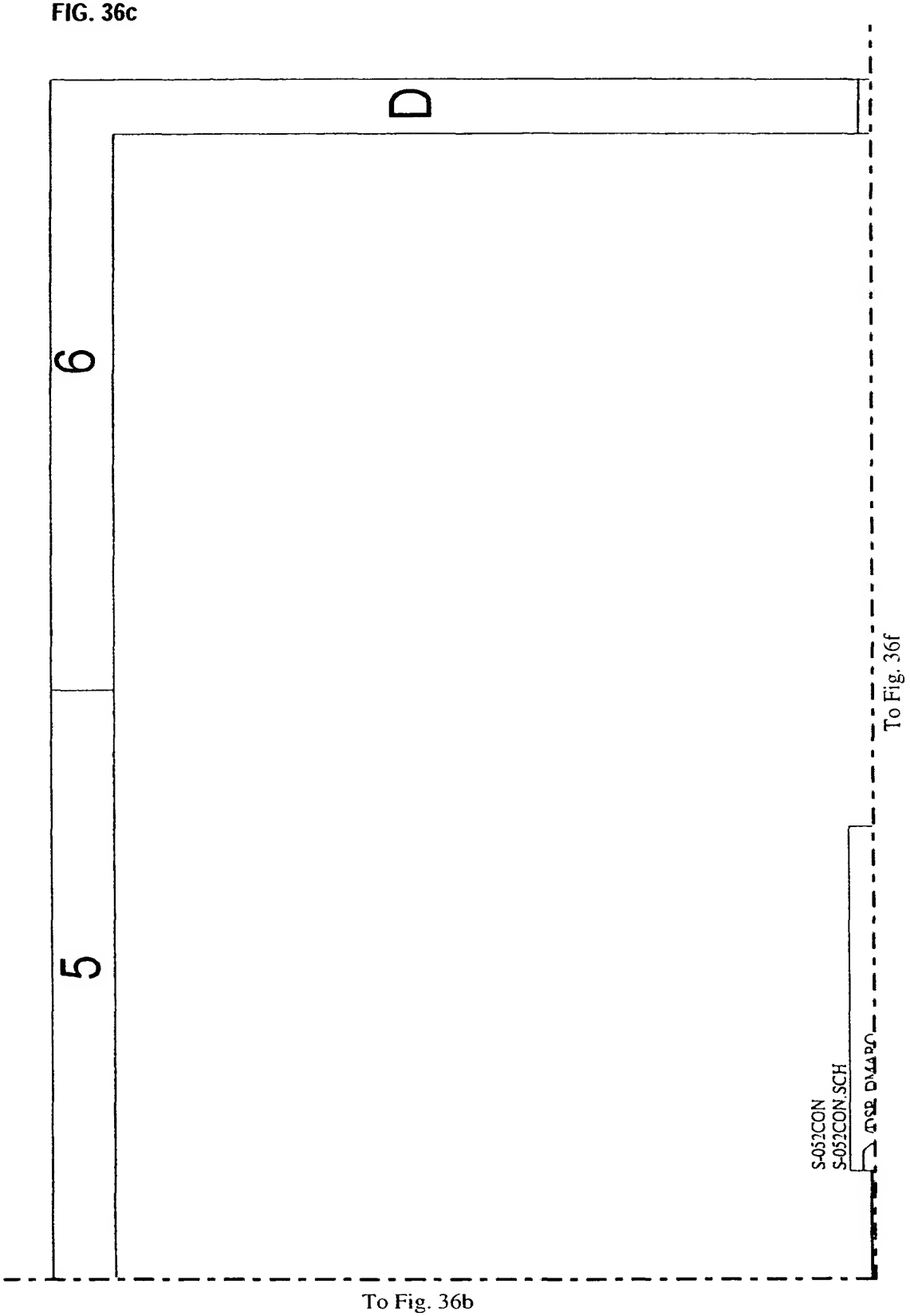


FIG. 36d

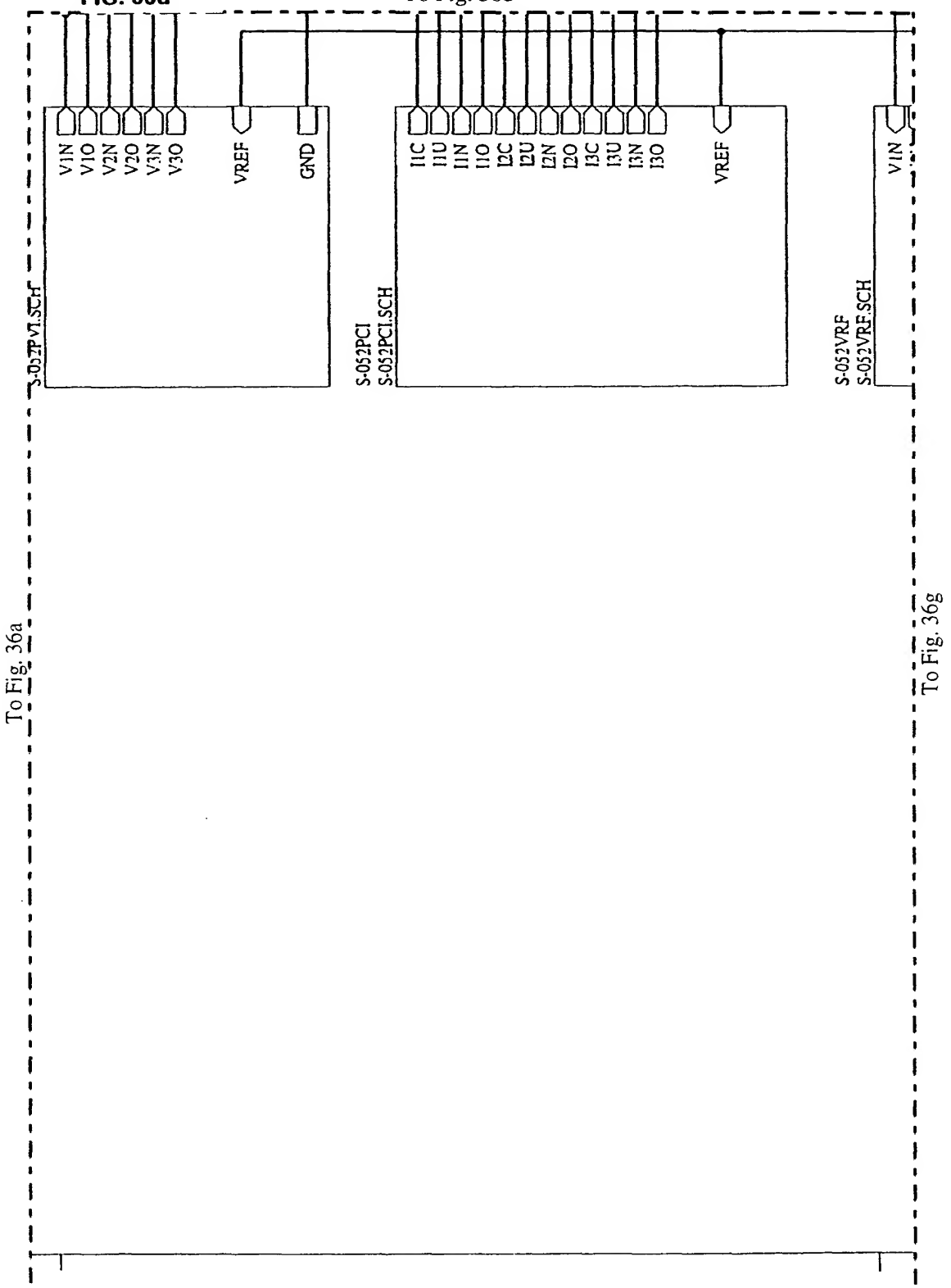

To Fig. 36e
V1N
V1O
V2N
V2O
V3N
V3O
VREF
GND
S-052PV1.SCH
I1C
I1U
I1N
I1O
I2C
I2U
I2N
I2O
I3C
I3U
I3N
I3O
VREF
S-052PCI
S-052PCI.SCH
V1N
S-052VRF
S-052VRF.SCH
To Fig. 36a
To Fig. 36g

FIG. 36e

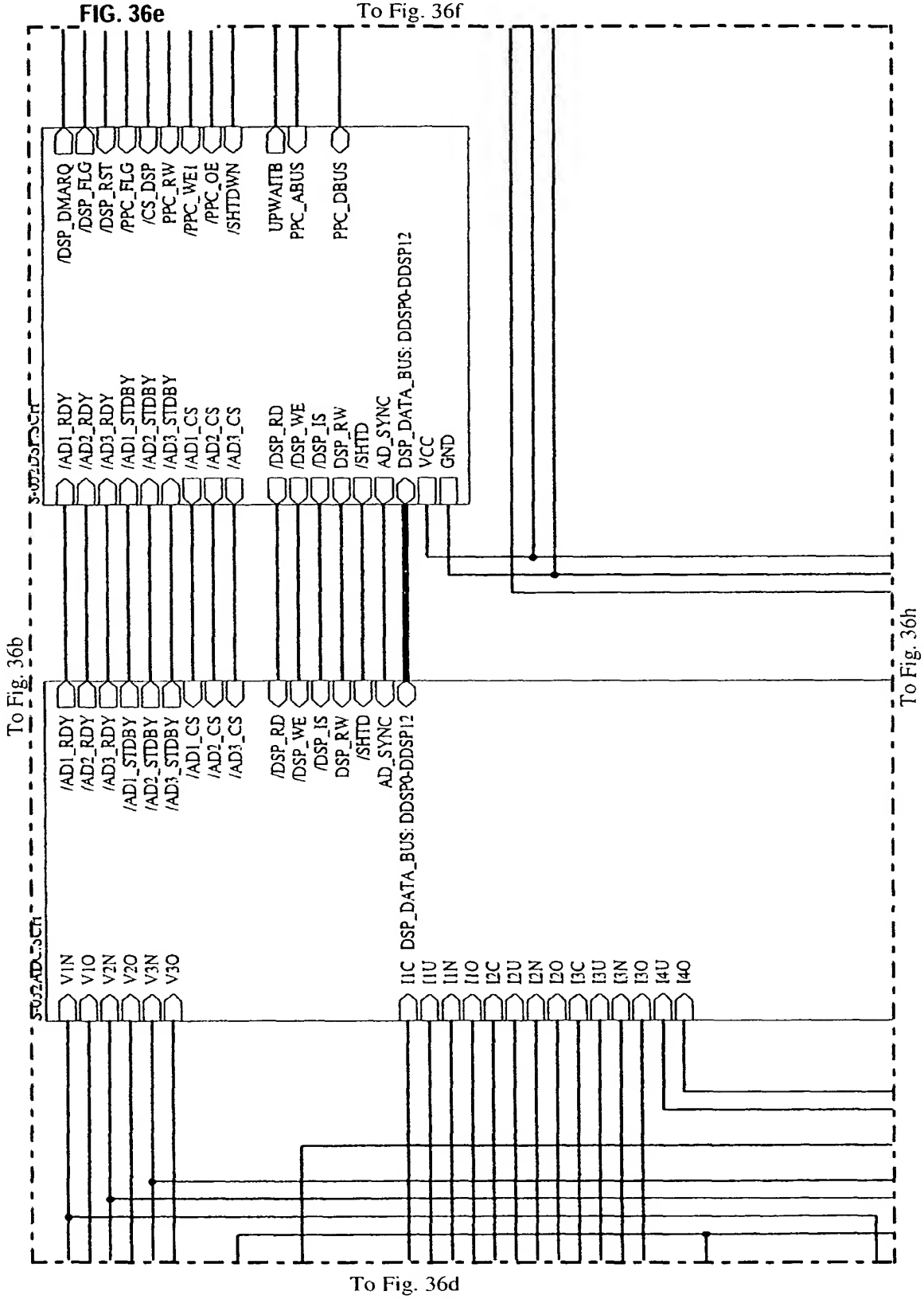
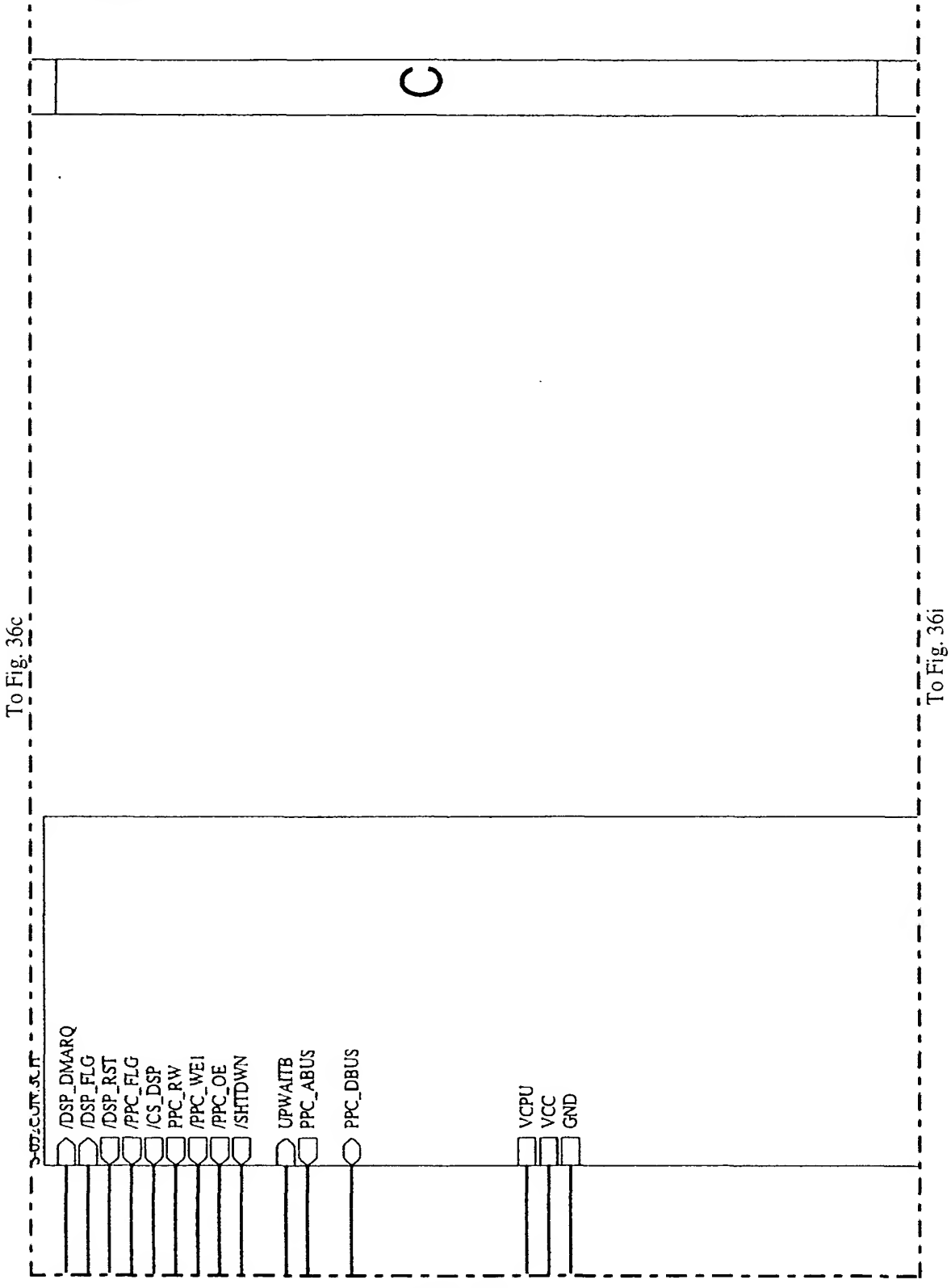

To Fig. 36f
/DSP_DMARQ
/DSP_FLG
/DSP_RST
/PPC_FLG
/CS_DSP
PPC_RW
/PPC_WEI
/PPC_OE
/SHTDWN
UPWAITB
PPC_ABUS
PPC_DBUS
/AD1_RDY
/AD2_RDY
/AD3_RDY
/AD1_STDBY
/AD2_STDBY
/AD3_STDBY
/AD1_CS
/AD2_CS
/AD3_CS
/DSP_RD
/DSP_WE
/DSP_IS
DSP_RW
/SHTD
AD_SYNC
DSP_DATA_BUS: DDSP0-DDSP12
VCC
GND
To Fig. 36b
To Fig. 36h
V1N
V1O
V2N
V2O
V3N
V3O
I1C
I1U
I1N
I1O
I2C
I2U
I2N
I2O
I3C
I3U
I3N
I3O
I4U
I4O
To Fig. 36d

FIG. 36f



To Fig. 36e

FIG. 36g

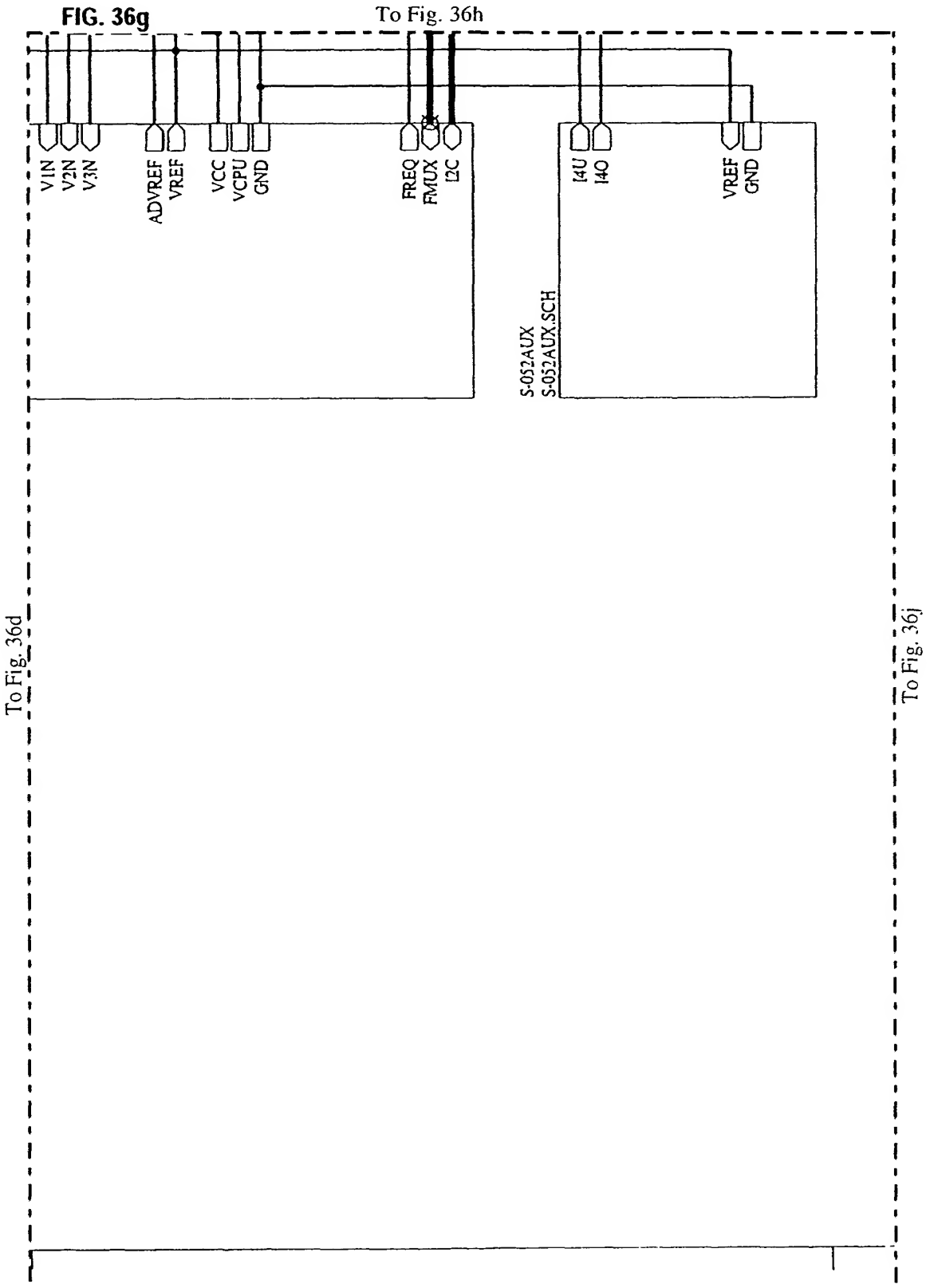

To Fig. 36h
V1N
V2N
V3N
ADVREF
VREF
VCC
VCPU
GND
FREQ
FMUX
I2C
I4U
I4O
VREF
GND
S-052AUX
S-052AUX.SCH
To Fig. 36d
To Fig. 36j

FIG. 36h

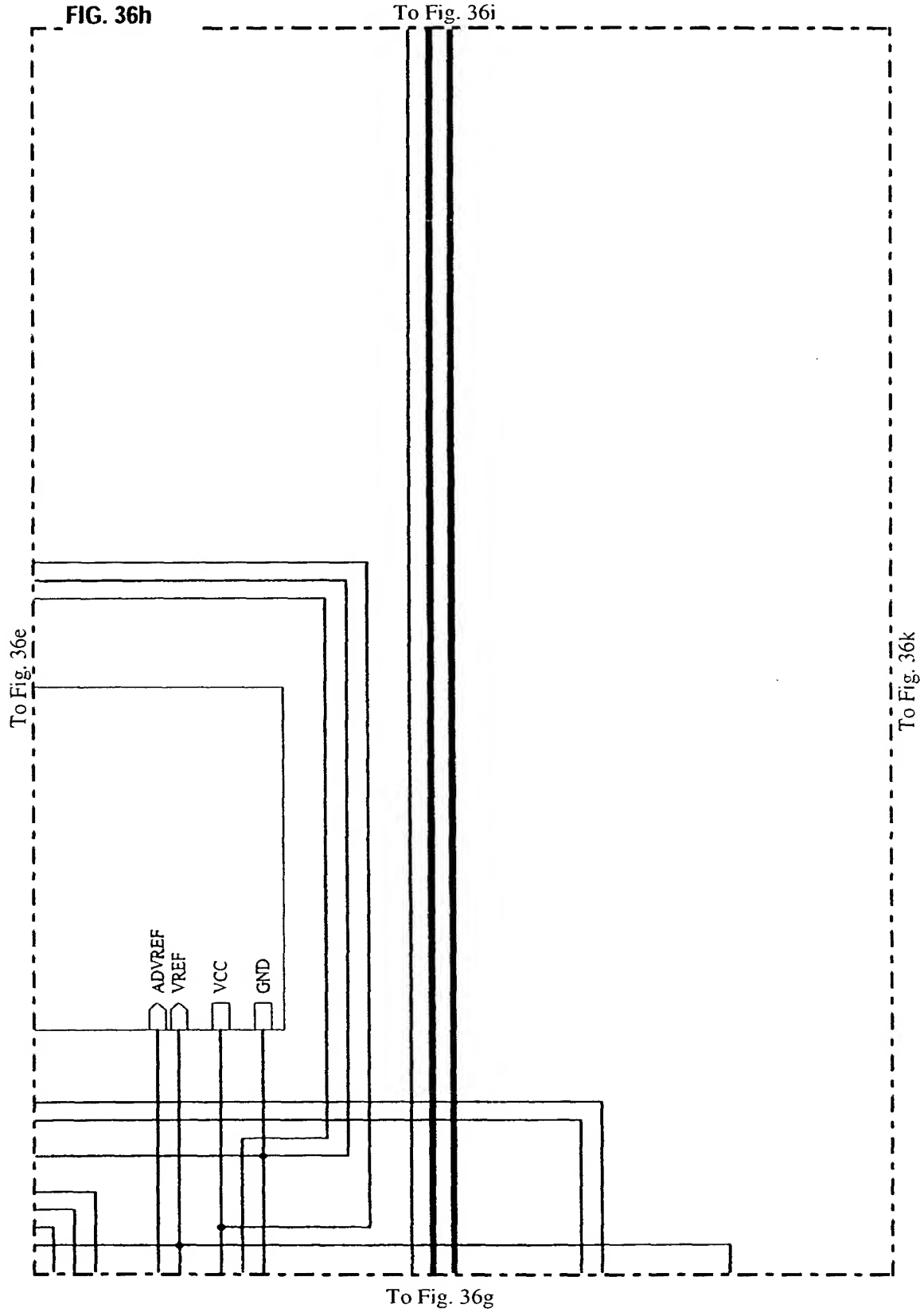


FIG. 36i

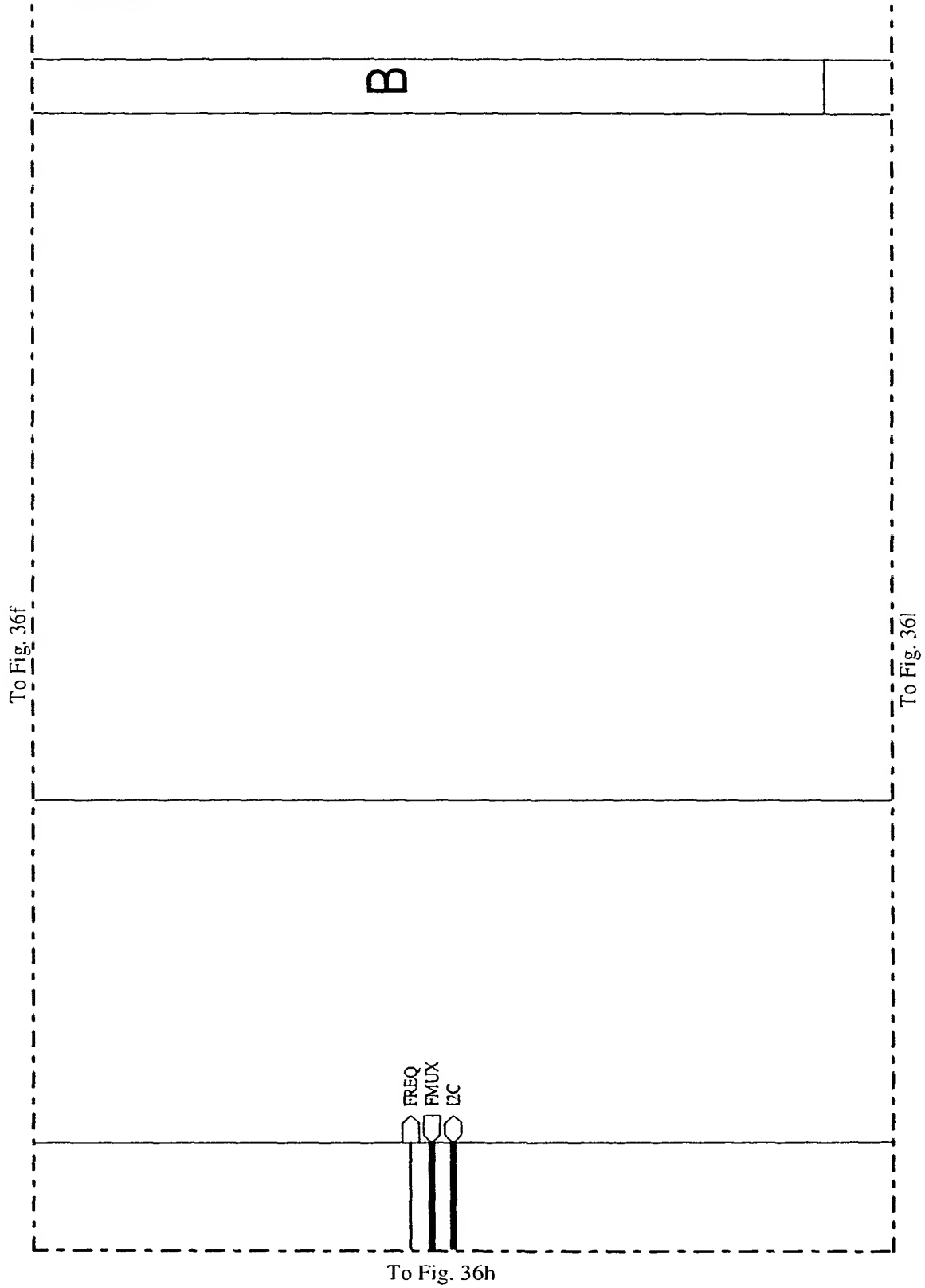


FIG. 36j

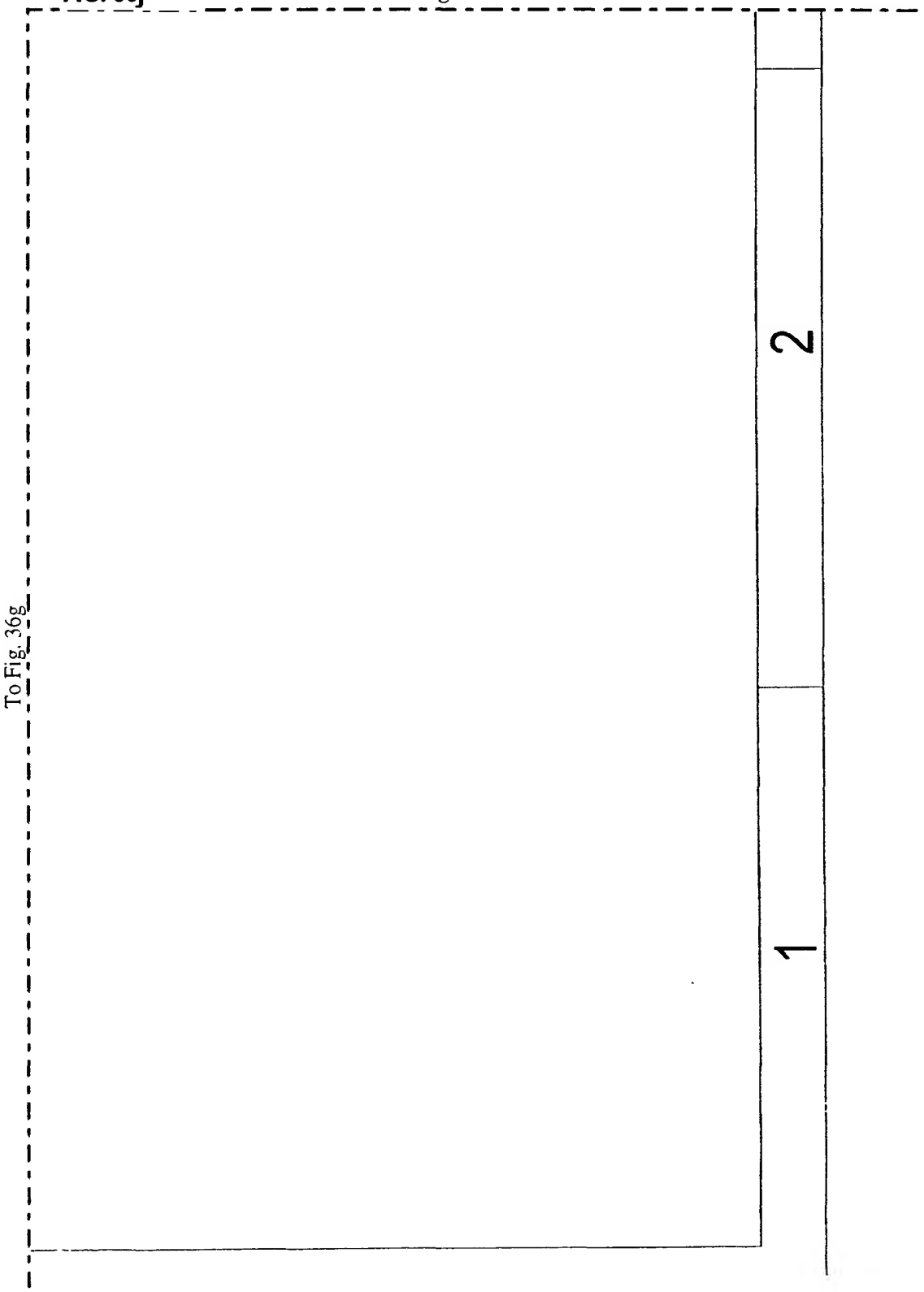
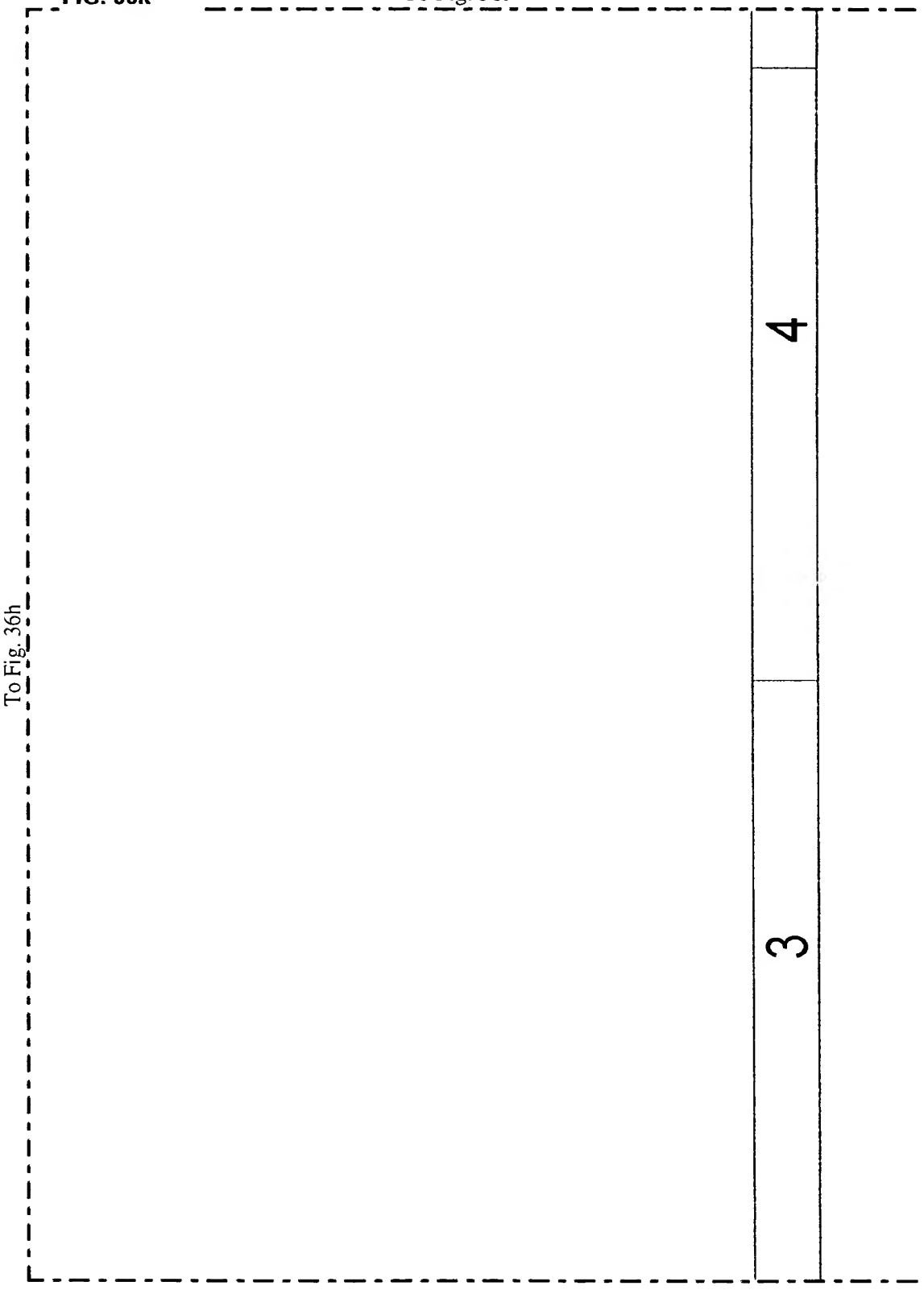


FIG. 36k

To Fig. 36l



To Fig. 36h

To Fig. 36j

FIG. 36l

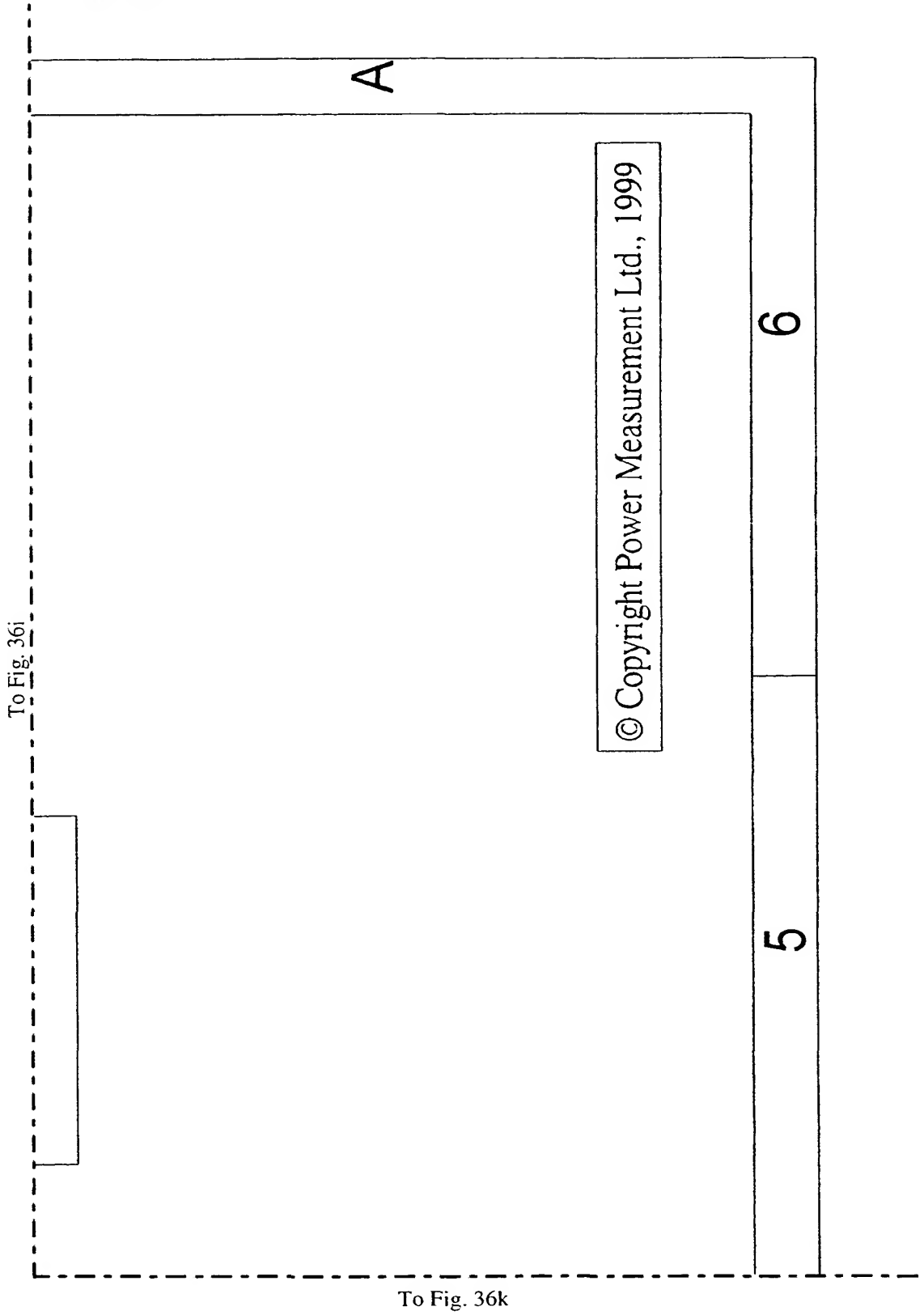

A
6
5
© Copyright Power Measurement Ltd., 1999
To Fig. 36i
To Fig. 36k

FIG. 37a

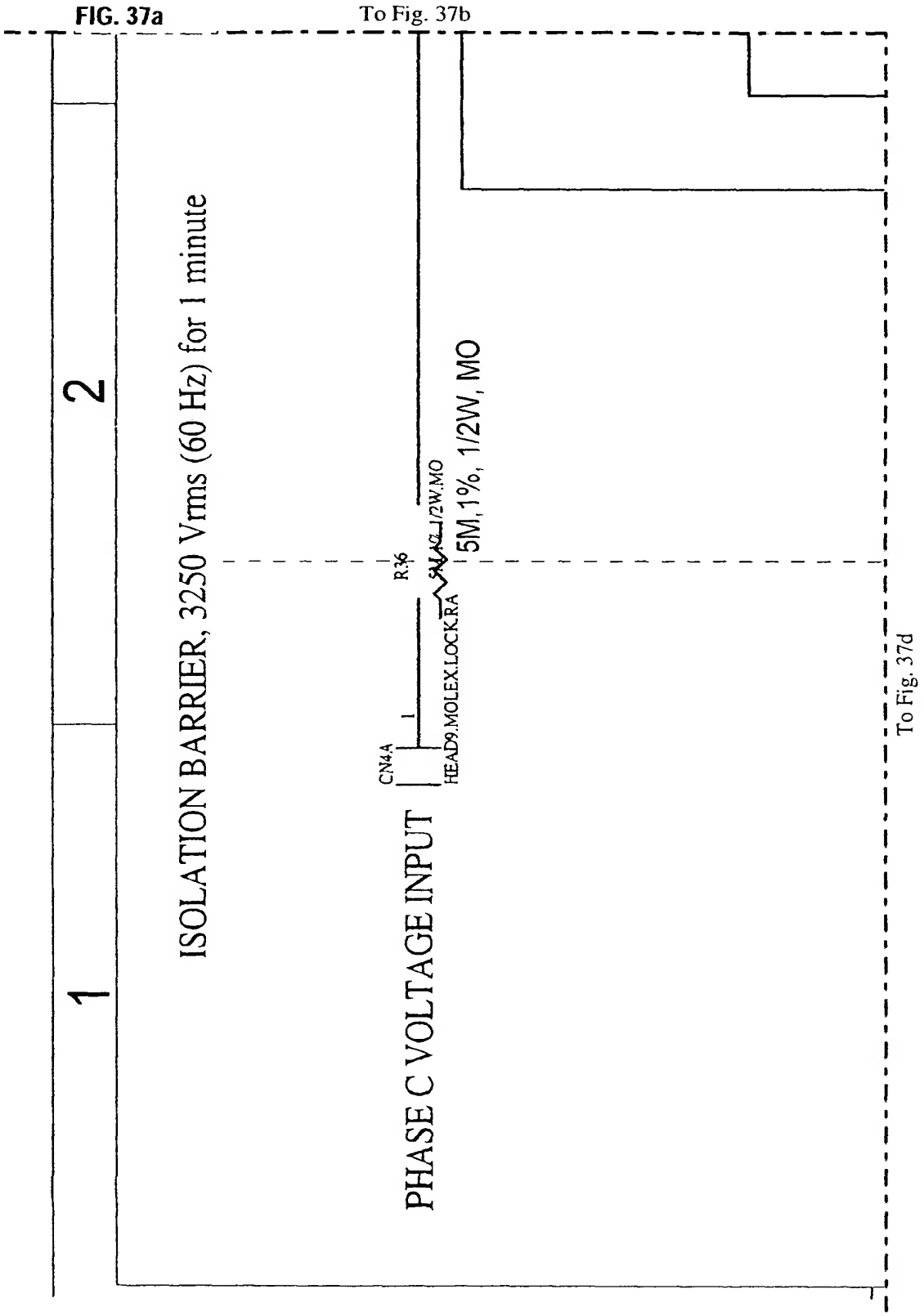

To Fig. 37b
2
1
ISOLATION BARRIER, 3250 Vrms (60 Hz) for 1 minute
PHASE C VOLTAGE INPUT
CN4A
1
HEAD9.MOLEX.LOCK.RA
R36
5M,1%, 1/2W, MO
To Fig. 37d

FIG. 37b

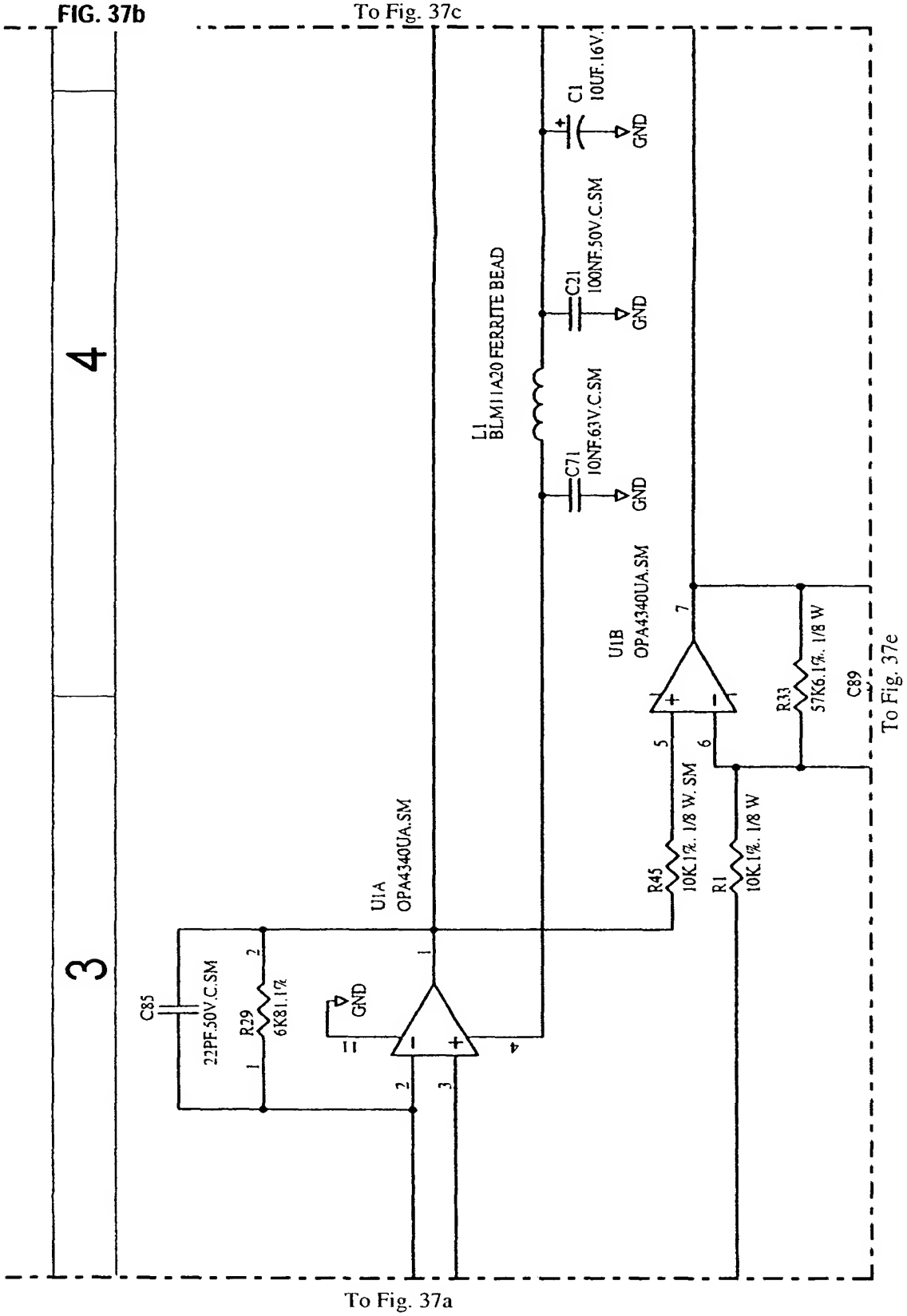

To Fig. 37c
4
3
C1
10UF.16V
GND
C21
100NF.50V.C.SM
GND
L1
BLM11A20 FERRITE BEAD
C71
10NF.63V.C.SM
GND
U1B
OPA4340UA.SM
U1A
OPA4340UA.SM
R45
10K.1%. 1/8 W. SM
R1
10K.1%. 1/8 W
R33
57K6.1%. 1/8 W
C89
C85
22PF.50V.C.SM
R29
6K81.1%
GND
To Fig. 37e
To Fig. 37a

FIG. 37c

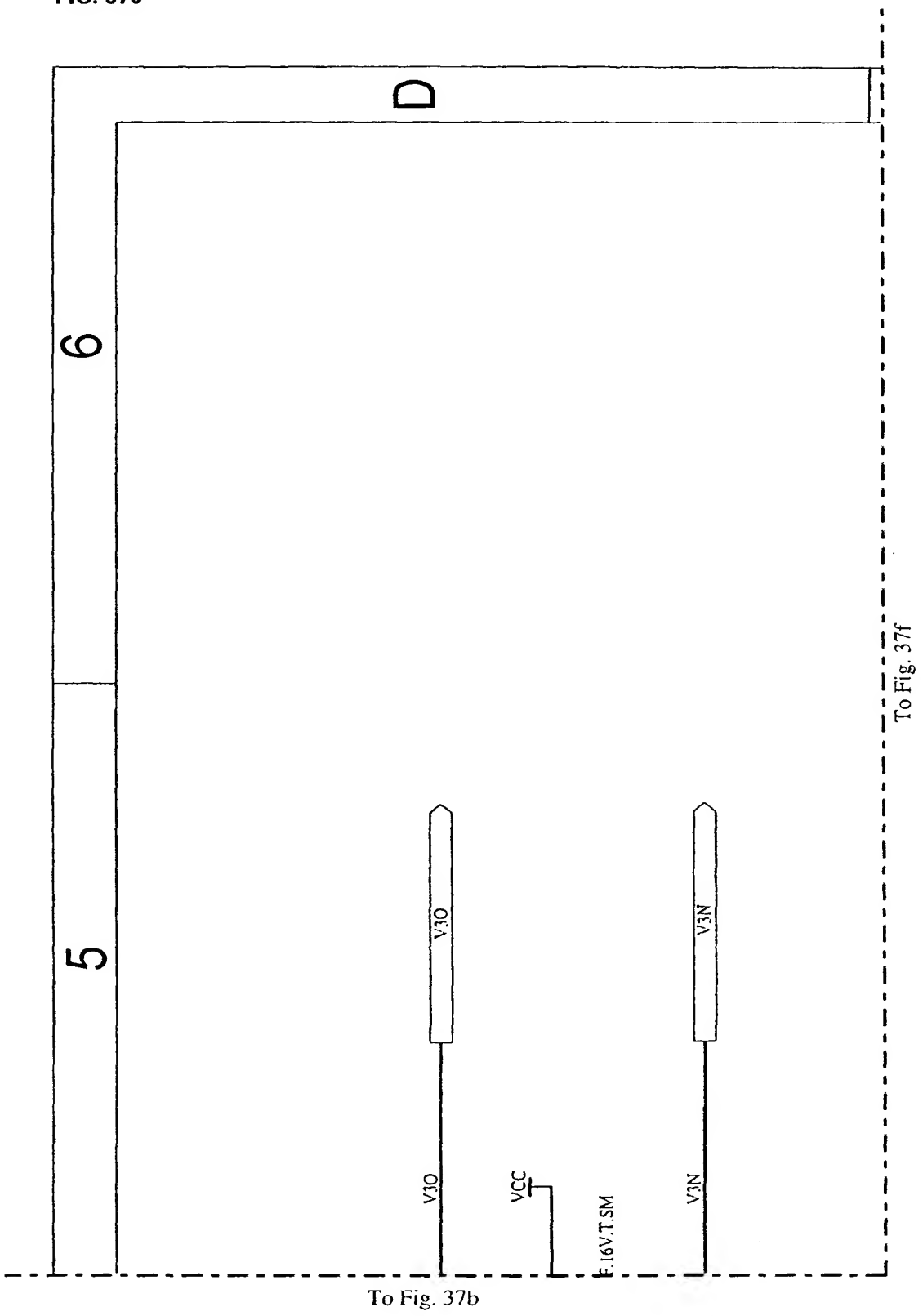


FIG. 37d

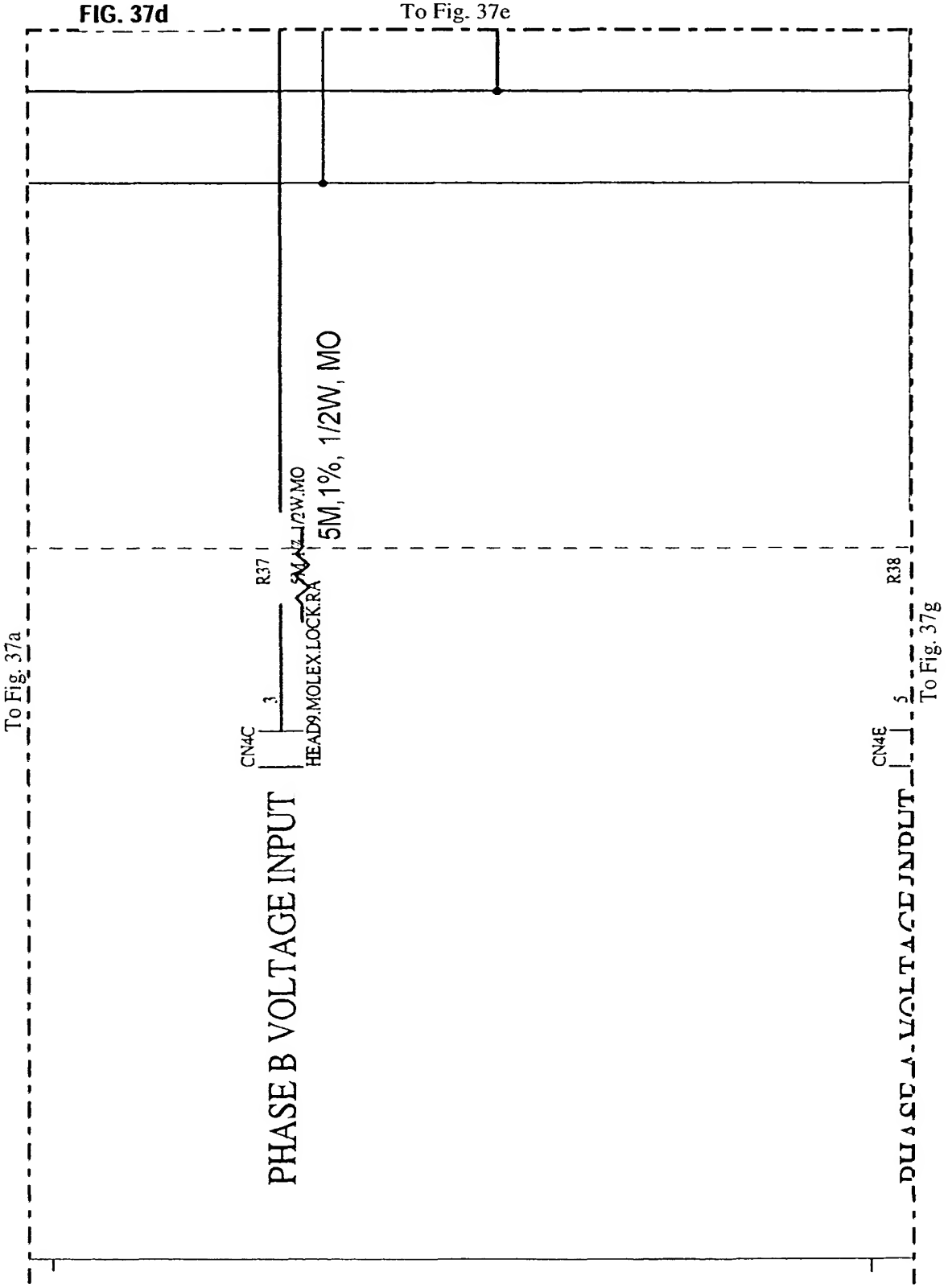

To Fig. 37e
To Fig. 37a
To Fig. 37g
R37
R38
5M, 1%, 1/2W, MO
5M, 1%, 1/2W, MO
HEAD9.MOLEX.LOCK.RA
CN4C
CN4E
3
5
PHASE B VOLTAGE INPUT

FIG. 37e

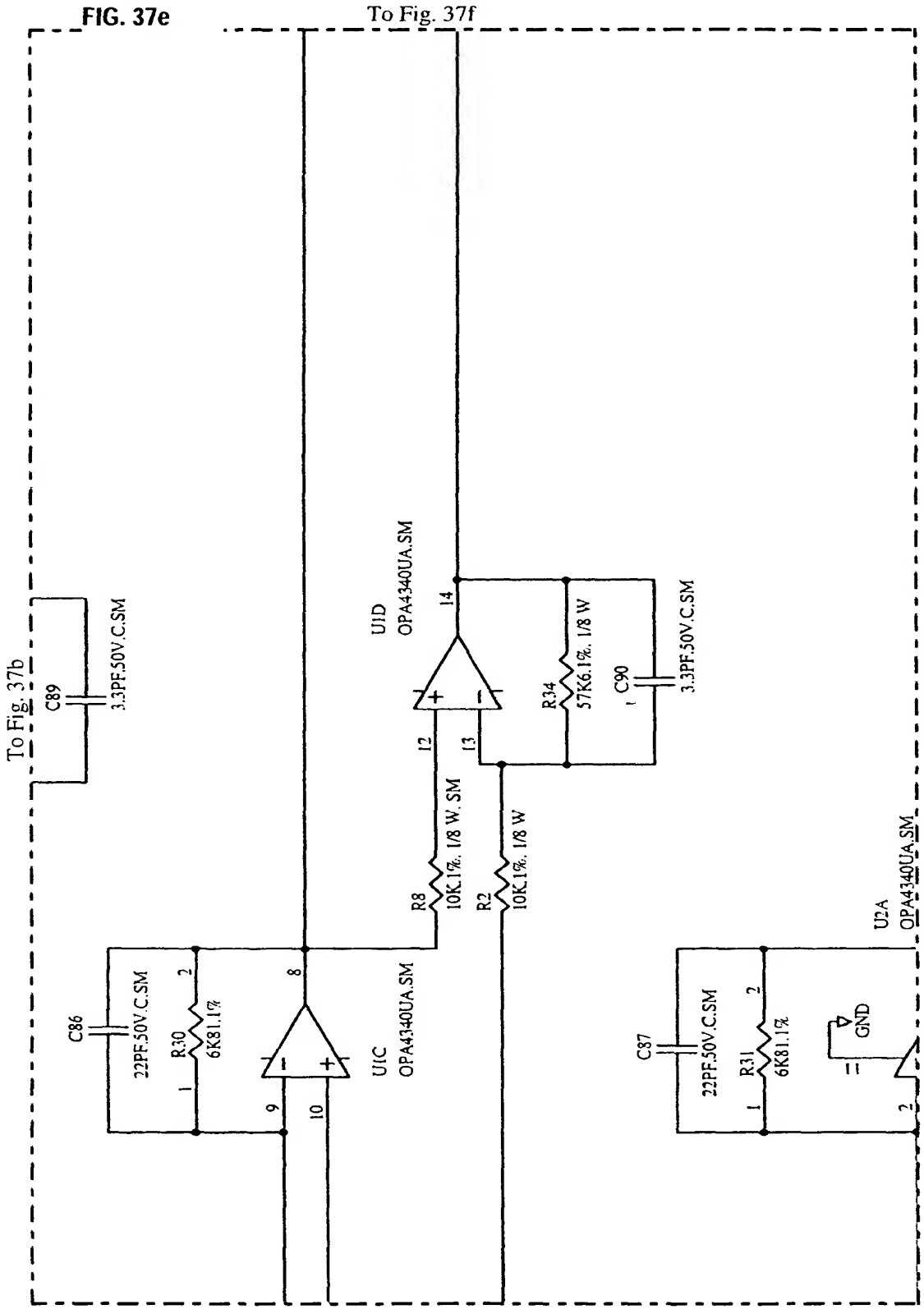

To Fig. 37f
To Fig. 37b
To Fig. 37h
To Fig. 37d
C89
3.3PF.50V.C.SM
U1D
OPA4340UA.SM
14
12
13
R34
57K6.1%. 1/8 W
C90
3.3PF.50V.C.SM
R8
10K.1%. 1/8 W.SM
R2
10K.1%. 1/8 W
C86
22PF.50V.C.SM
R30
6K81.1%
2
1
8
9
10
U1C
OPA4340UA.SM
U2A
OPA4340UA.SM
C87
22PF.50V.C.SM
R31
6K81.1%
GND

FIG. 37f

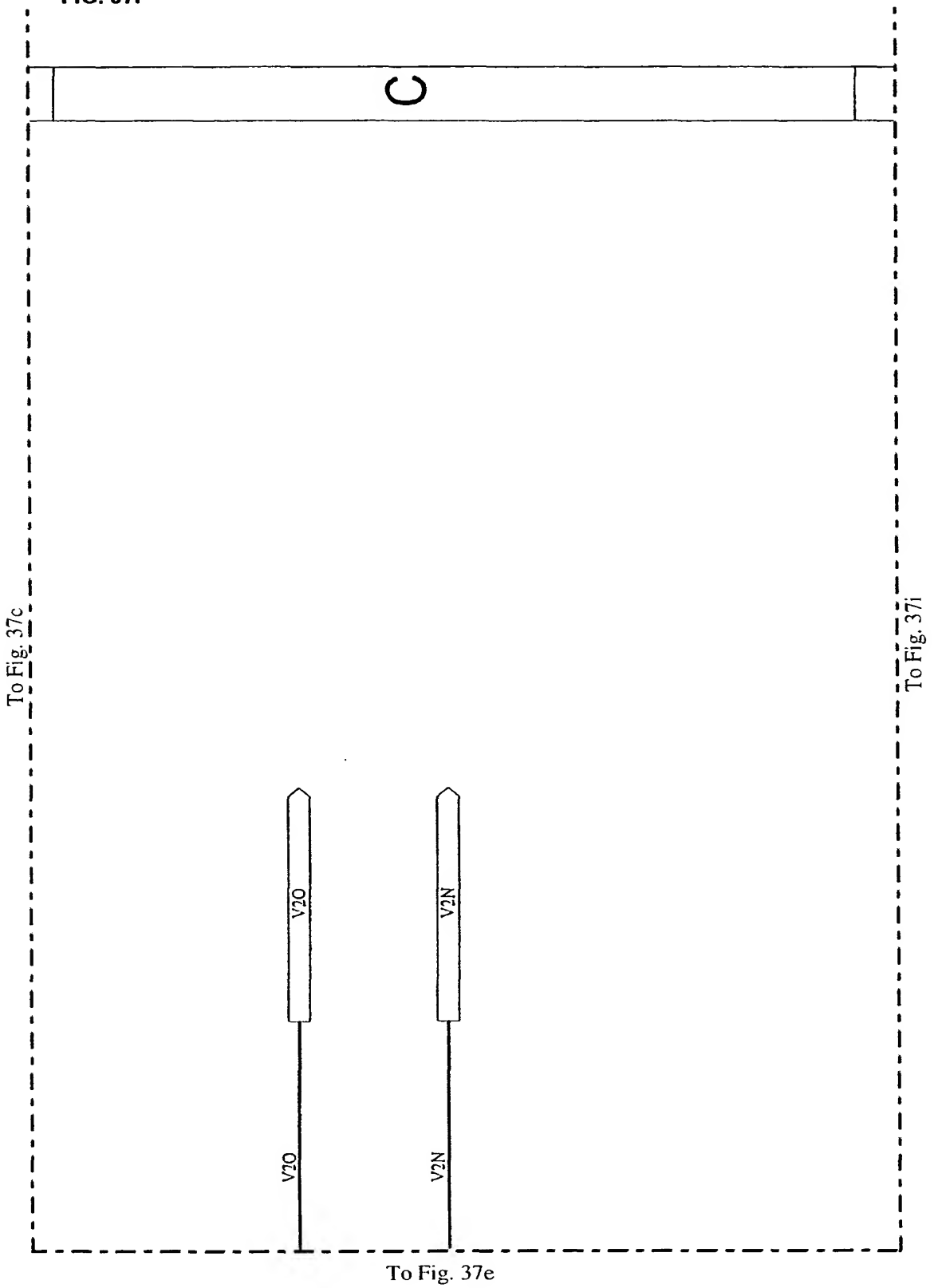


FIG. 37g

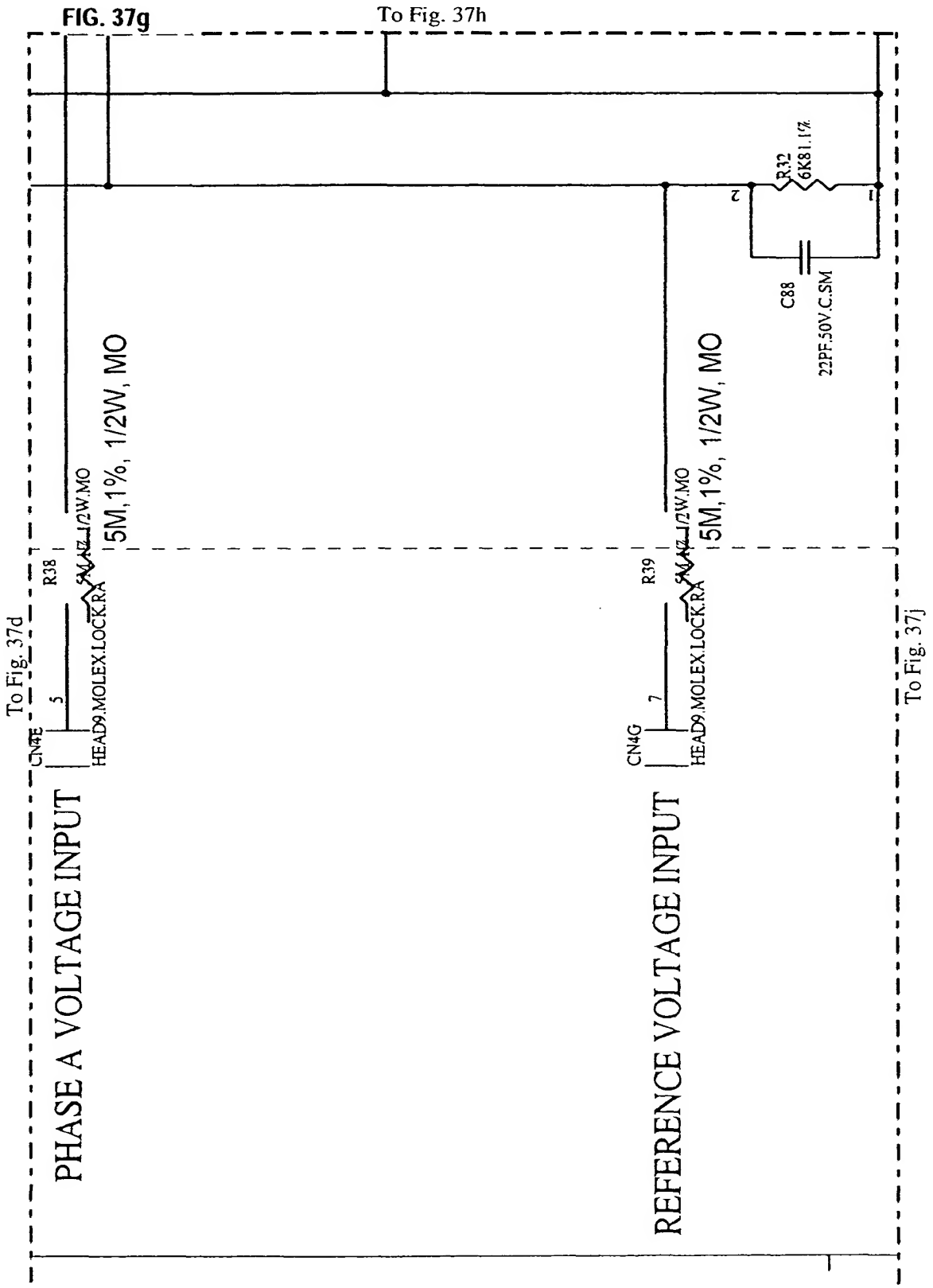

To Fig. 37h
To Fig. 37d
To Fig. 37j
PHASE A VOLTAGE INPUT
REFERENCE VOLTAGE INPUT
CN4E
CN4G
HEAD9.MOLEX.LOCK.RA
5
7
R38
R39
5M,1%, 1/2W, MO
R32
6K81.1%
C88
22PF.50V.C.SM

FIG. 37h

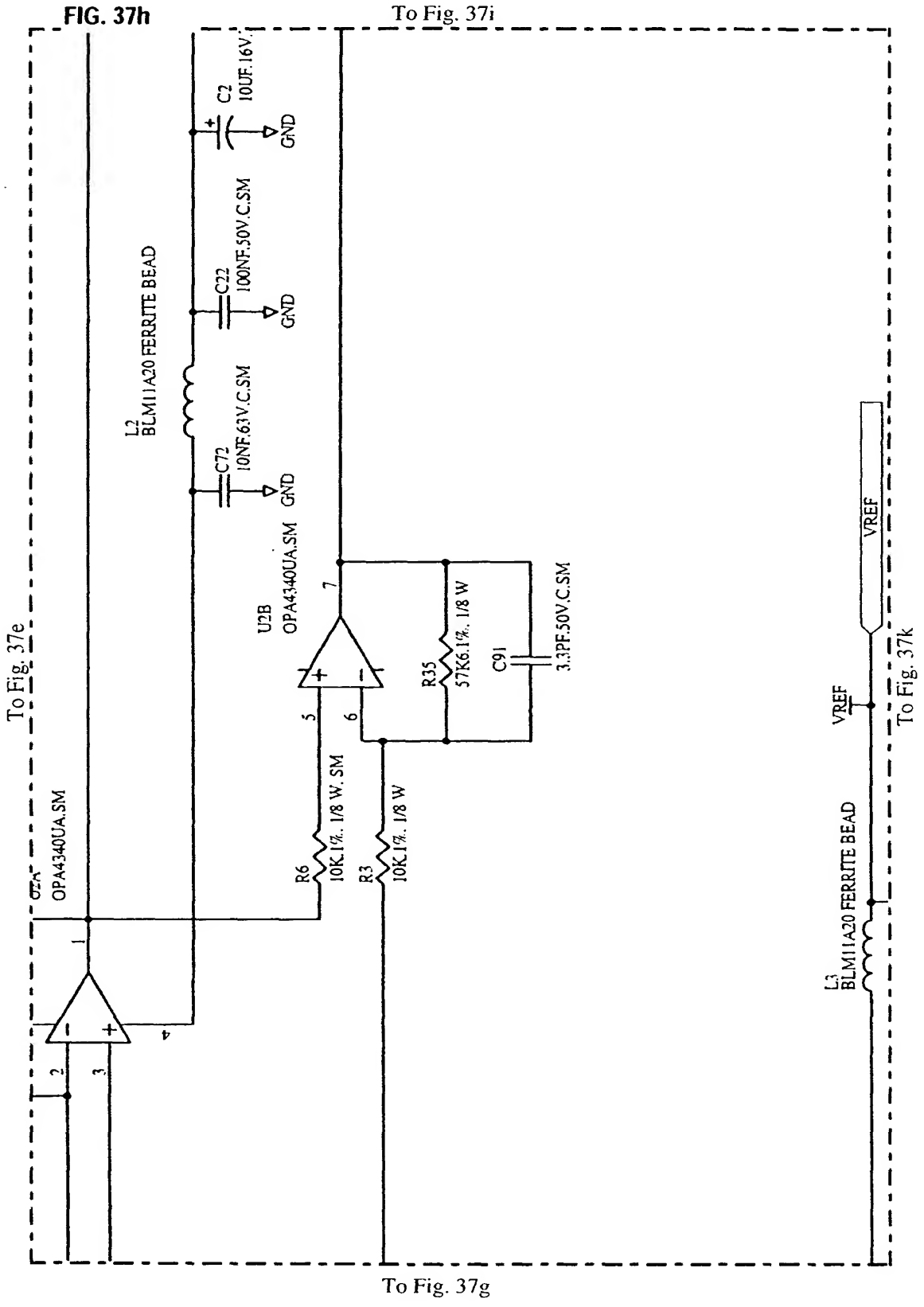

To Fig. 37i
To Fig. 37e
To Fig. 37k
To Fig. 37g
C2 10UF.16V.
GND
C22 100NF.50V.C.SM
L2 BLM11A20 FERRITE BEAD
C72 10NF.63V.C.SM
U2B OPA4340UA.SM
R35 57K6.1%. 1/8 W
C91 3.3PF.50V.C.SM
R6 10K.1%. 1/8 W. SM
R3 10K.1%. 1/8 W
VREF
L3 BLM11A20 FERRITE BEAD

FIG. 37i

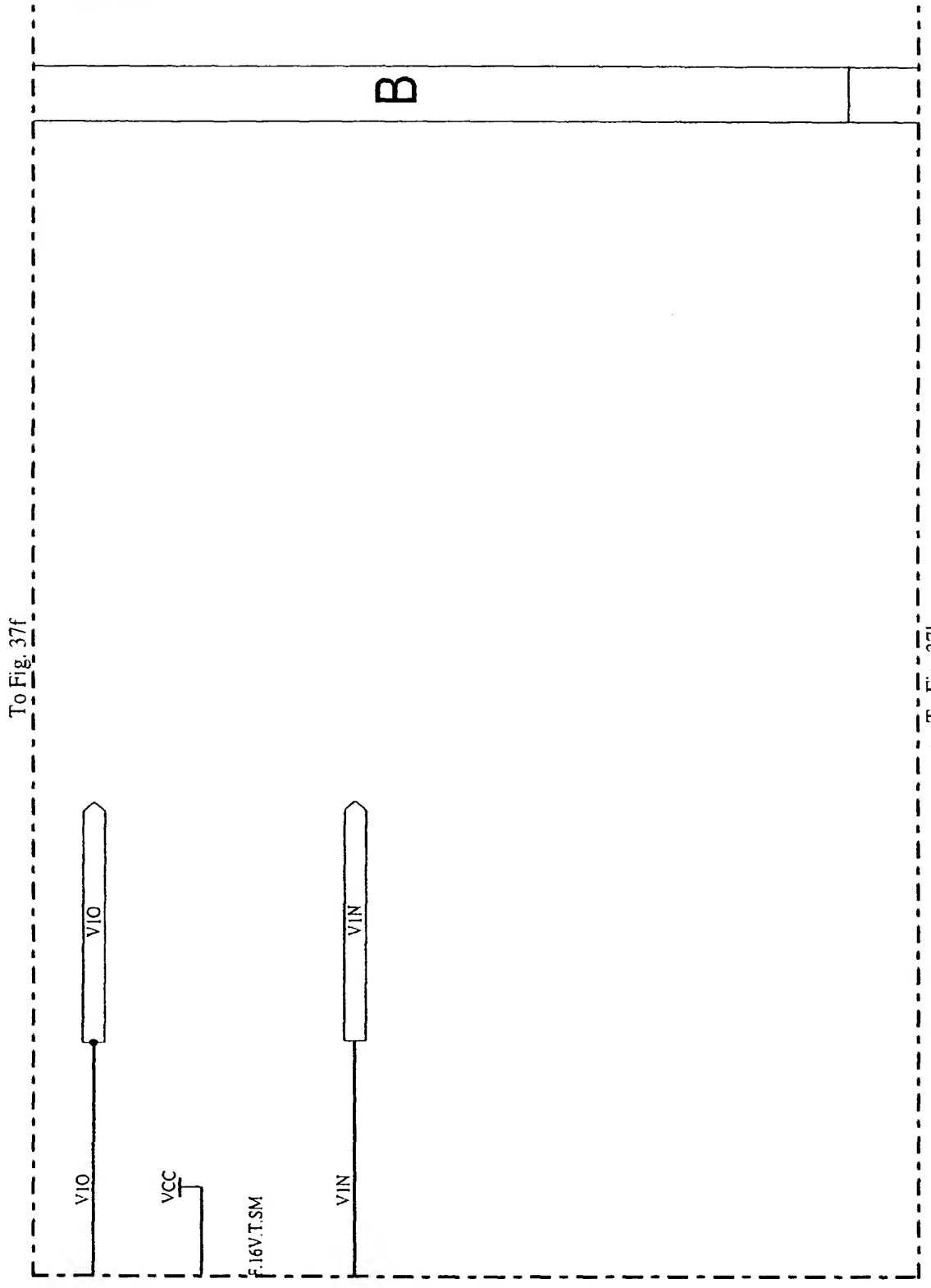


FIG. 37j

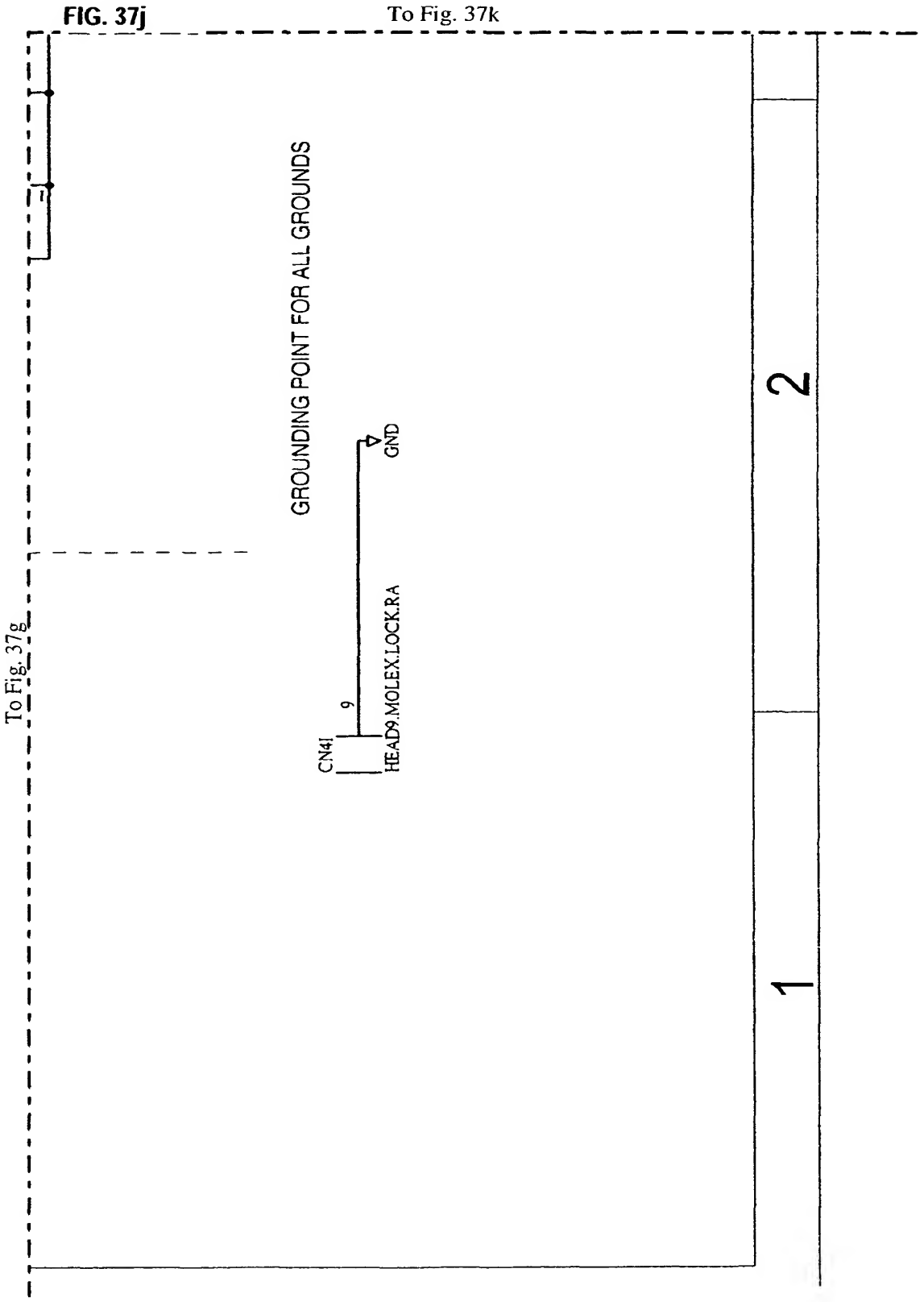
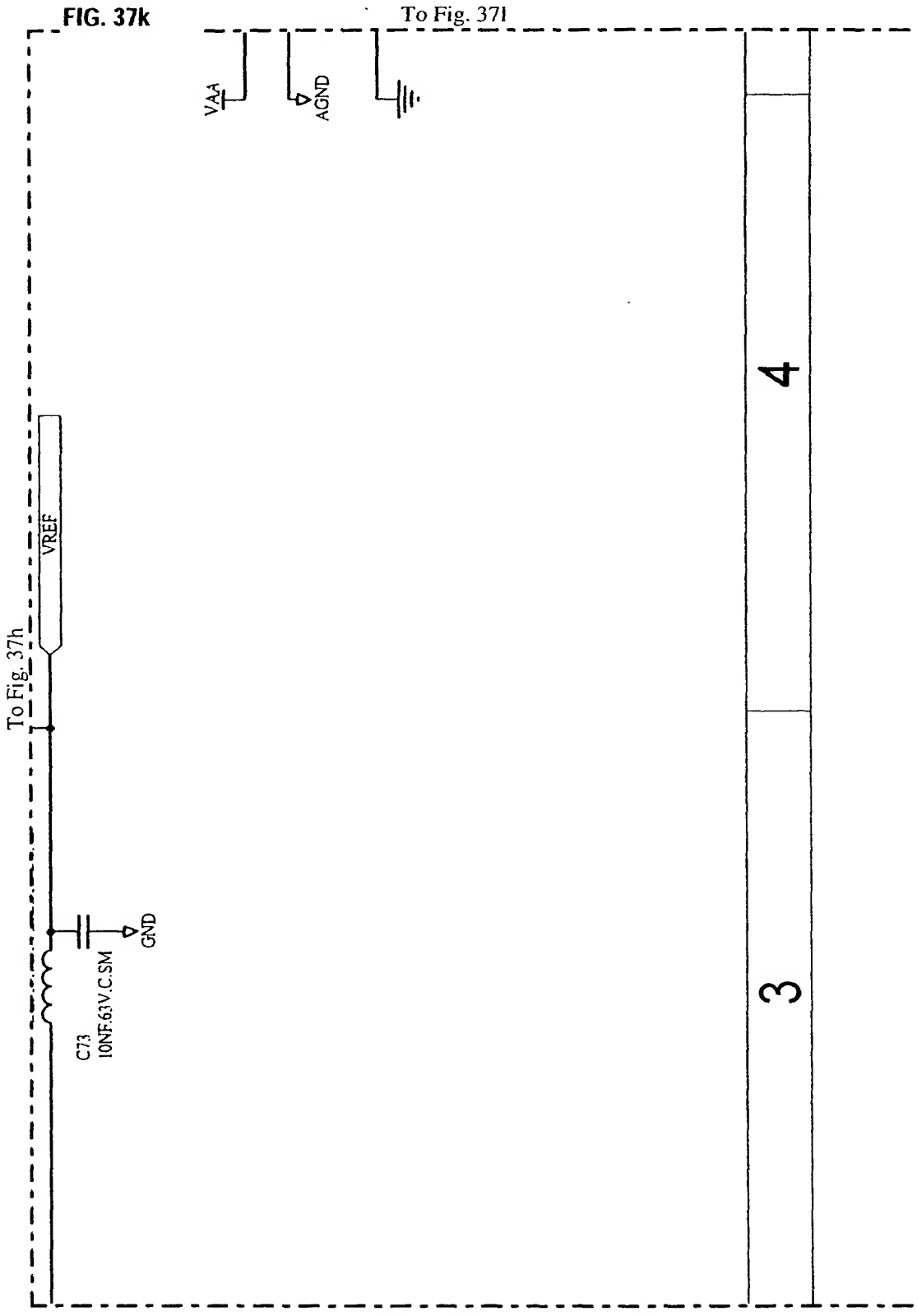

To Fig. 37k
GROUNDING POINT FOR ALL GROUNDS
GND
9
CN41
HEAD9.MOLEX.LOCK.RA
To Fig. 37g
2
1

FIG. 37k



To Fig. 37j

FIG. 37l

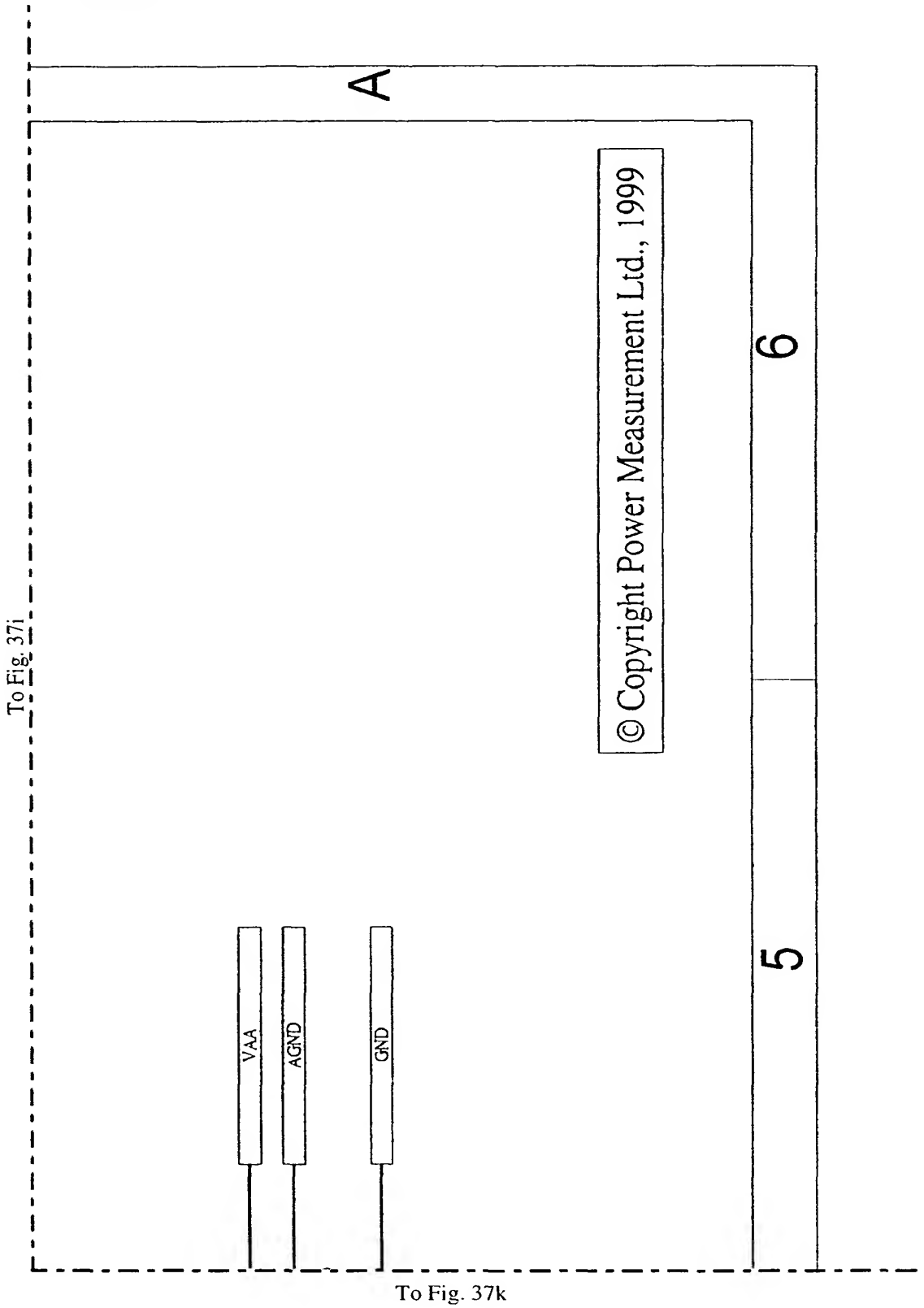

A
6
5
© Copyright Power Measurement Ltd., 1999
VAA
AGND
GND
To Fig. 37i
To Fig. 37k

FIG. 38a

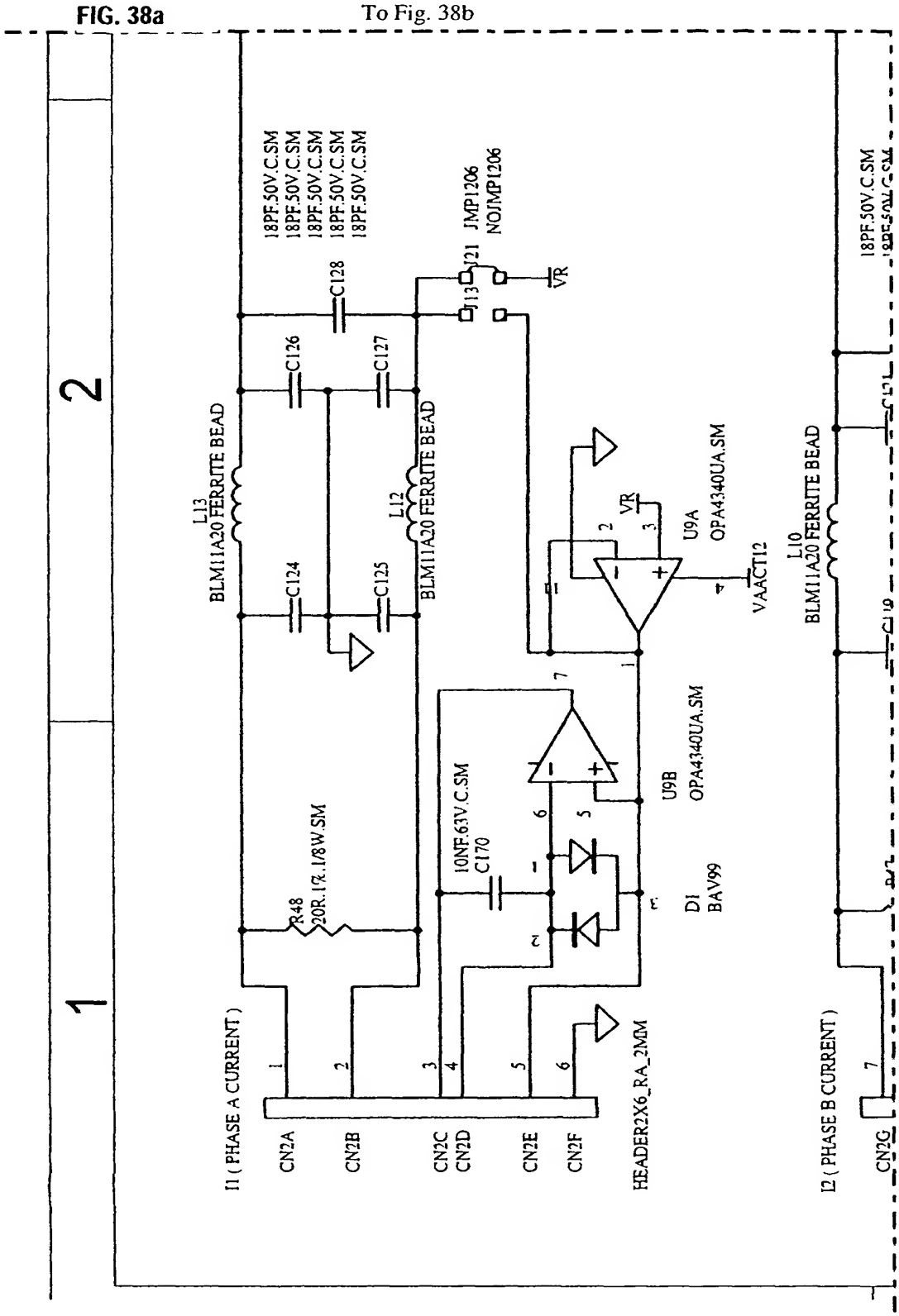
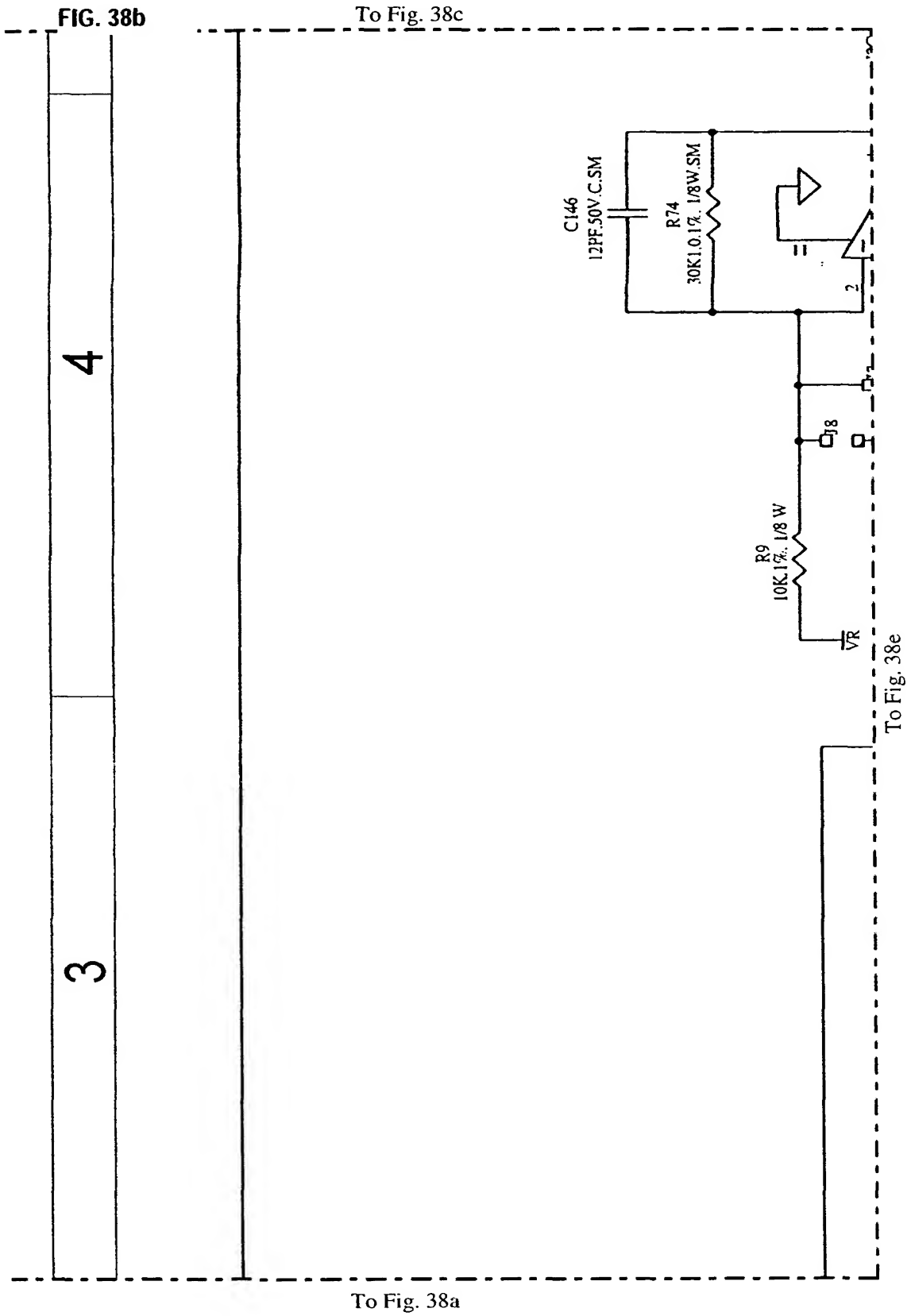
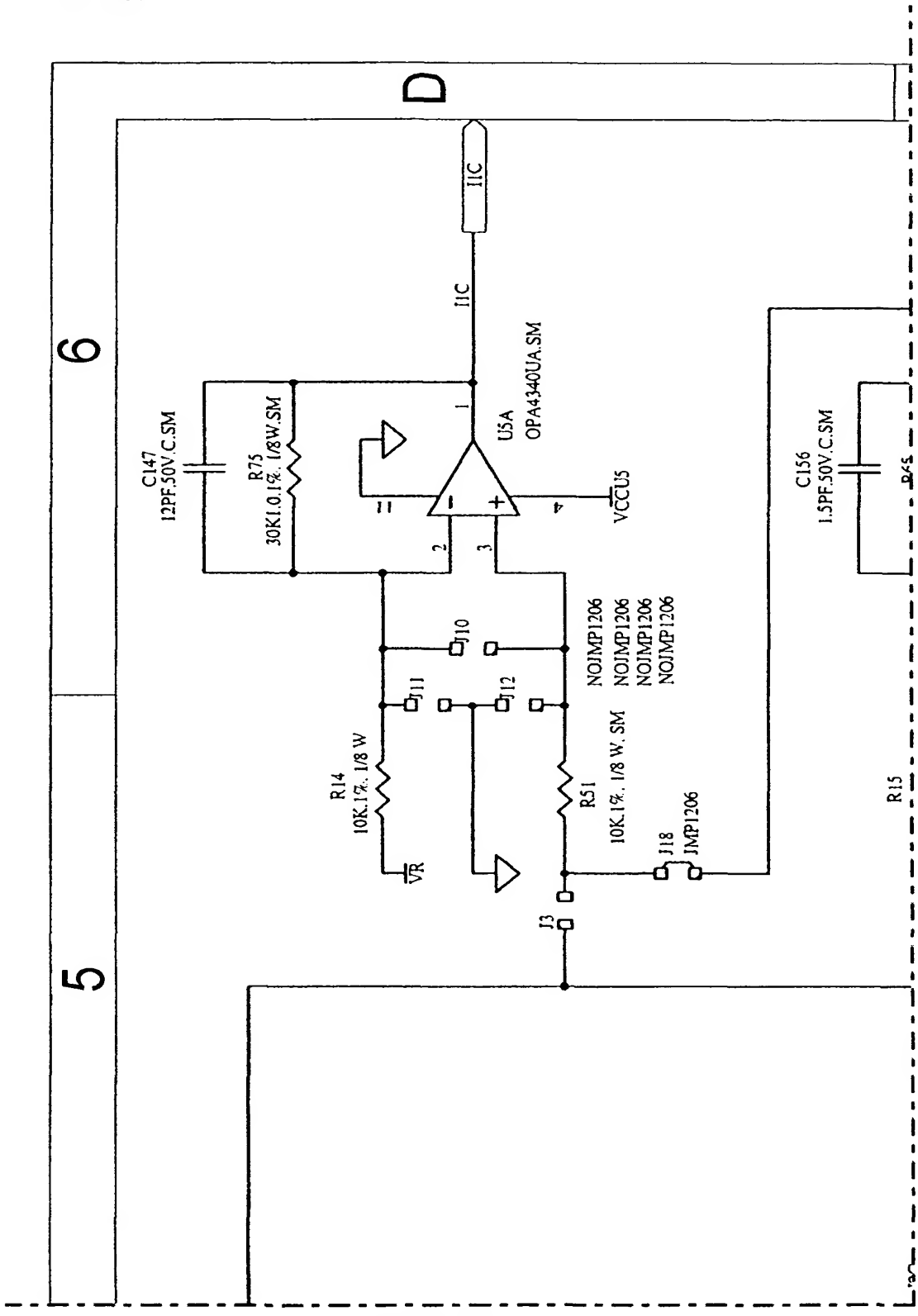

To Fig. 38b
2
1
18PF.50V.C.SM
C128
C126
C127
C124
C125
L13
BLM11A20 FERRITE BEAD
L12
BLM11A20 FERRITE BEAD
JMP1206
NO/MP1206
J21
J13
VR
U9A
OPA4340UA.SM
VAACT12
L10
BLM11A20 FERRITE BEAD
U9B
OPA4340UA.SM
10NF.63V.C.SM
C170
R48
20R.1%.1/8W.SM
D1
BAV99
I1 (PHASE A CURRENT)
I2 (PHASE B CURRENT)
CN2A
CN2B
CN2C
CN2D
CN2E
CN2F
CN2G
HEADER2X6_RA_2MM
To Fig. 38d

FIG. 38b



To Fig. 38a

FIG. 38c



To Fig. 38b

FIG. 38d

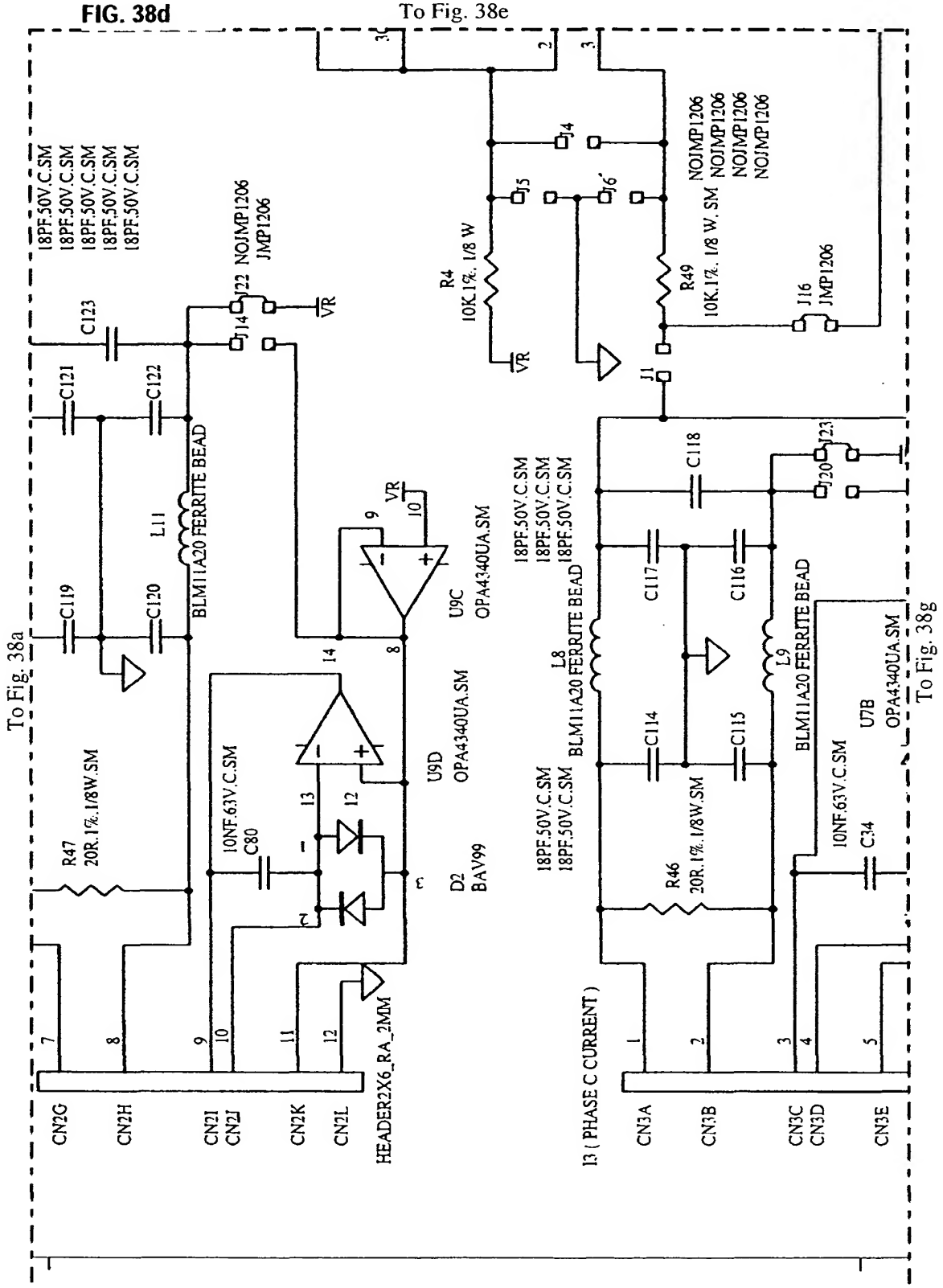

To Fig. 38e
To Fig. 38a
To Fig. 38g
18PF.50V.C.SM
C123
C121
C122
L11
BLM11A20 FERRITE BEAD
C119
C120
R47
20R.1%.1/8W.SM
10NF.63V.C.SM
C80
J14
J22 NOJMP1206
JMP1206
VR
R4
10K.1%. 1/8 W
J4
J5
J6
R49
10K.1%. 1/8 W. SM
NOJMP1206
J16
J1
C118
J20
J23
U9C
OPA4340UA.SM
U9D
OPA4340UA.SM
D2
BAV99
L8
L9
C117
C116
C114
C115
R46
20R.1%.1/8W.SM
U7B
OPA4340UA.SM
C34
HEADER2X6_RA_2MM
CN2G
CN2H
CN2I
CN2J
CN2K
CN2L
I3 (PHASE C CURRENT)
CN3A
CN3B
CN3C
CN3D
CN3E

FIG. 38e

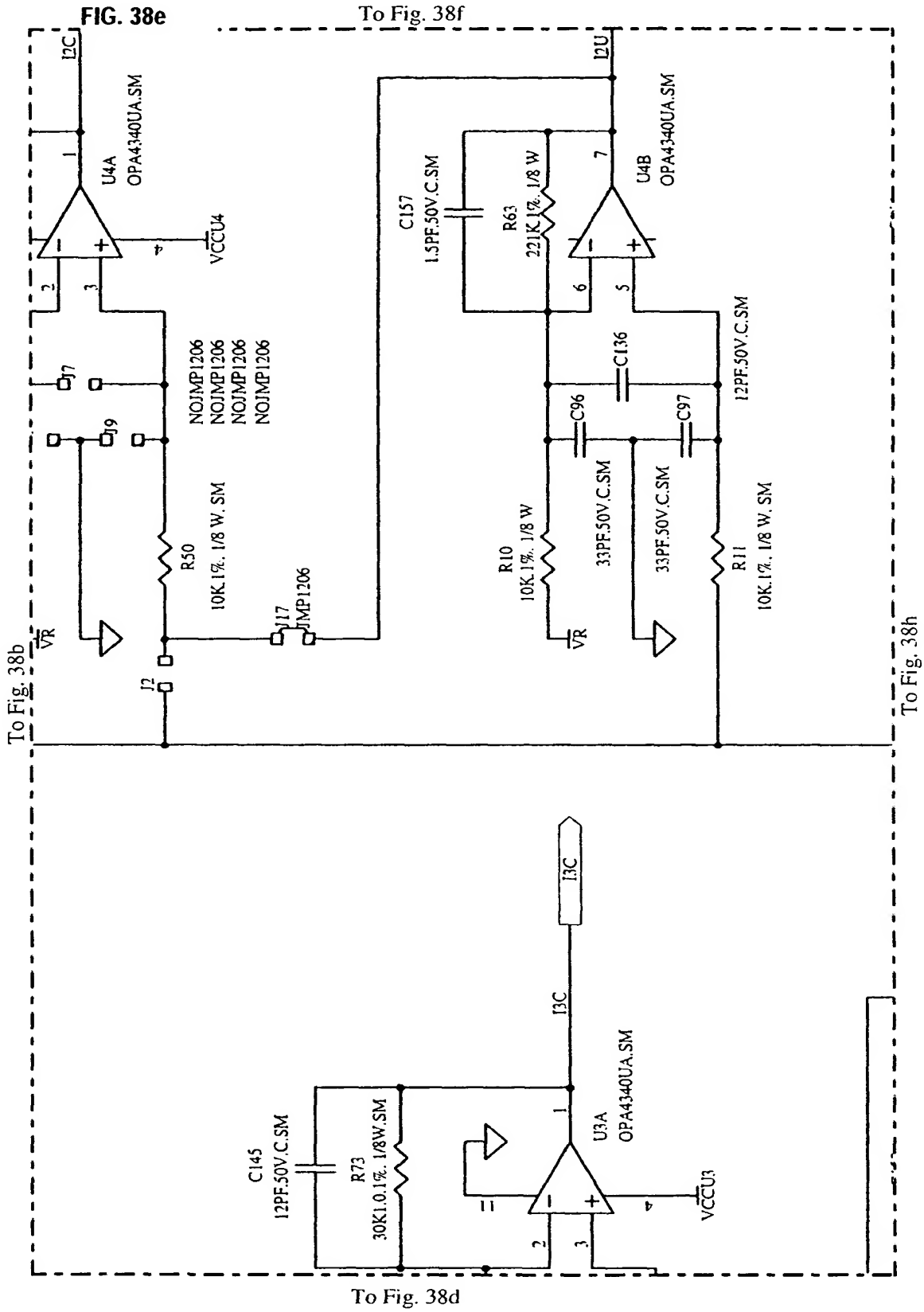
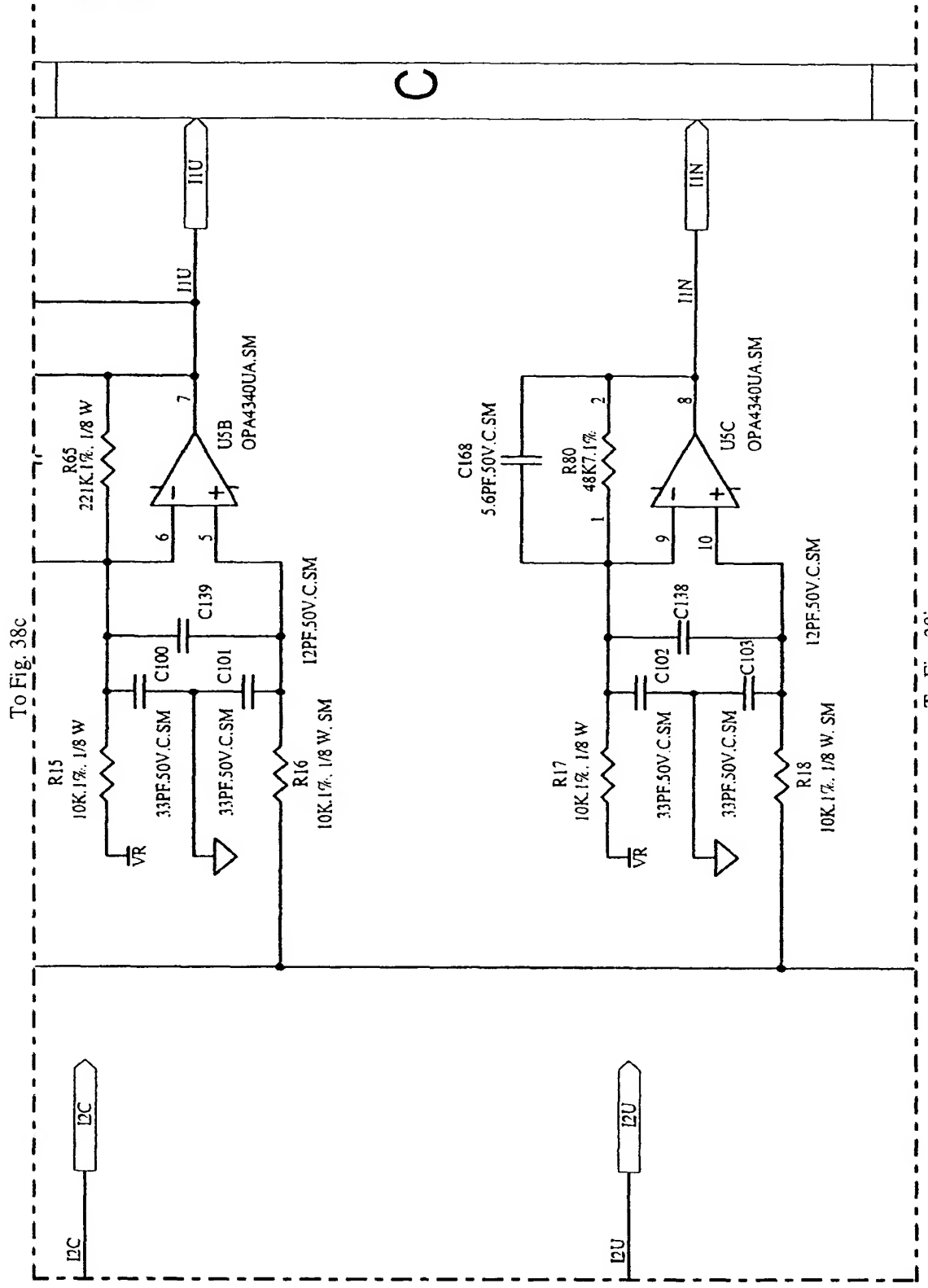

To Fig. 38f
I2C
U4A
OPA4340UA.SM
VCCU4
I2U
U4B
OPA4340UA.SM
C157
1.5PF.50V.C.SM
R63
221K.1%. 1/8 W
C136
12PF.50V.C.SM
C96
C97
33PF.50V.C.SM
33PF.50V.C.SM
J7
J9
NOJMP1206
NOJMP1206
NOJMP1206
NOJMP1206
R50
10K.1%. 1/8 W. SM
J17
JMP1206
J2
R10
10K.1%. 1/8 W
R11
10K.1%. 1/8 W. SM
VR
VR
To Fig. 38b
To Fig. 38h
I3C
I3C
U3A
OPA4340UA.SM
VCCU3
C145
12PF.50V.C.SM
R73
30K1.0.1%. 1/8W.SM
To Fig. 38d

FIG. 38f



To Fig. 38e

FIG. 38g

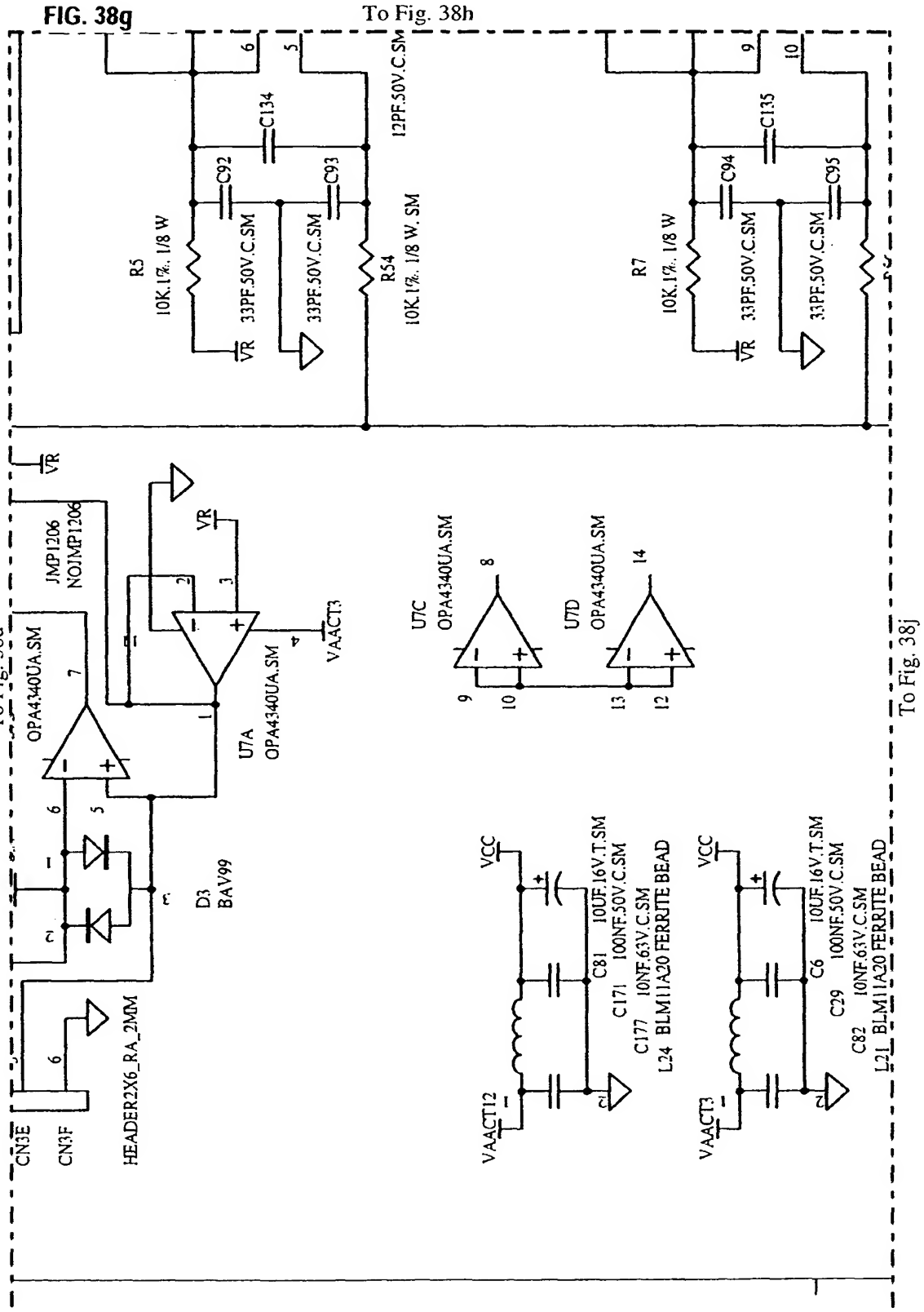

To Fig. 38h
To Fig. 38d
To Fig. 38j
R5
10K.1%. 1/8 W
33PF.50V.C.SM
C92
C93
C134
12PF.50V.C.SM
R54
10K.1%. 1/8 W. SM
R7
C94
C95
C135
VR
JMP1206
NO1MP1206
OPA4340UA.SM
U7A
U7C
U7D
VAACT3
D3
BAV99
CN3E
CN3F
HEADER2X6_RA_2MM
VCC
VAACT12
C81 10UF.16V.T.SM
C171 100NF.50V.C.SM
C177 10NF.63V.C.SM
L24 BLM11A20 FERRITE BEAD
C6 10UF.16V.T.SM
C29 100NF.50V.C.SM
C82 10NF.63V.C.SM
L21 BLM11A20 FERRITE BEAD

FIG. 38h

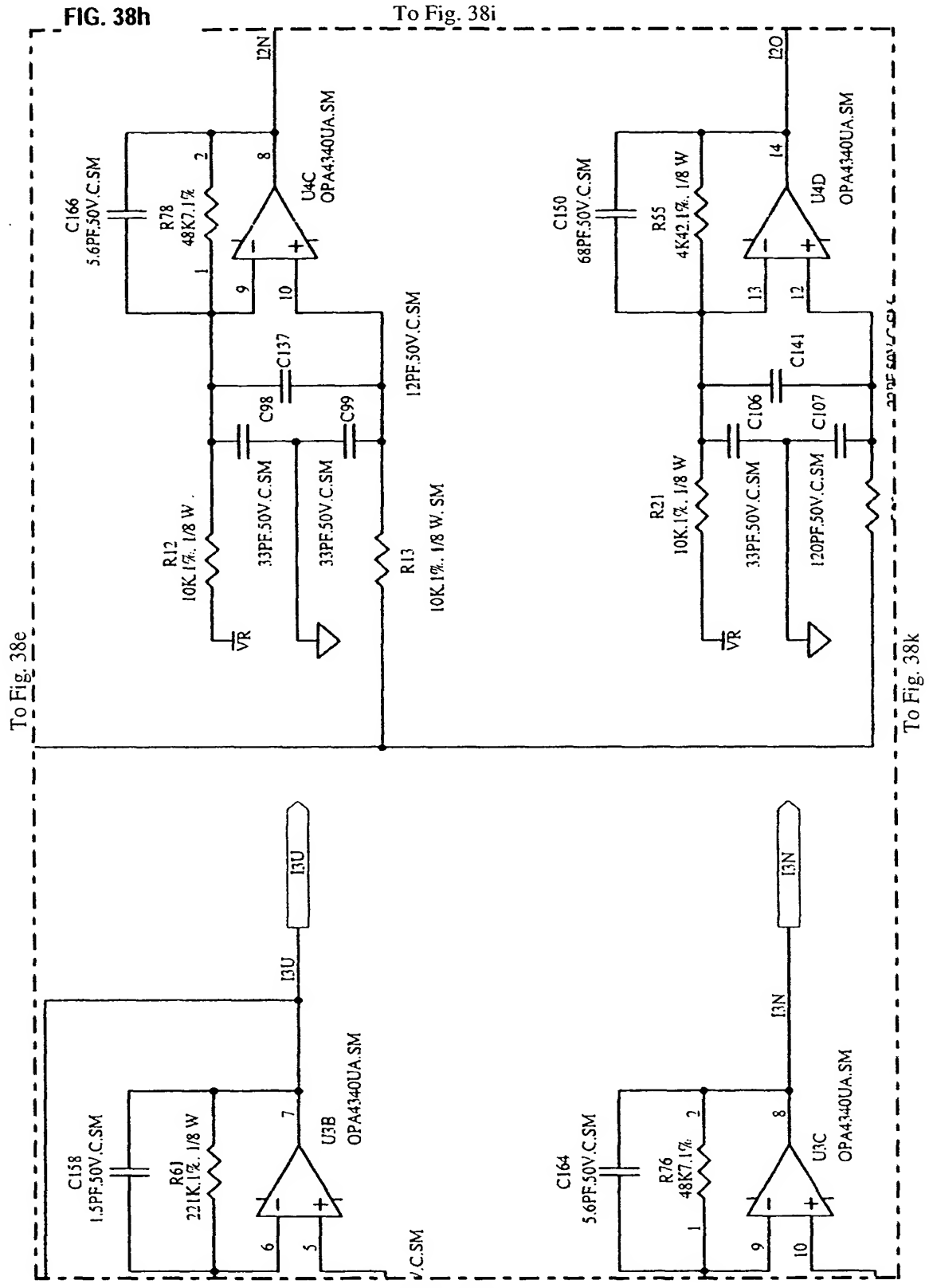
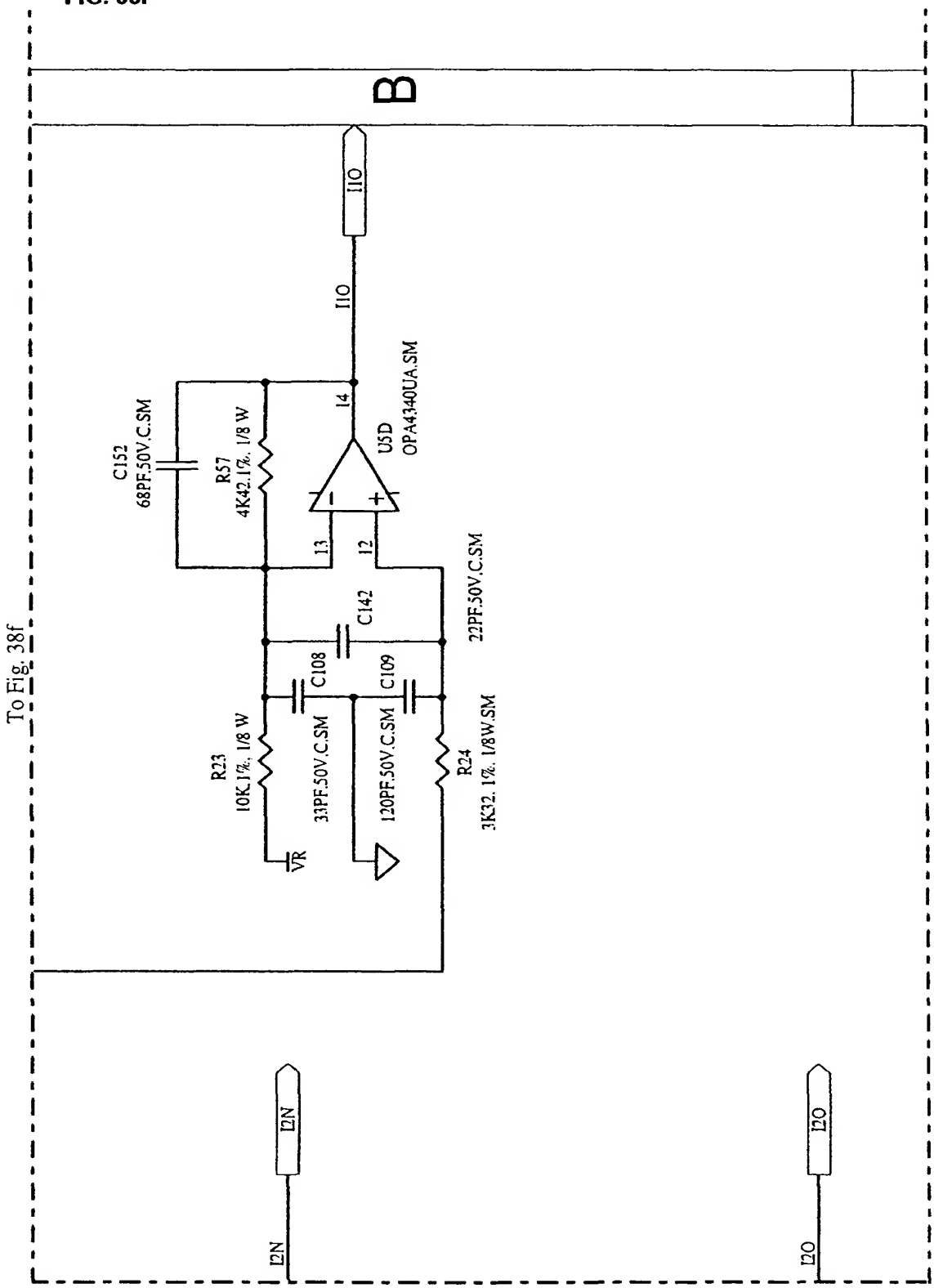

To Fig. 38i
To Fig. 38e
To Fig. 38k
To Fig. 38g
I2N
I2O
I3U
I3N
U4C OPA4340UA.SM
U4D OPA4340UA.SM
U3B OPA4340UA.SM
U3C OPA4340UA.SM
C166 5.6PF.50V.C.SM
R78 48K7.1%
C137
C98
C99
12PF.50V.C.SM
33PF.50V.C.SM
R12 10K.1%. 1/8 W
R13 10K.1%. 1/8 W. SM
VR
C150 68PF.50V.C.SM
R55 4K42.1%. 1/8 W
C141
C106
C107
R21 10K.1%. 1/8 W
120PF.50V.C.SM
C158 1.5PF.50V.C.SM
R61 221K.1%. 1/8 W
C164 5.6PF.50V.C.SM
R76 48K7.1%

FIG. 38i



To Fig. 38h

FIG. 38j

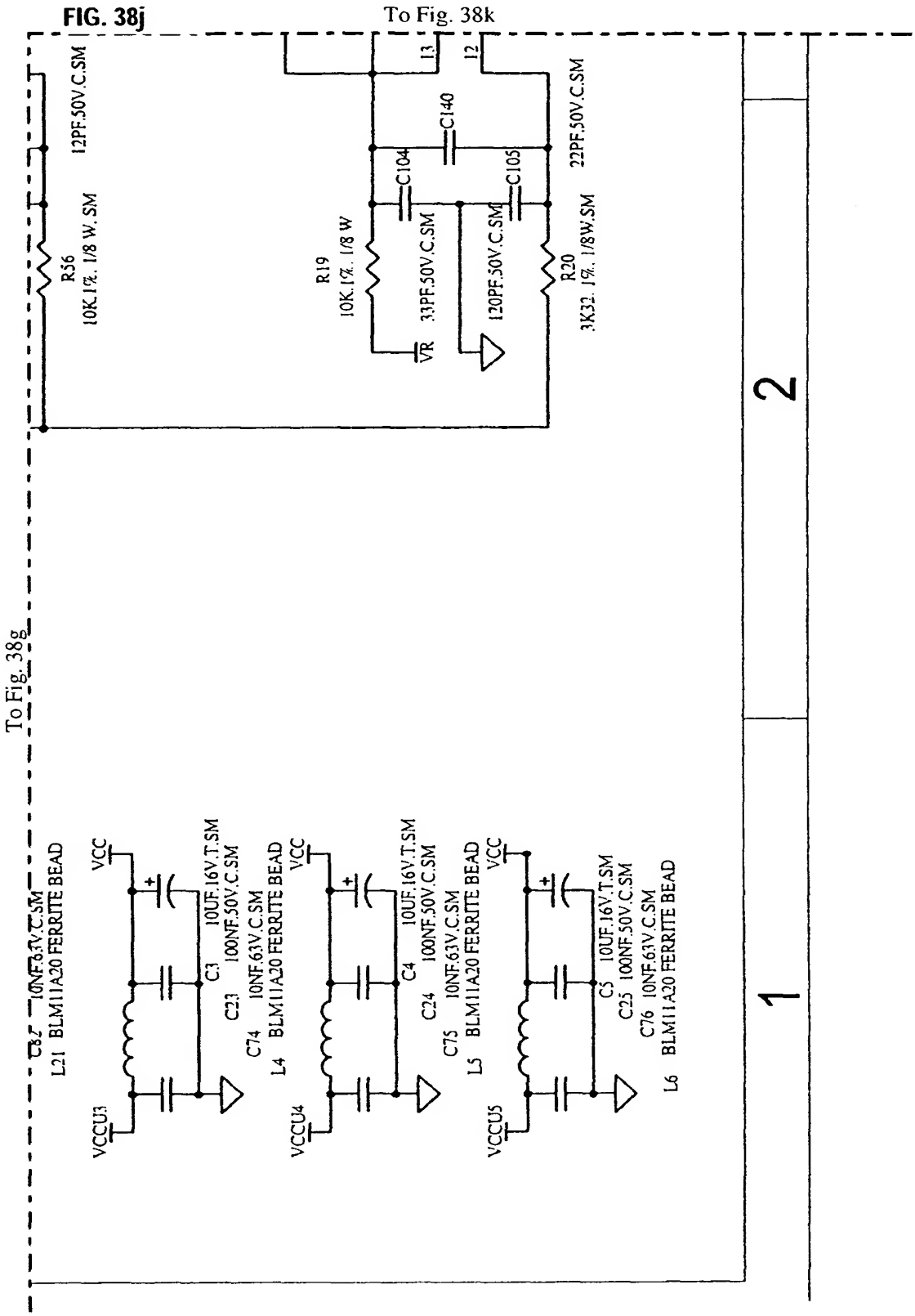

To Fig. 38k
To Fig. 38g
R36
10K.1%. 1/8 W. SM
12PF.50V.C.SM
R19
10K.1%. 1/8 W
C104
33PF.50V.C.SM
VR
C140
C105
120PF.50V.C.SM
R20
3K32. 1%. 1/8W.SM
22PF.50V.C.SM
I3
I2
2
1
VCC
VCCU3
C3 10UF.16V.T.SM
C23 100NF.50V.C.SM
C74 10NF.63V.C.SM
L4 BLM11A20 FERRITE BEAD
VCCU4
C4 10UF.16V.T.SM
C24 100NF.50V.C.SM
C75 10NF.63V.C.SM
L5 BLM11A20 FERRITE BEAD
VCCU5
C5 10UF.16V.T.SM
C25 100NF.50V.C.SM
C76 10NF.63V.C.SM
L6 BLM11A20 FERRITE BEAD
L21 BLM11A20 FERRITE BEAD

FIG. 38k

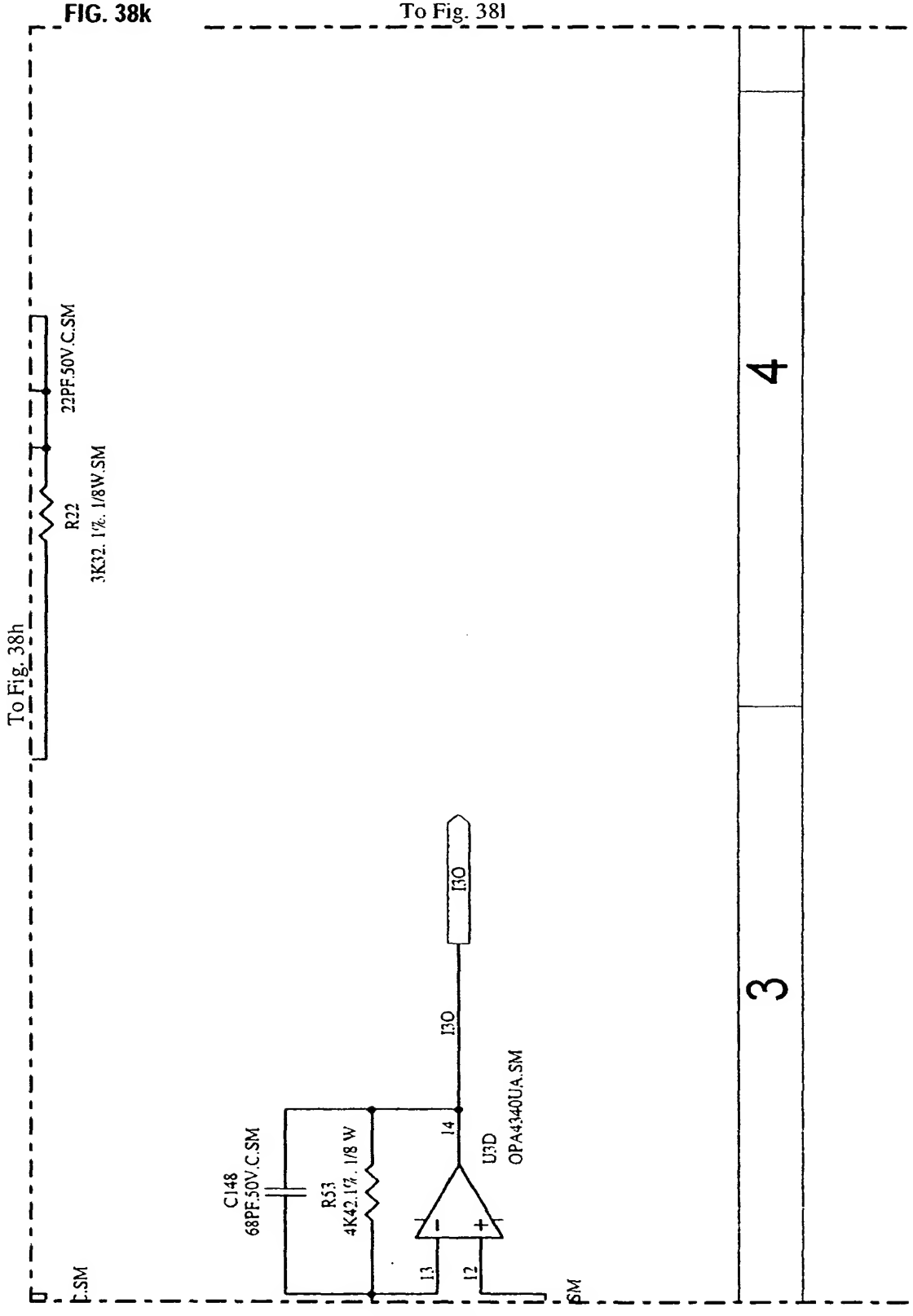

To Fig. 38l
To Fig. 38h
22PF.50V.C.SM
R22
3K32. 1%. 1/8W.SM
4
3
I30
I30
U3D
OPA4340UA.SM
14
C148
68PF.50V.C.SM
R53
4K42.1%. 1/8 W
13
12
To Fig. 38j

FIG. 38I

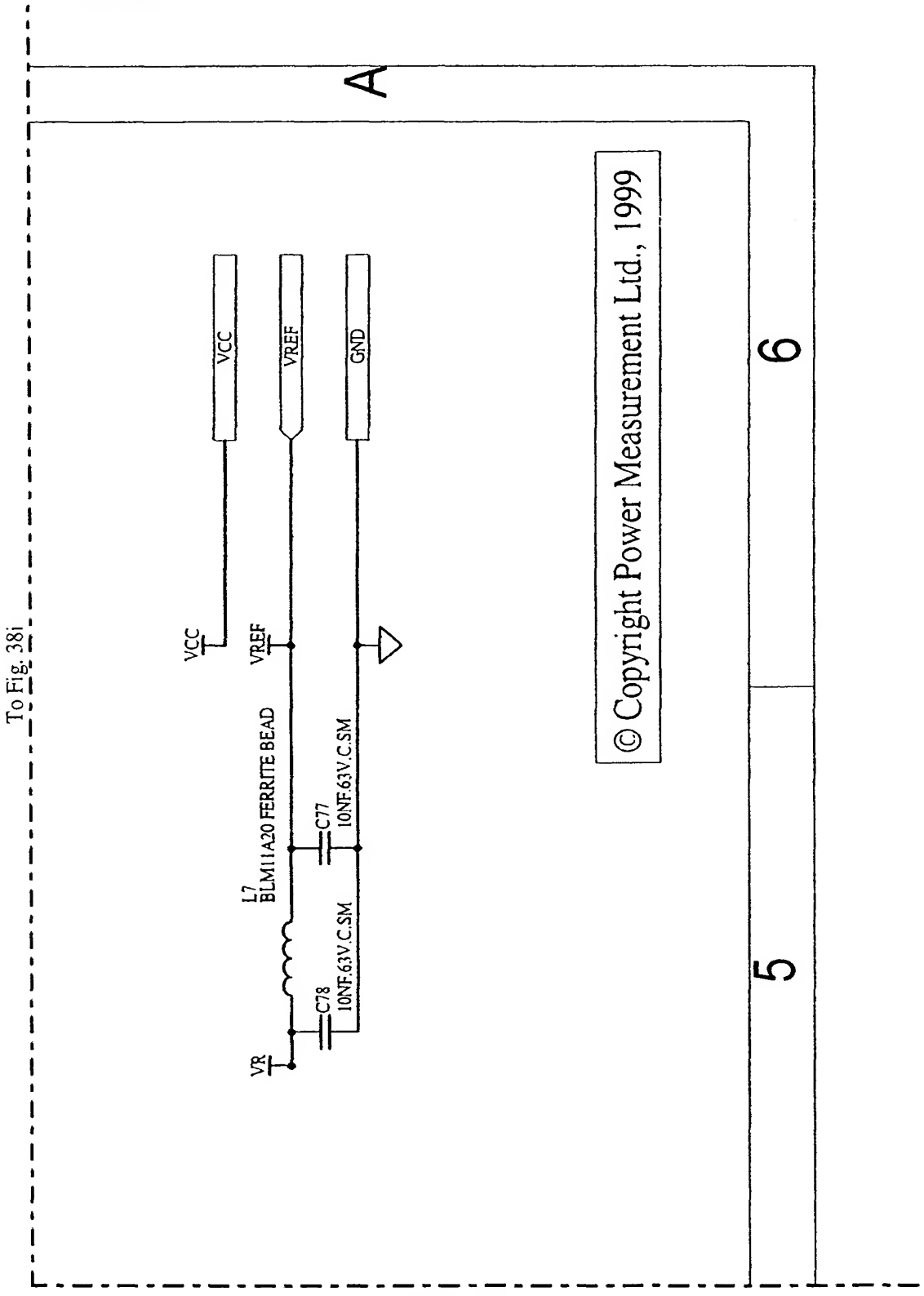

A
6
5
VCC
VREF
GND
VCC
VREF
L7
BLM11A20 FERRITE BEAD
C77
10NF.63V.C.SM
C78
10NF.63V.C.SM
VR
© Copyright Power Measurement Ltd., 1999
To Fig. 38i
To Fig. 38k

FIG. 39a

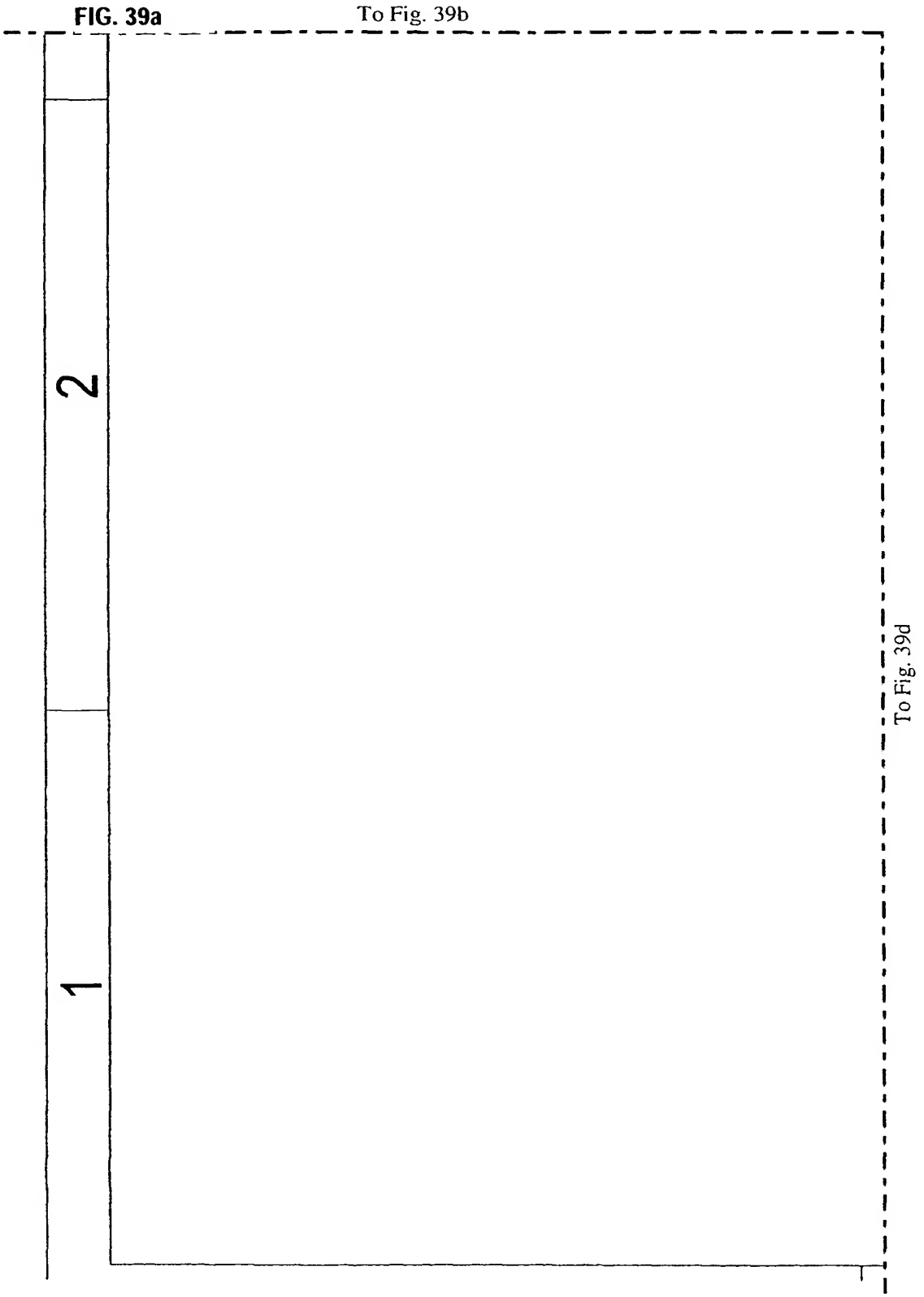


FIG. 39b

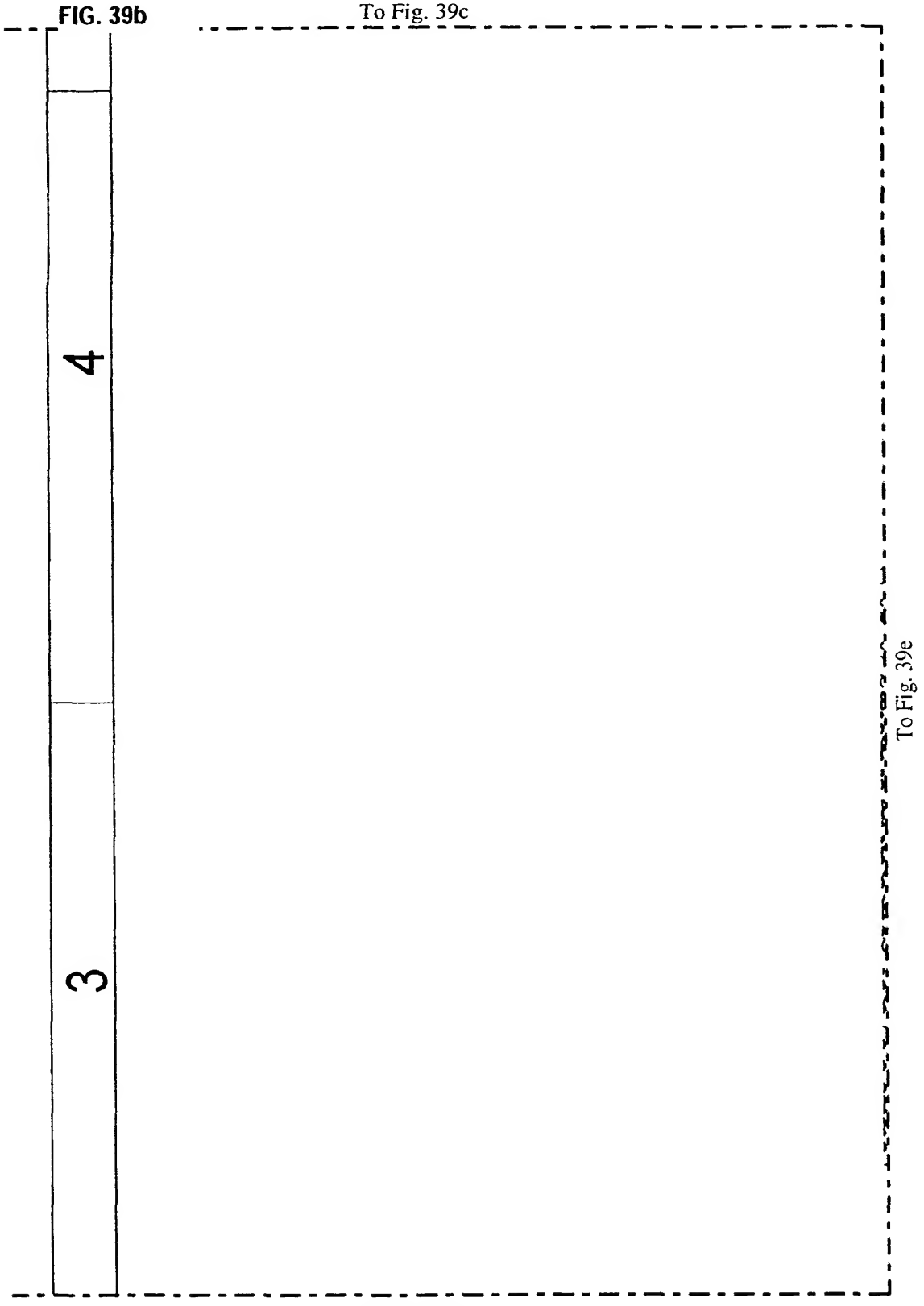


FIG. 39c

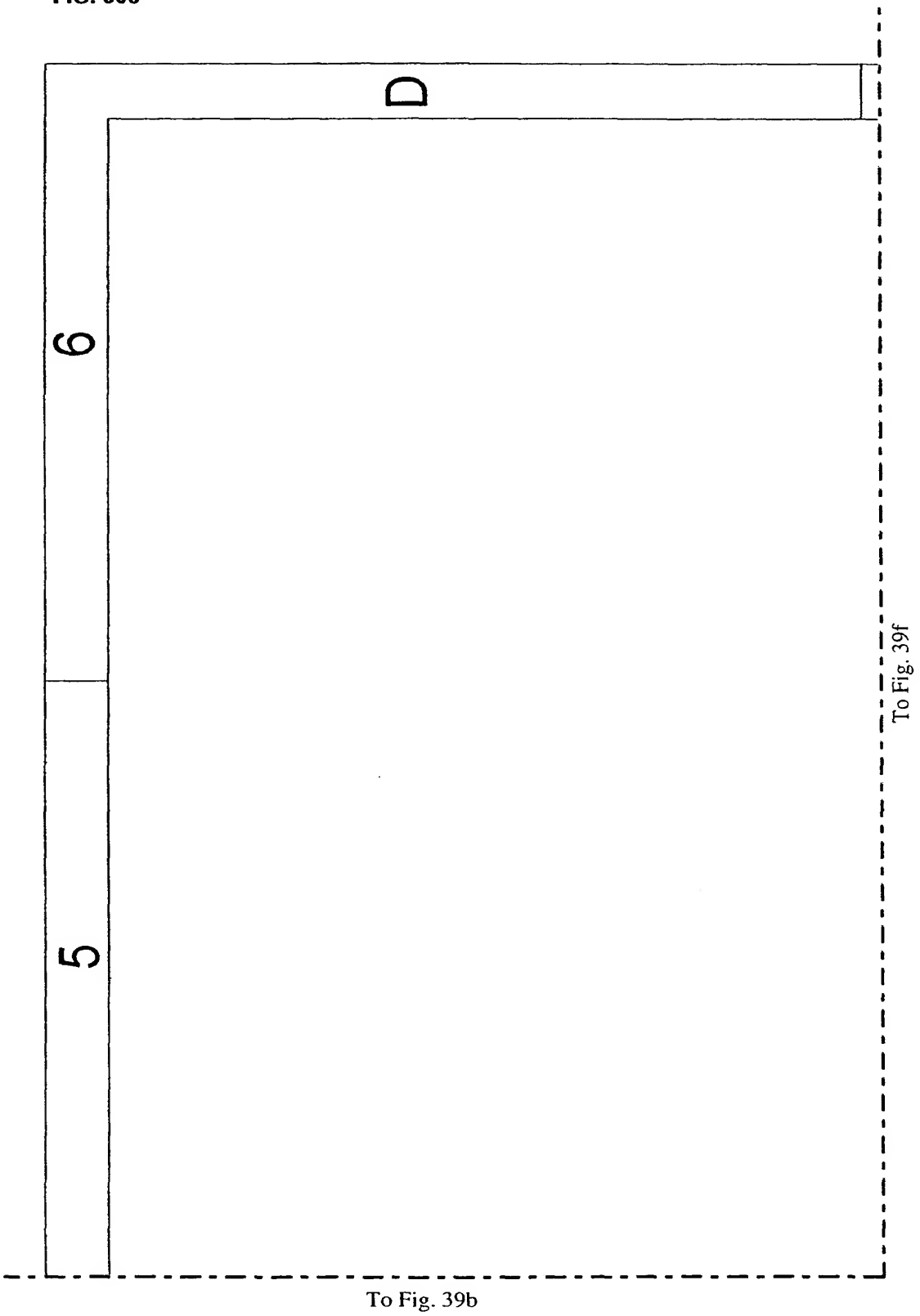


FIG. 39d

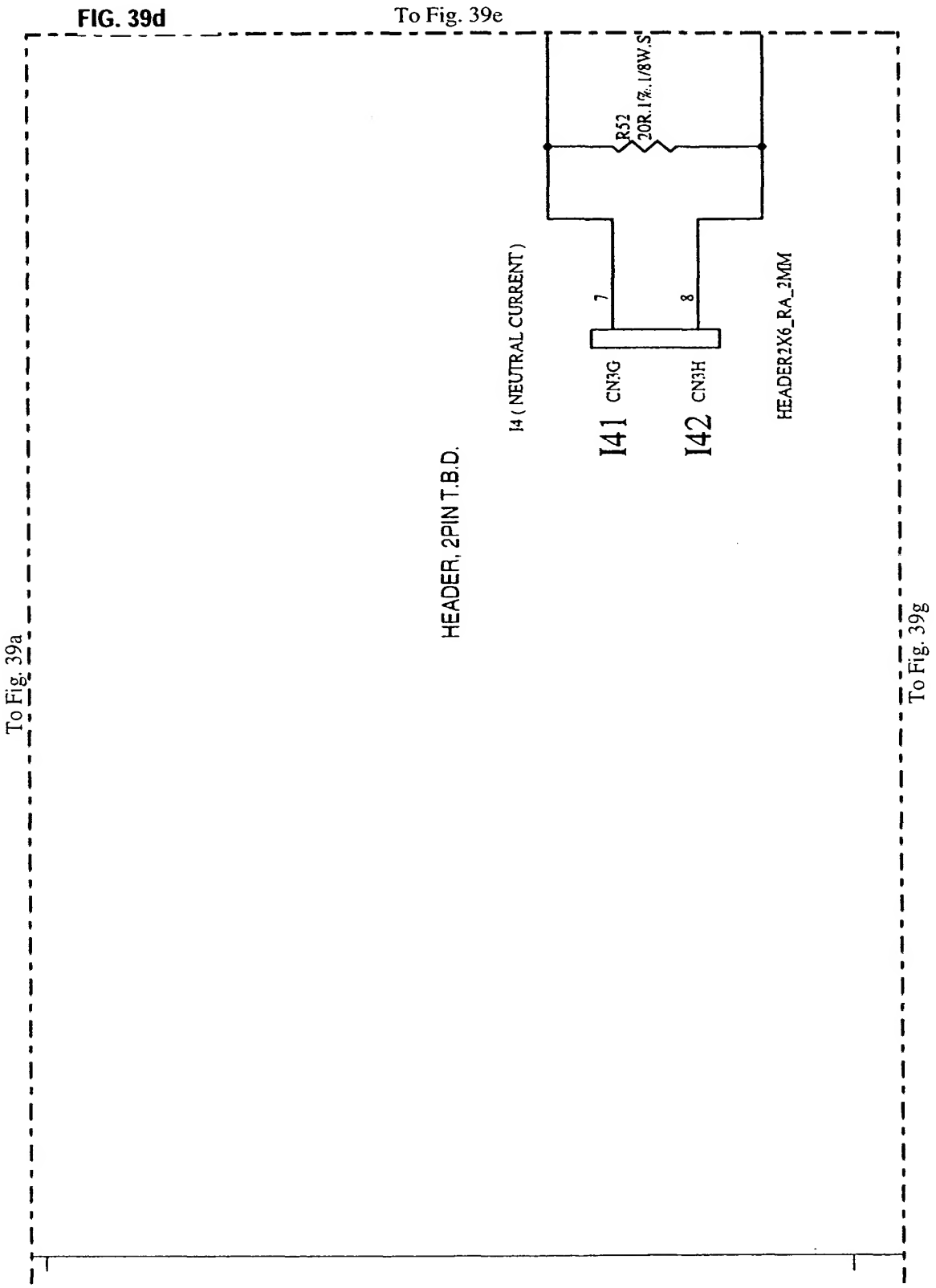

To Fig. 39e
To Fig. 39a
To Fig. 39g
HEADER, 2PIN T.B.D.
I4 (NEUTRAL CURRENT)
I41 CN3G
I42 CN3H
HEADER2X6_RA_2MM
R52
20R.1%.1/8W.S
7
8

FIG. 39e

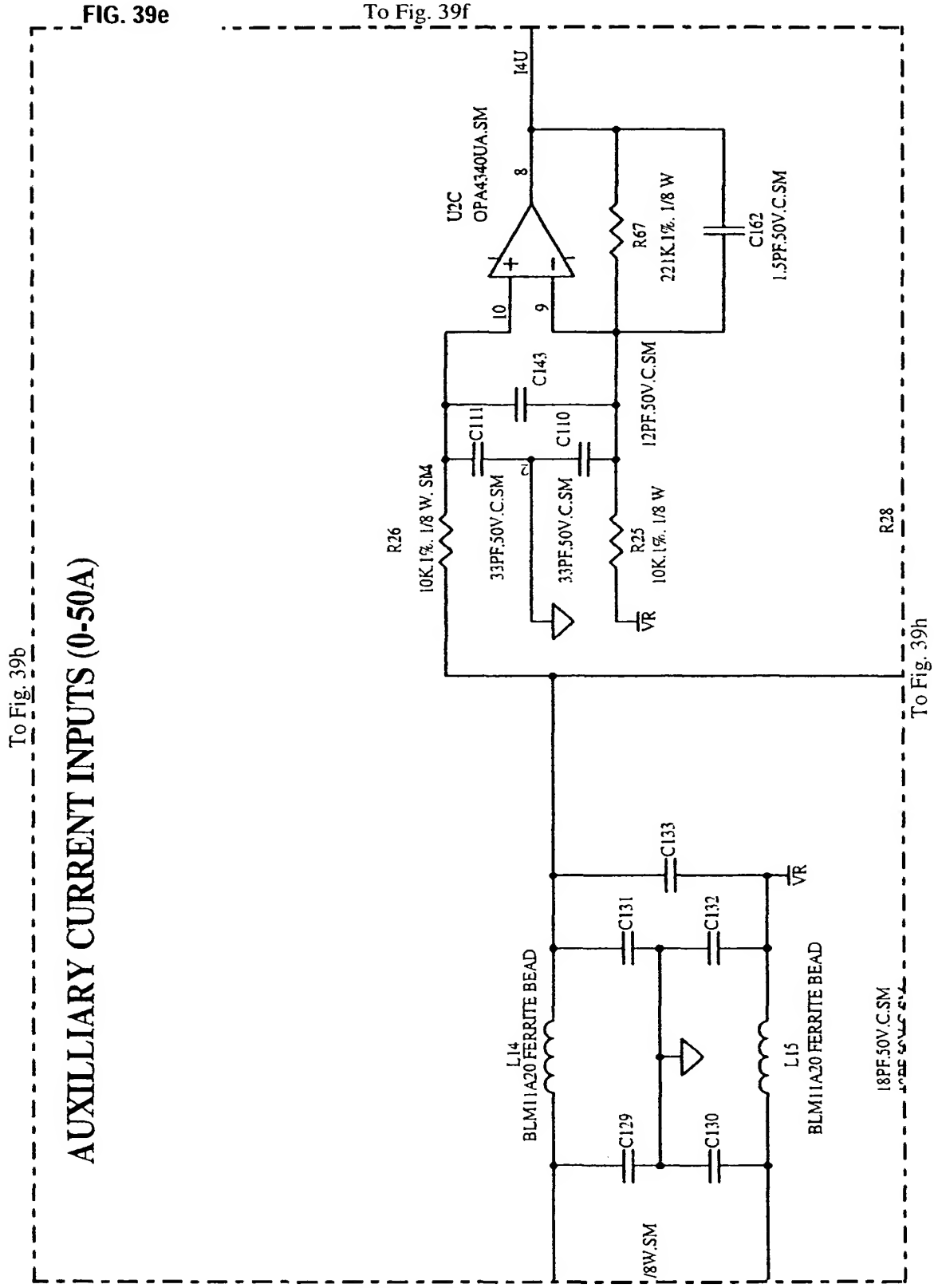

To Fig. 39f
AUXILLIARY CURRENT INPUTS (0-50A)
To Fig. 39b
To Fig. 39h
To Fig. 39d
I4U
U2C
OPA4340UA.SM
8
10
9
R67
221K.1%. 1/8 W
C162
1.5PF.50V.C.SM
C143
12PF.50V.C.SM
C111
C110
33PF.50V.C.SM
33PF.50V.C.SM
R26
10K.1%. 1/8 W. SM4
R25
10K.1%. 1/8 W
VR
R28
C133
C131
C132
L14
BLM11A20 FERRITE BEAD
L15
BLM11A20 FERRITE BEAD
C129
C130
18PF.50V.C.SM
/8W.SM

FIG. 39f

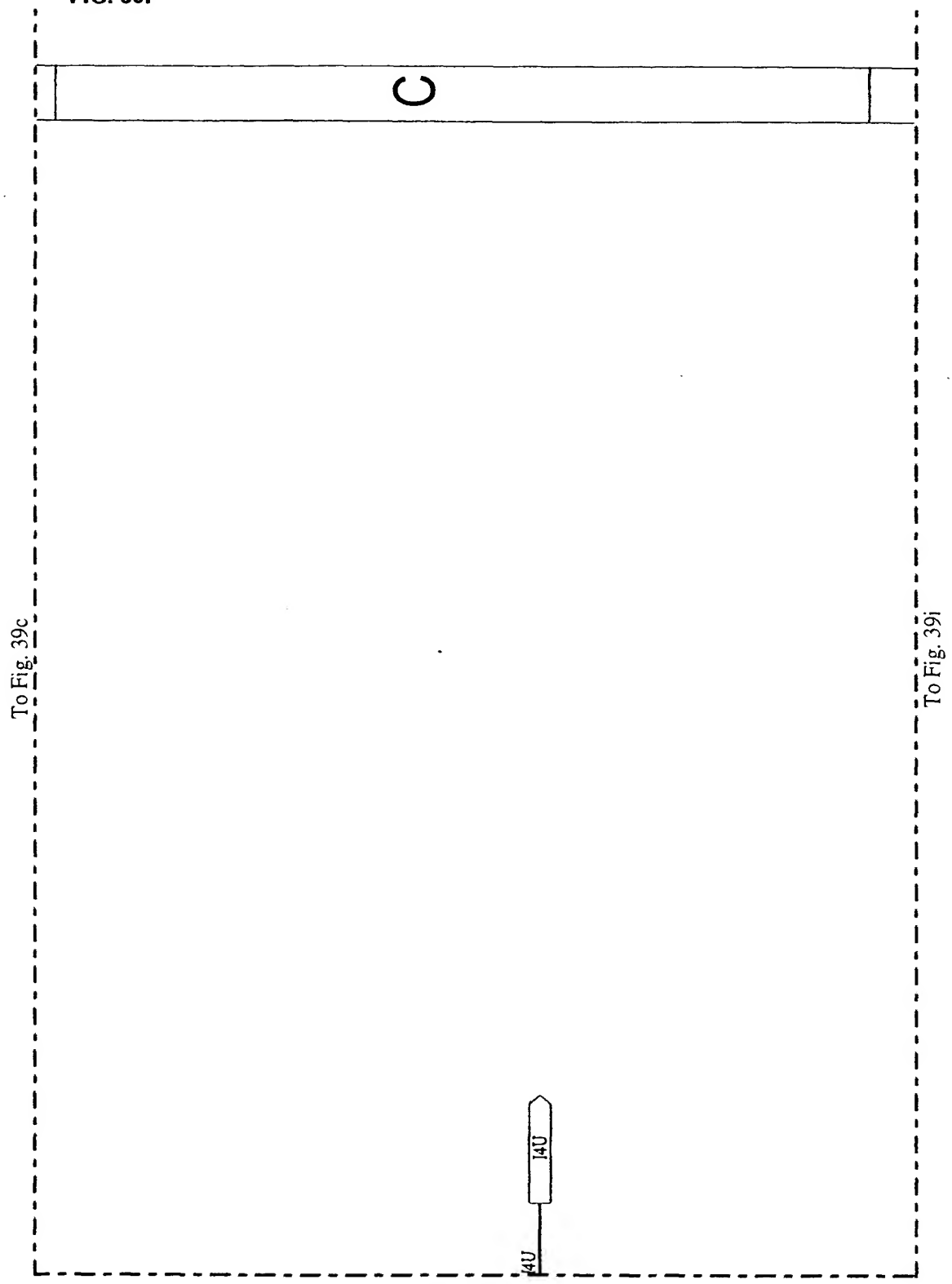


FIG. 39g

To Fig. 39h

To Fig. 39d

To Fig. 39j

FIG. 39h

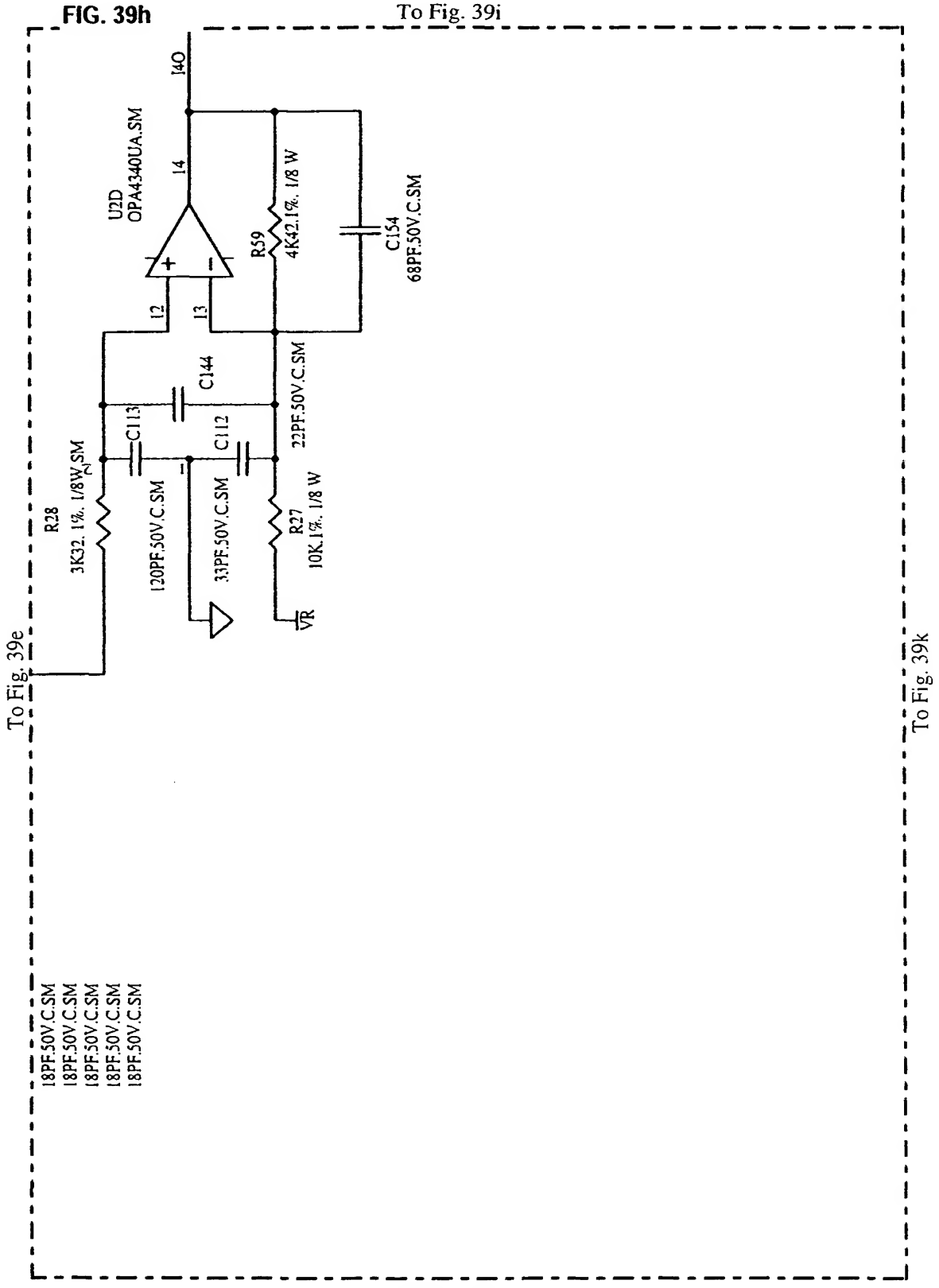

To Fig. 39i
To Fig. 39e
To Fig. 39k
To Fig. 39g
U2D
OPA4340UA.SM
14O
14
12
13
R59
4K42.1%. 1/8 W
C154
68PF.50V.C.SM
C144
22PF.50V.C.SM
C113
120PF.50V.C.SM
C112
33PF.50V.C.SM
R28
3K32. 1%. 1/8W.SM
R27
10K.1%. 1/8 W
VR
18PF.50V.C.SM
18PF.50V.C.SM
18PF.50V.C.SM
18PF.50V.C.SM
18PF.50V.C.SM

FIG. 39i

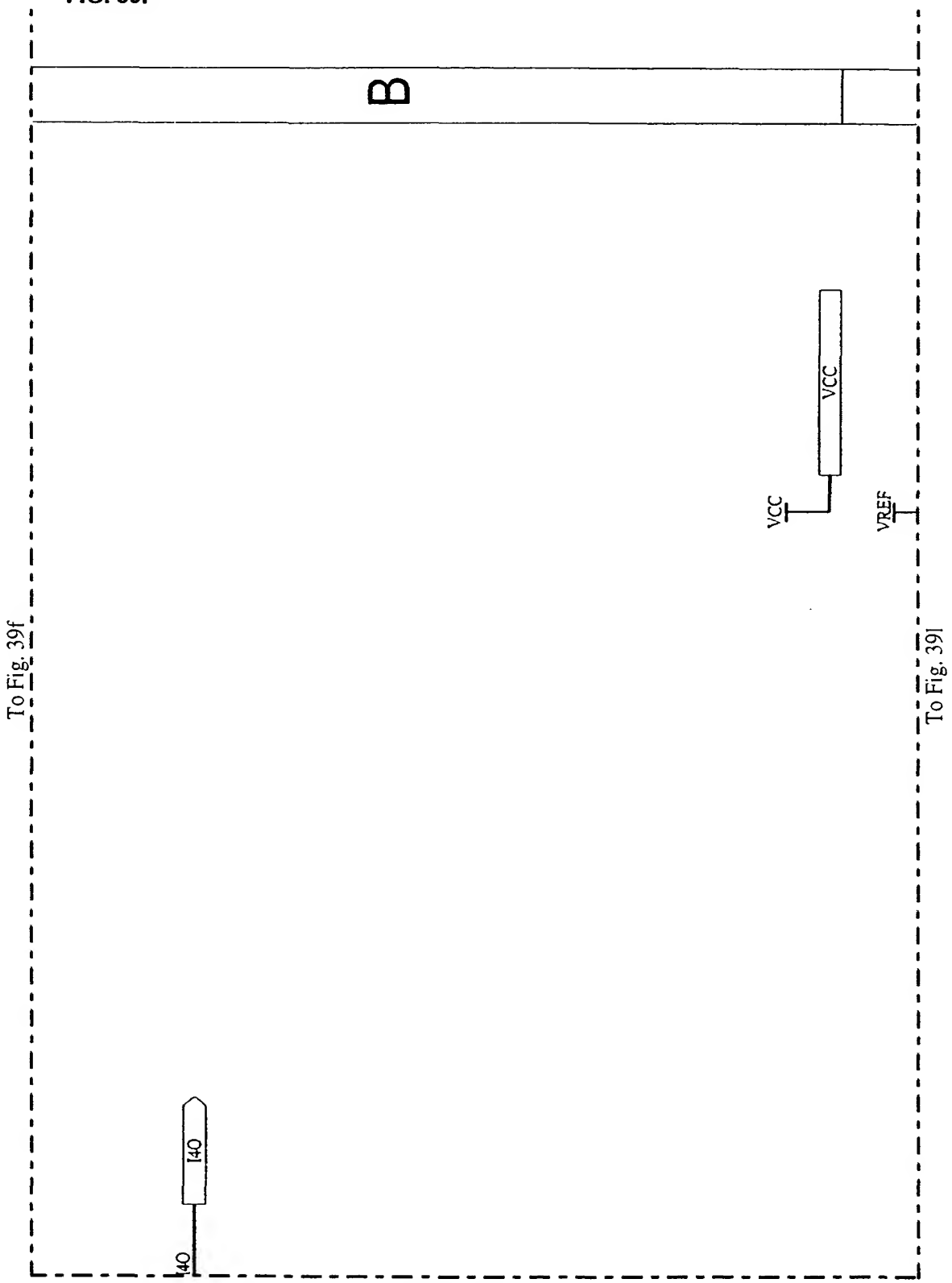


FIG. 39j

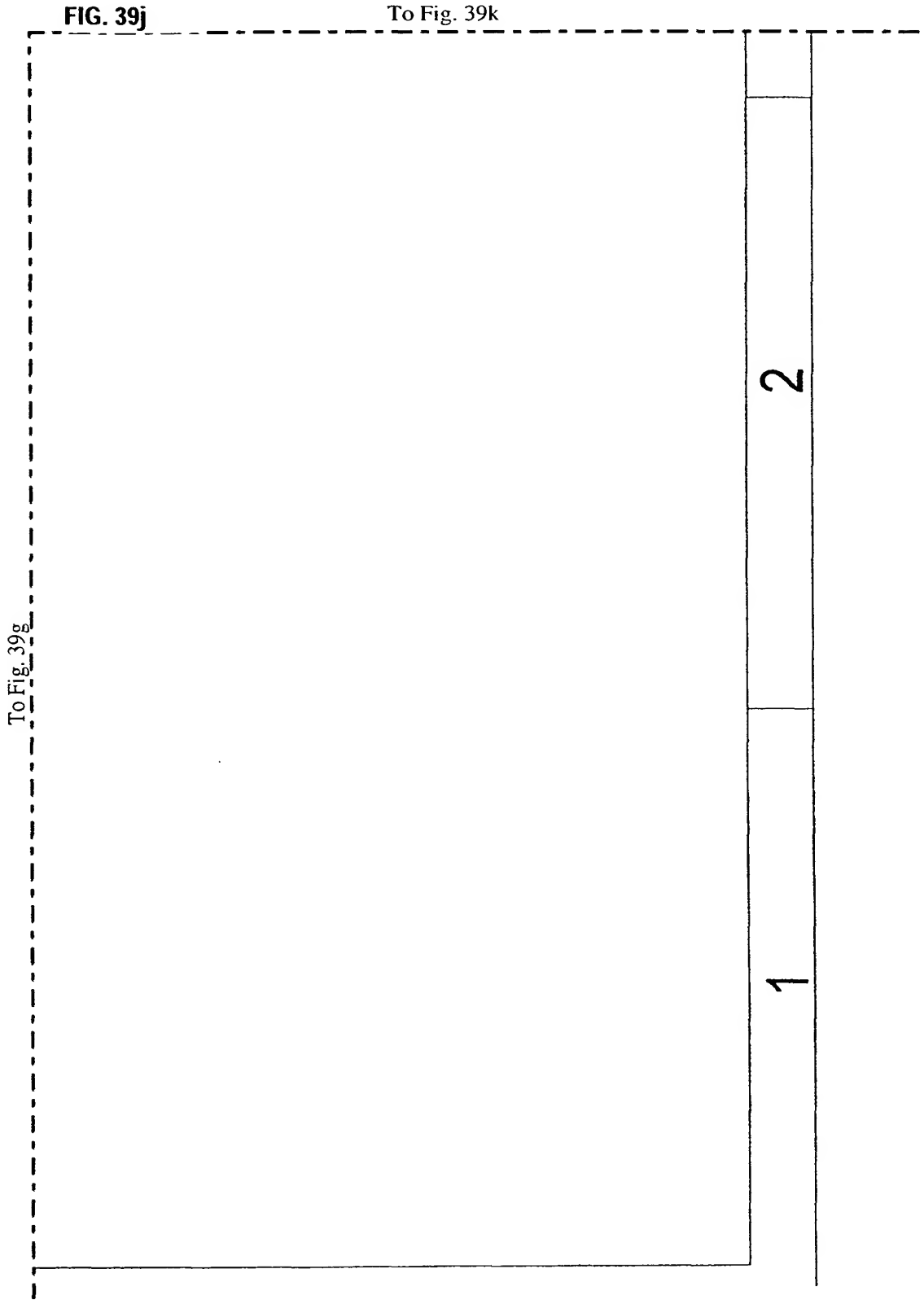


FIG. 39k

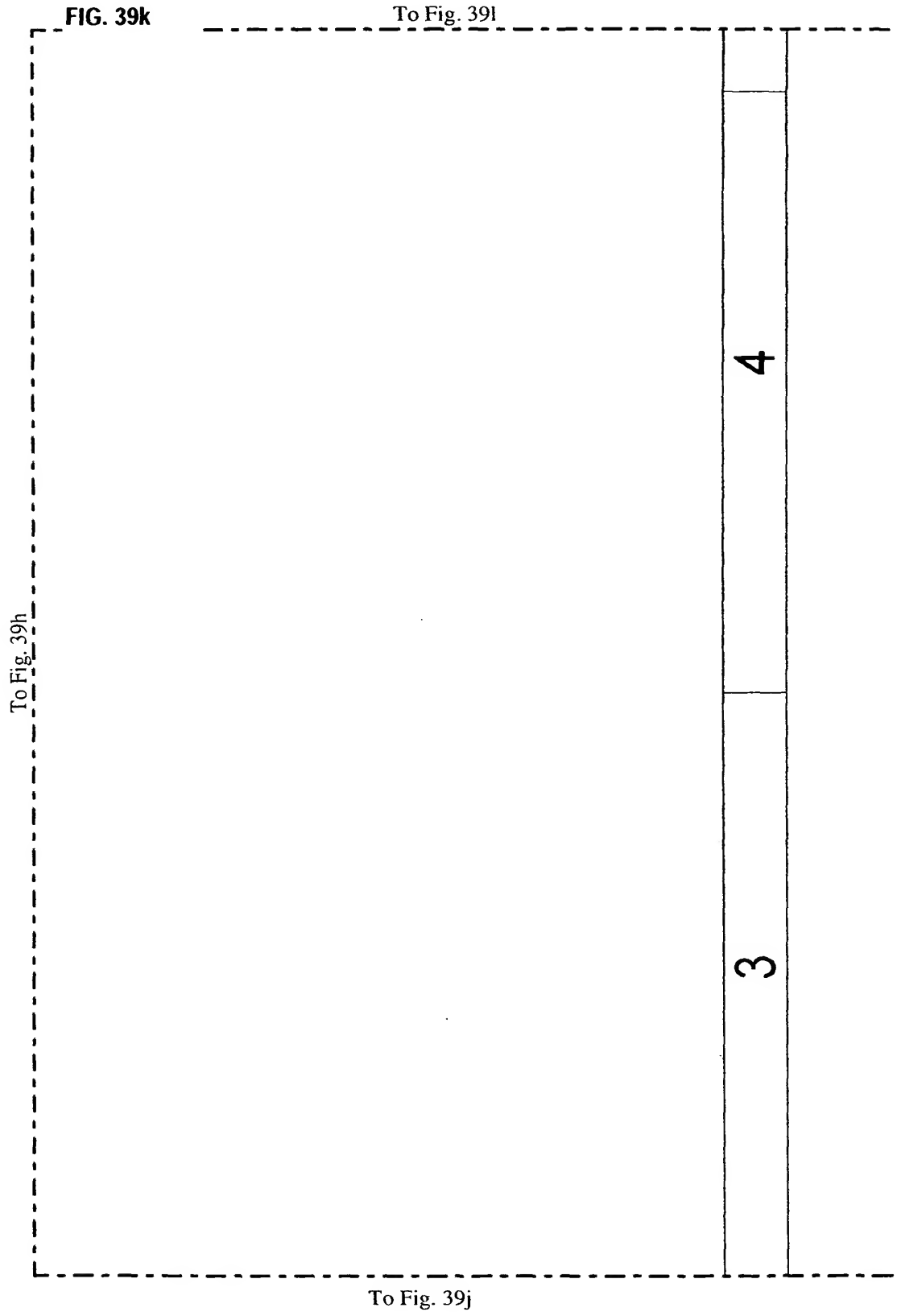
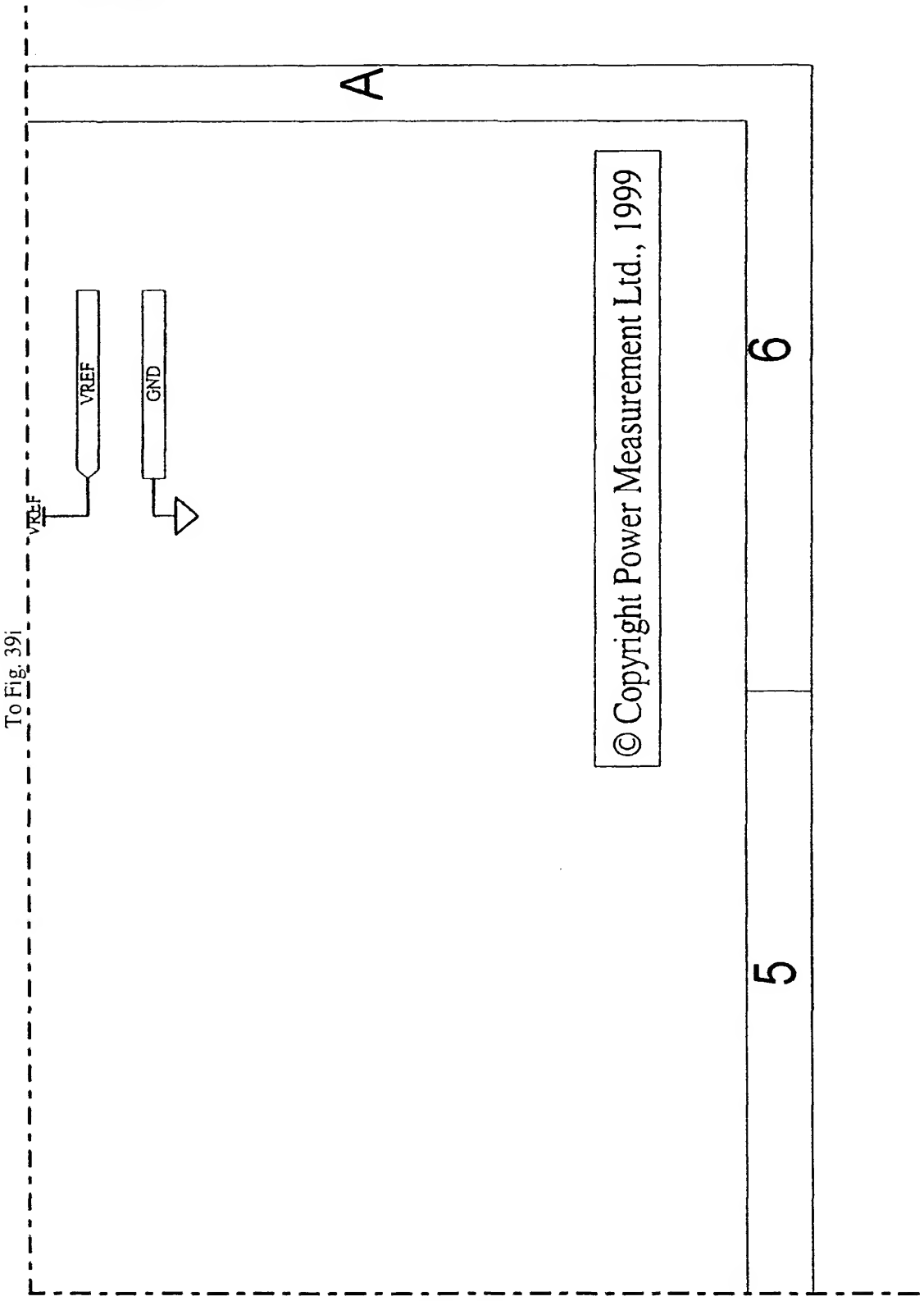


FIG. 39l



To Fig. 39k

FIG. 40a

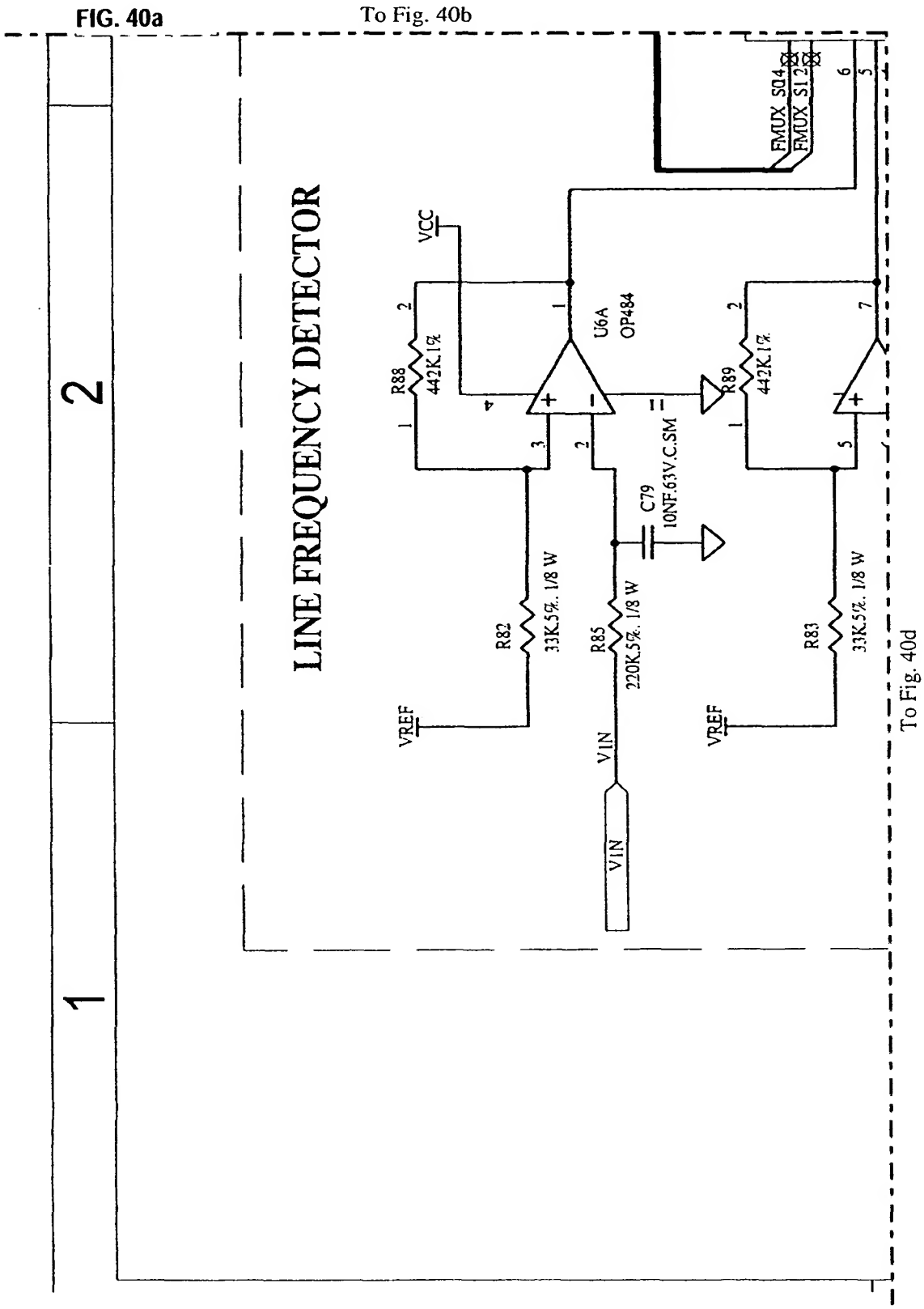

To Fig. 40b
LINE FREQUENCY DETECTOR
2
1
FMUX S04
FMUX S12
VCC
U6A
OP484
R88
442K.1%
R89
442K.1%
C79
10NF.63V.C.SM
R82
33K.5%. 1/8 W
R85
220K.5%. 1/8 W
R83
33K.5%. 1/8 W
VREF
VREF
VIN
VIN
To Fig. 40d

FIG. 40b

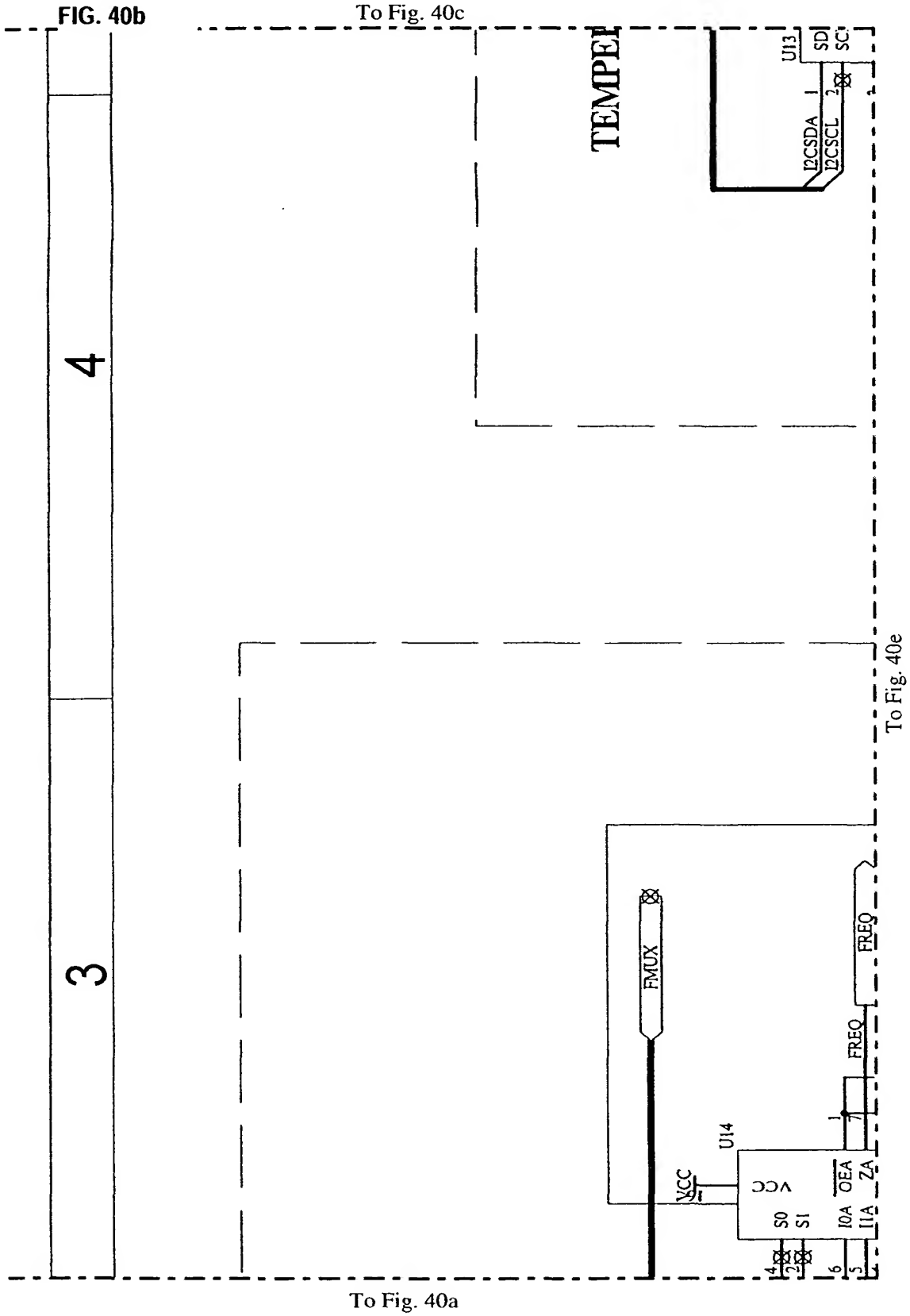
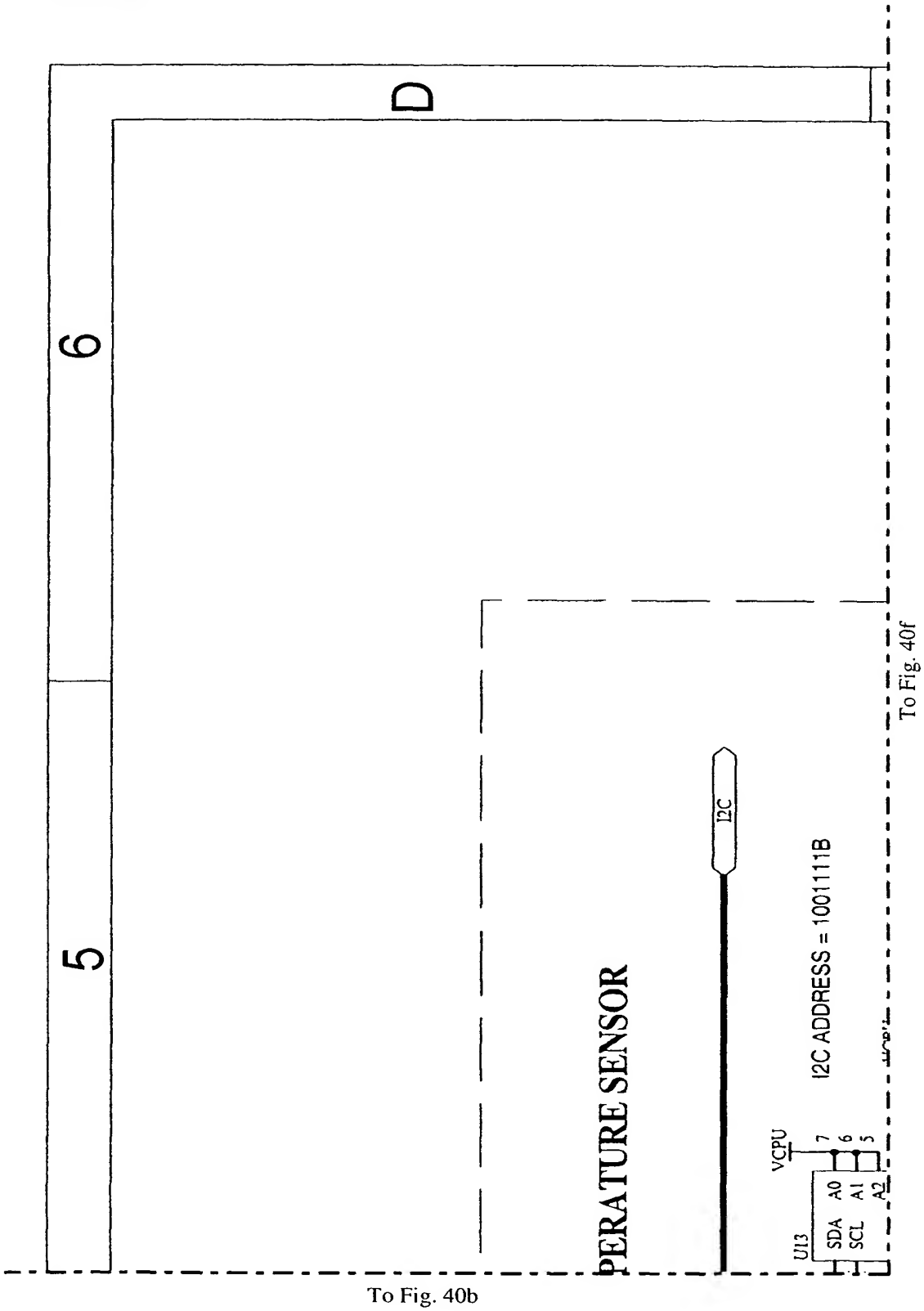

To Fig. 40c
TEMPE
U13
SDI
SCI
I2CSDA
I2CSCL
4
3
To Fig. 40e
FMUX
FREQ
FREQ
U14
VCC
VCC
OEA
2A
S0
S1
I0A
I1A
To Fig. 40a

FIG. 40c



To Fig. 40b

FIG. 40d

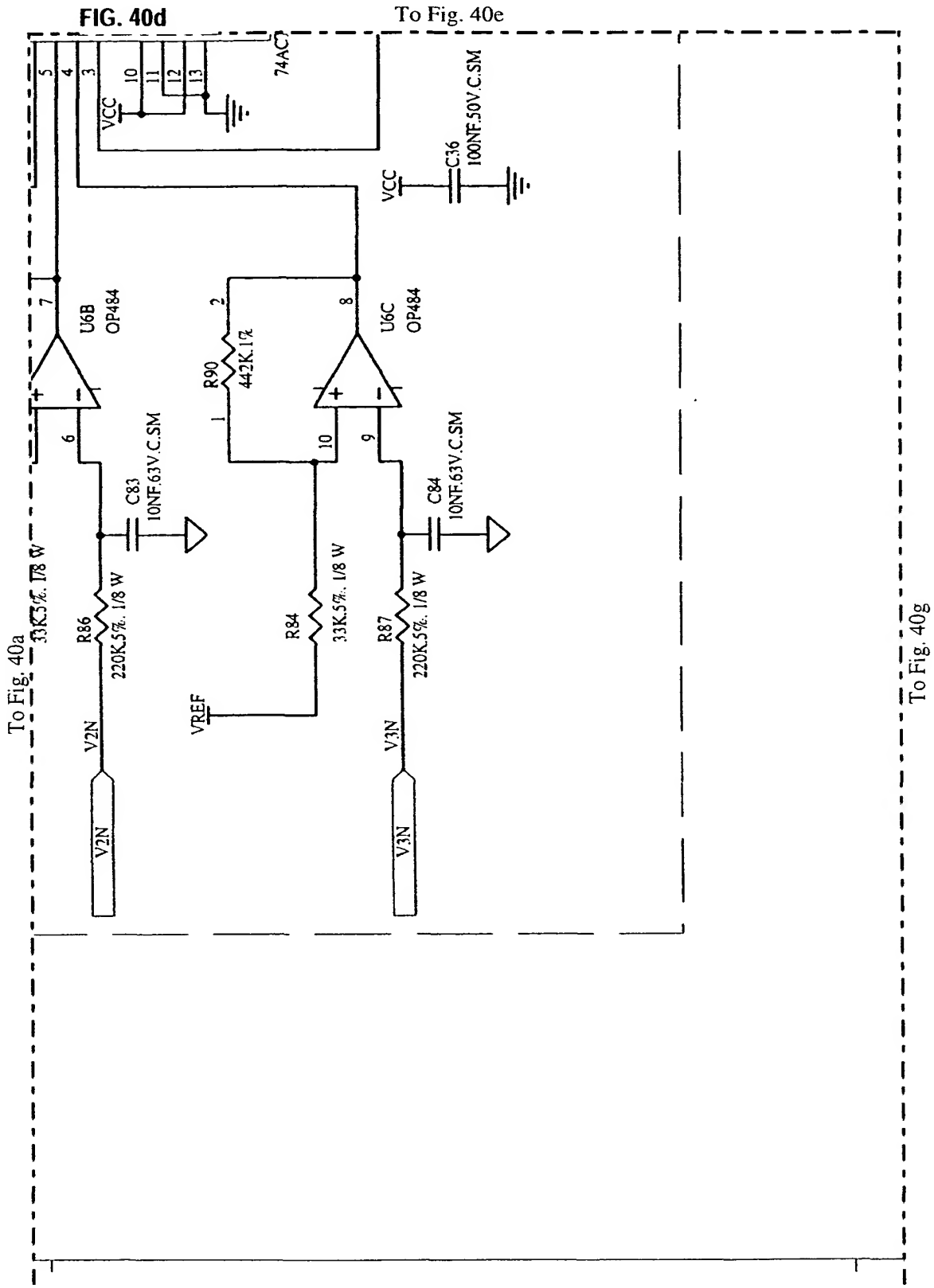

To Fig. 40e
To Fig. 40a
To Fig. 40g
74AC7
VCC
C36
100NF.50V.C.SM
U6B
OP484
U6C
OP484
R90
442K.1%
C83
10NF.63V.C.SM
C84
10NF.63V.C.SM
R86
220K.5%. 1/8 W
R84
33K.5%. 1/8 W
R87
220K.5%. 1/8 W
VREF
V2N
V3N

FIG. 40e

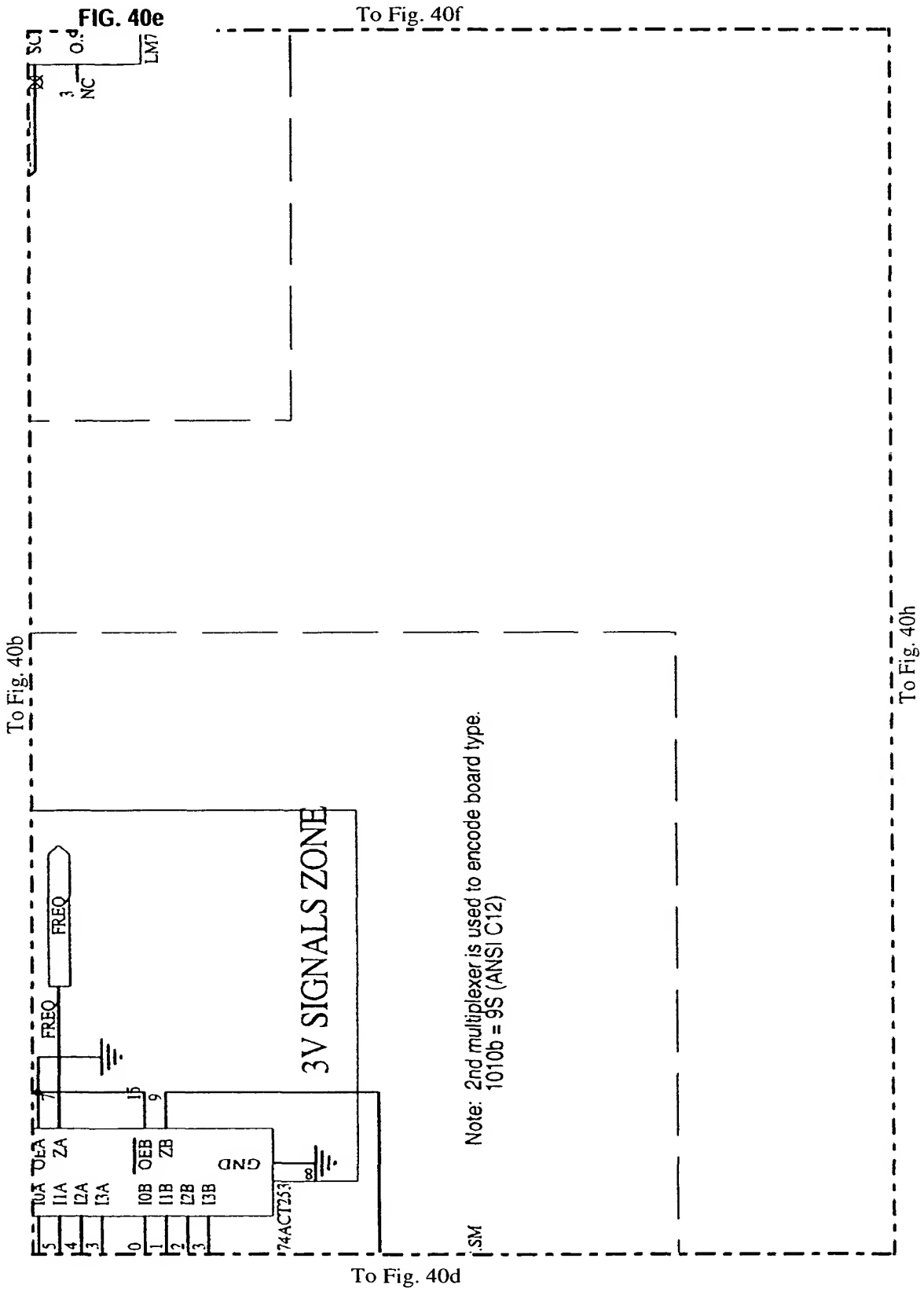
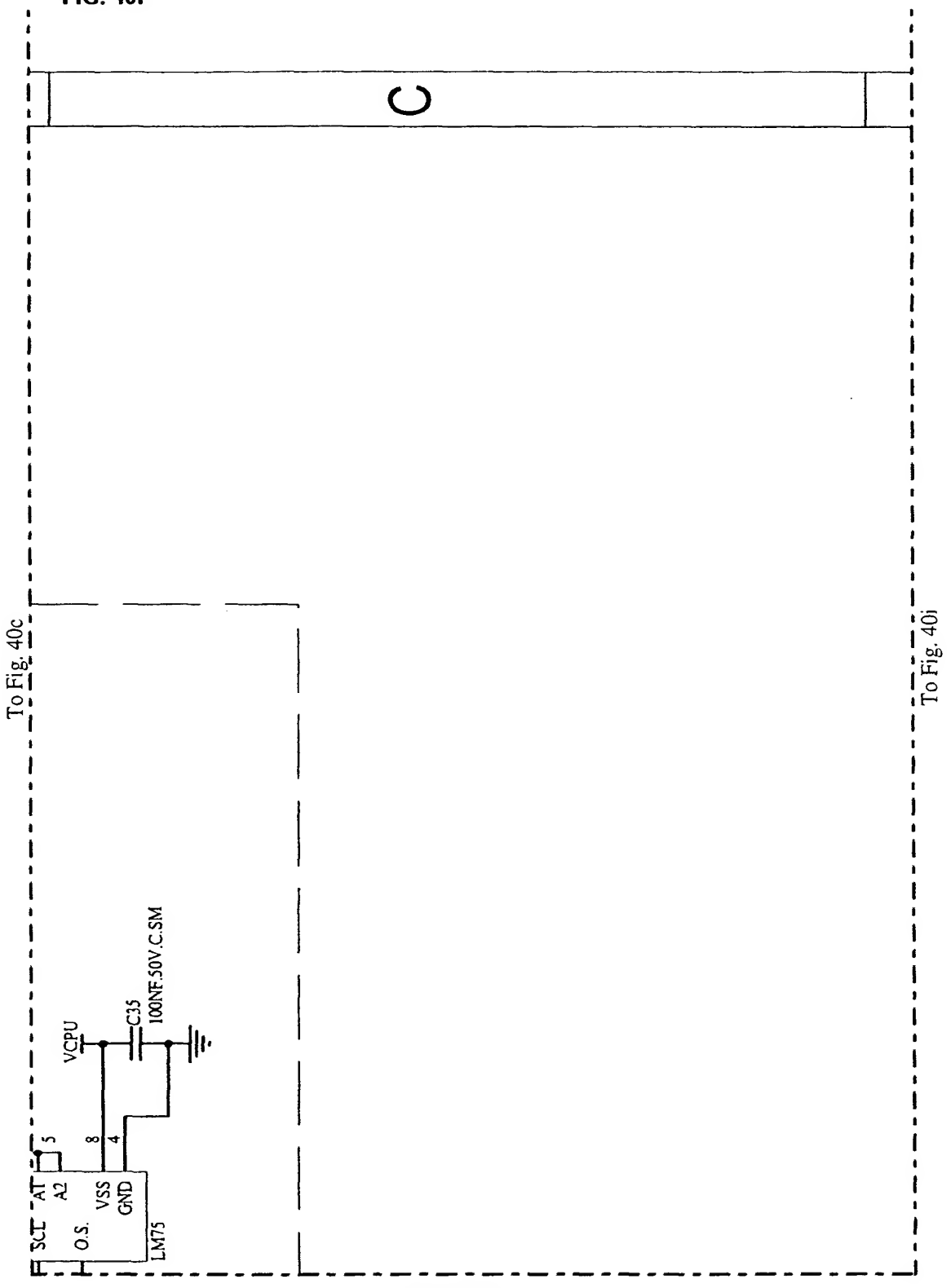

To Fig. 40f
To Fig. 40b
To Fig. 40h
To Fig. 40d
3V SIGNALS ZONE
FREQ
FREQ
Note: 2nd multiplexer is used to encode board type.
1010b = 9S (ANSI C12)
74ACT253
GND
OEA
ZA
OEB
ZB
I0A
I1A
I2A
I3A
I0B
I1B
I2B
I3B
NC
LM7

FIG. 40f



To Fig. 40e

FIG. 40g

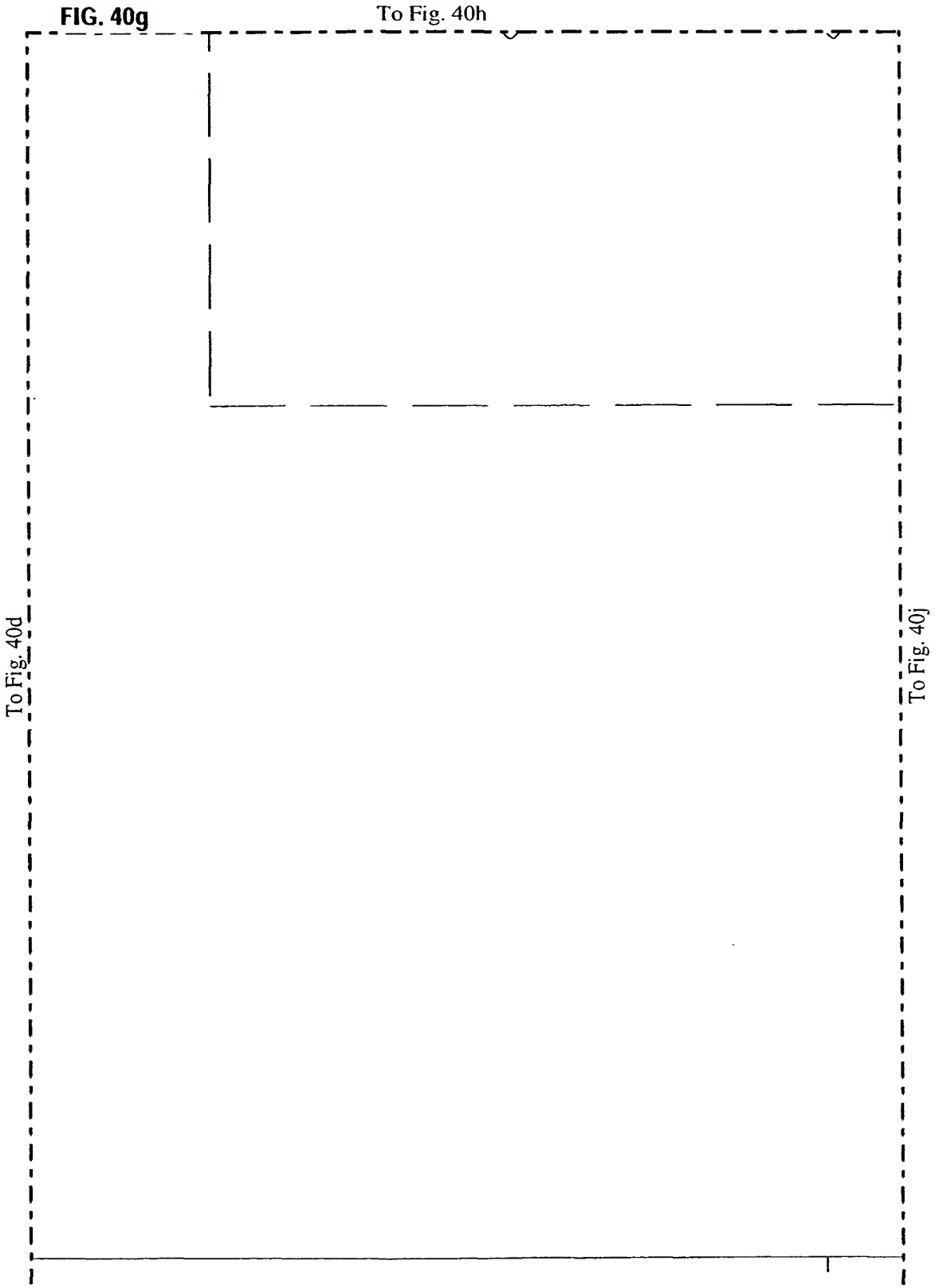


FIG. 40h

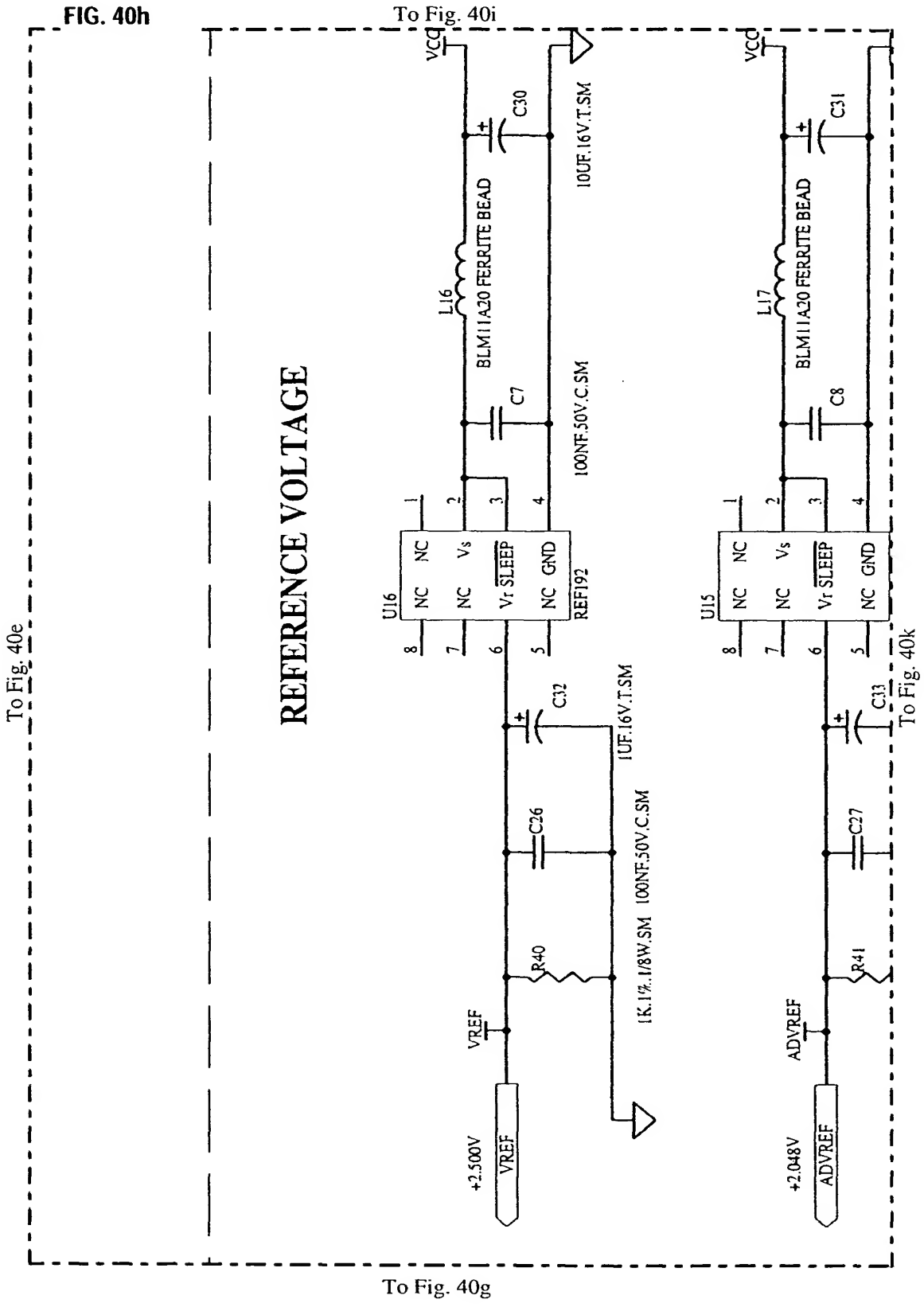

To Fig. 40i
To Fig. 40e
To Fig. 40k
To Fig. 40g
REFERENCE VOLTAGE
VCC
C30
10UF.16V.T.SM
L16
BLM11A20 FERRITE BEAD
C7
100NF.50V.C.SM
U16
NC
Vs
Vr SLEEP
GND
REF192
C32
1UF.16V.T.SM
C26
100NF.50V.C.SM
R40
1K.1%..1/8W.SM
VREF
+2.500V
VREF
L17
BLM11A20 FERRITE BEAD
C31
C8
U15
C33
C27
R41
ADVREF
+2.048V
ADVREF

FIG. 40i

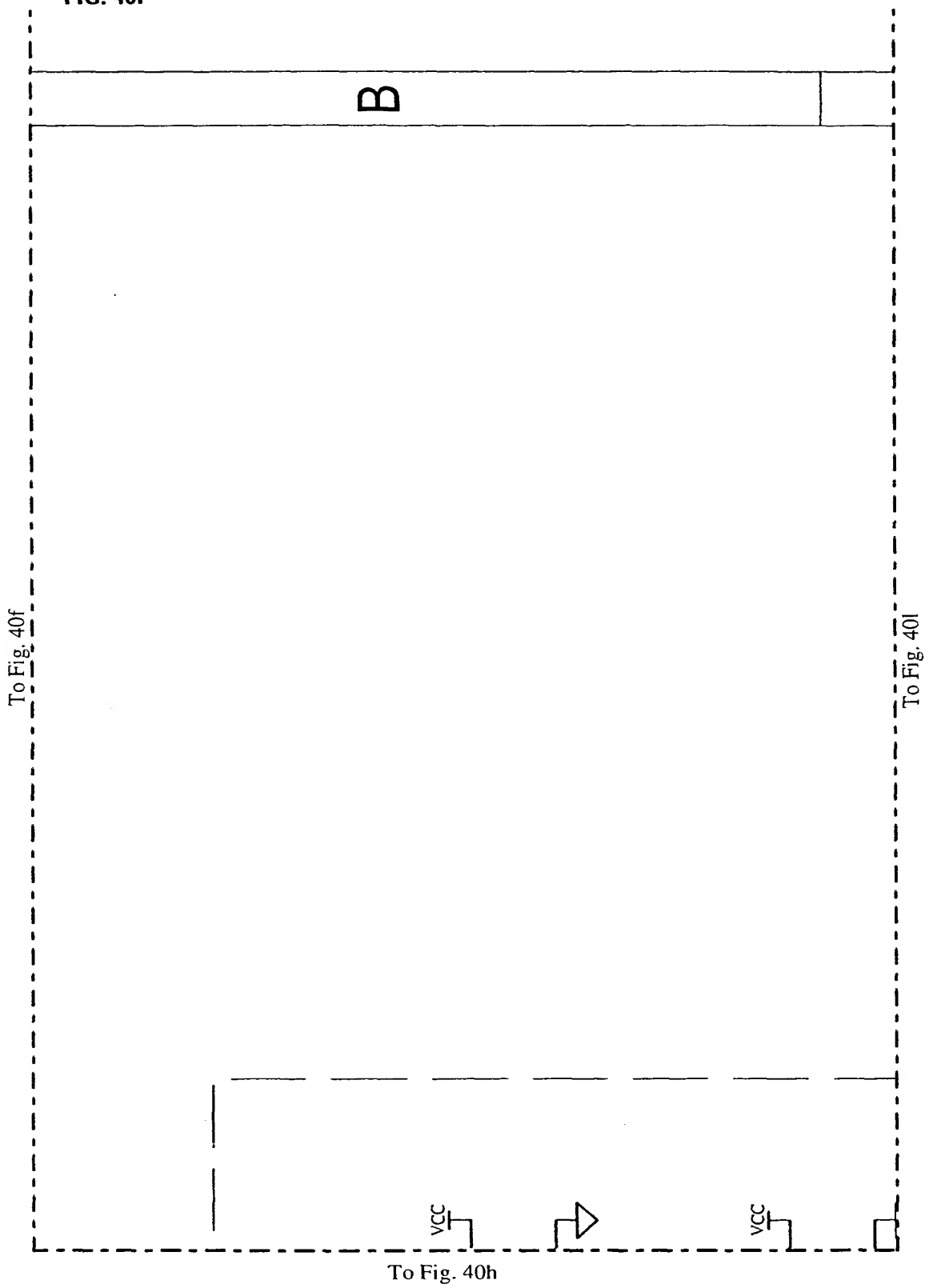


FIG. 40j

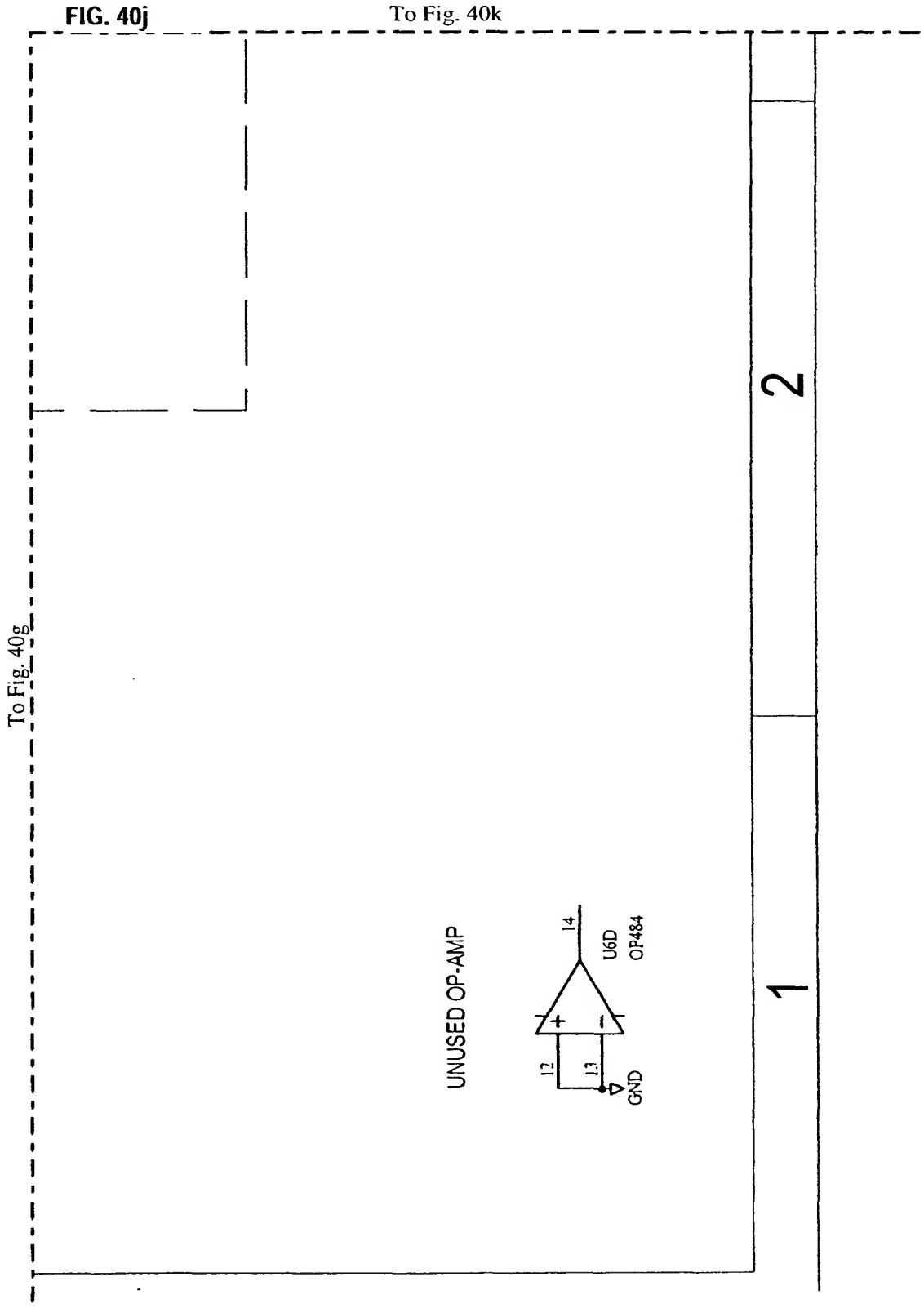
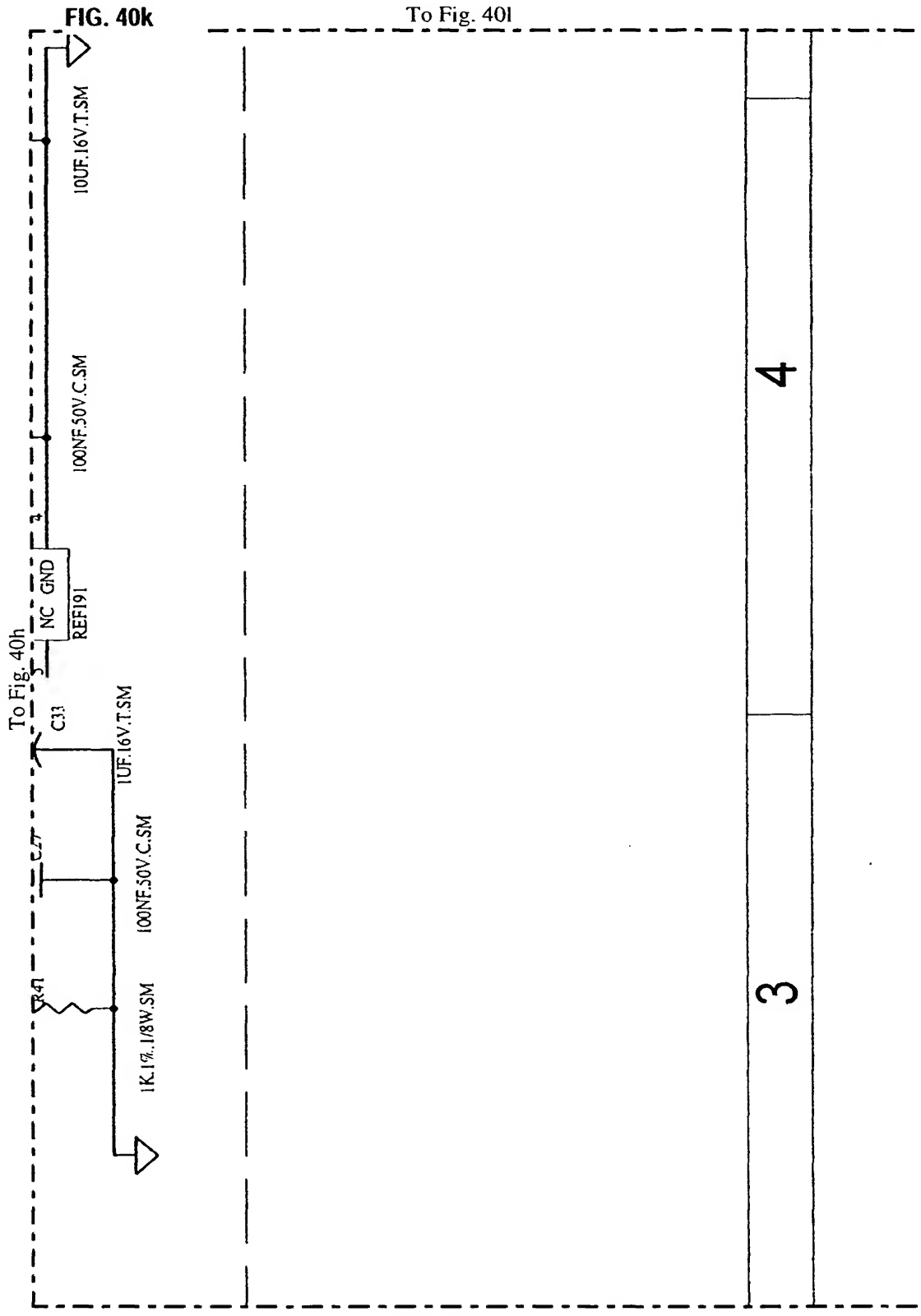


FIG. 40k



To Fig. 40j

FIG. 40l

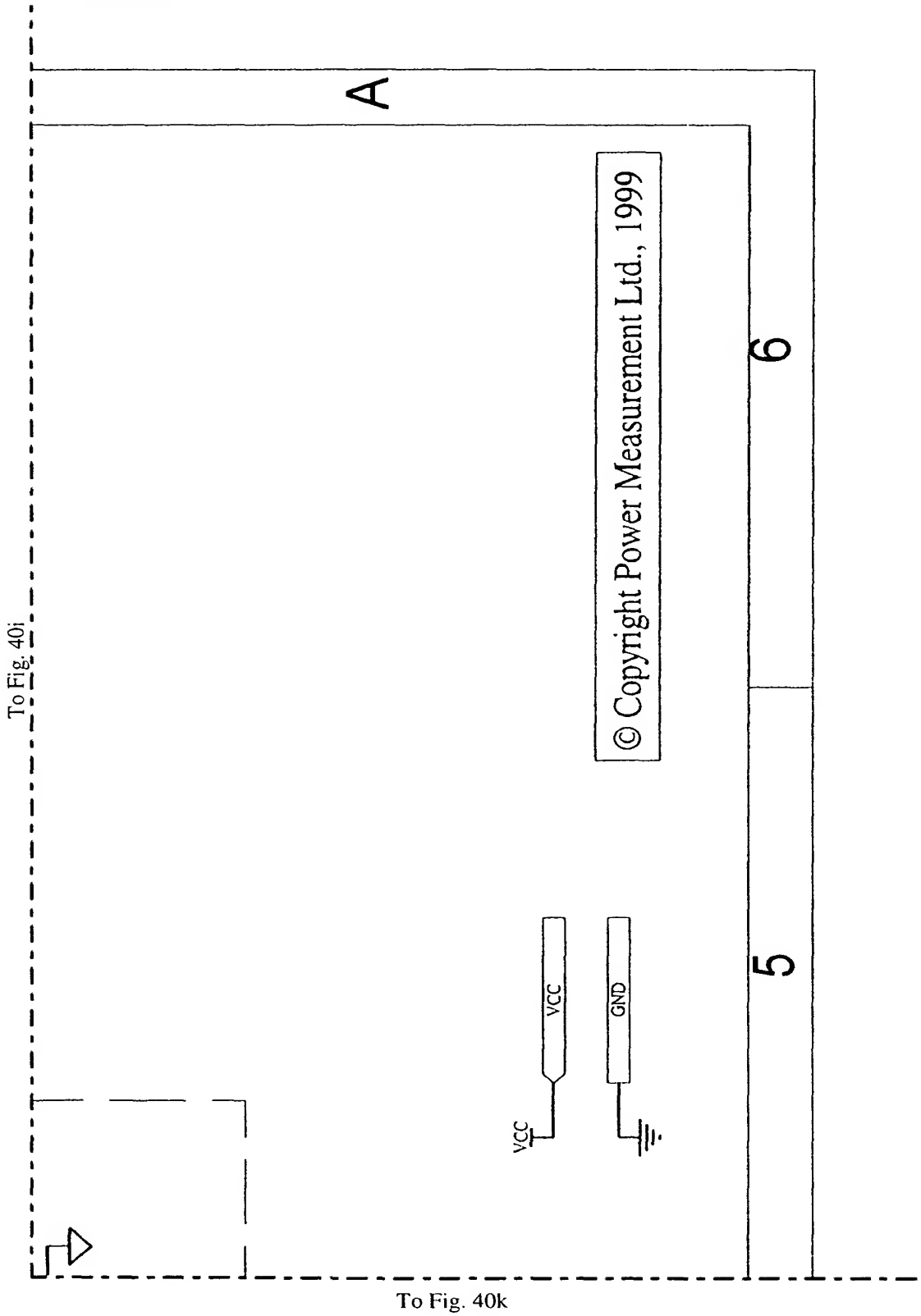

A
6
5
© Copyright Power Measurement Ltd., 1999
VCC
GND
VCC
To Fig. 40i
To Fig. 40k

FIG. 41a

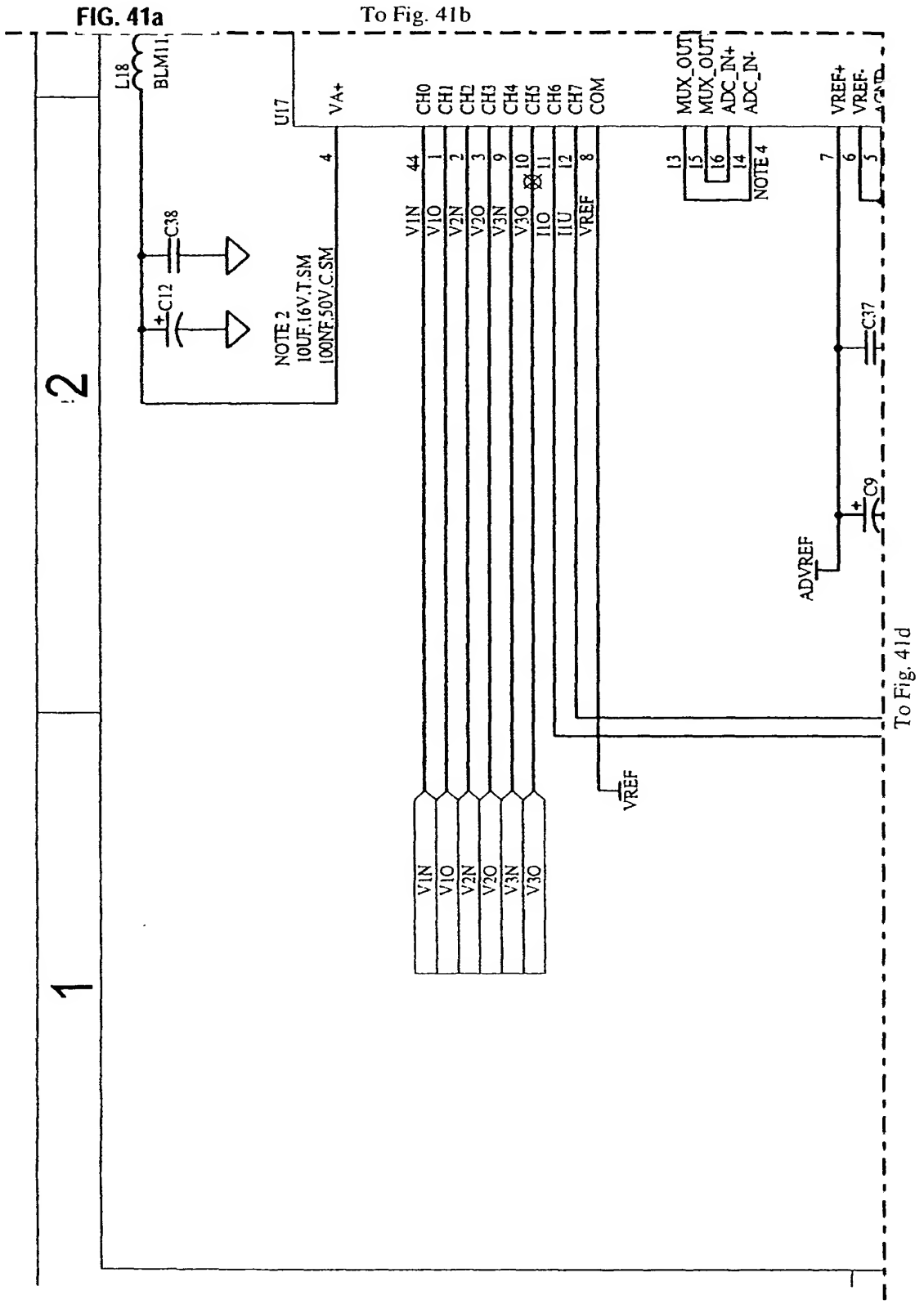

To Fig. 41b
L18
BLM11
U17
VA+
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
MUX_OUT
MUX_OUT
ADC_IN+
ADC_IN-
VREF+
VREF-
C38
C12
NOTE 2
10UF,16V,T,SM
100NF,50V,C,SM
NOTE 4
C37
C9
ADVREF
VREF
V1N
V1O
V2N
V2O
V3N
V3O
I1O
I1U
2
1
To Fig. 41d

FIG. 41b

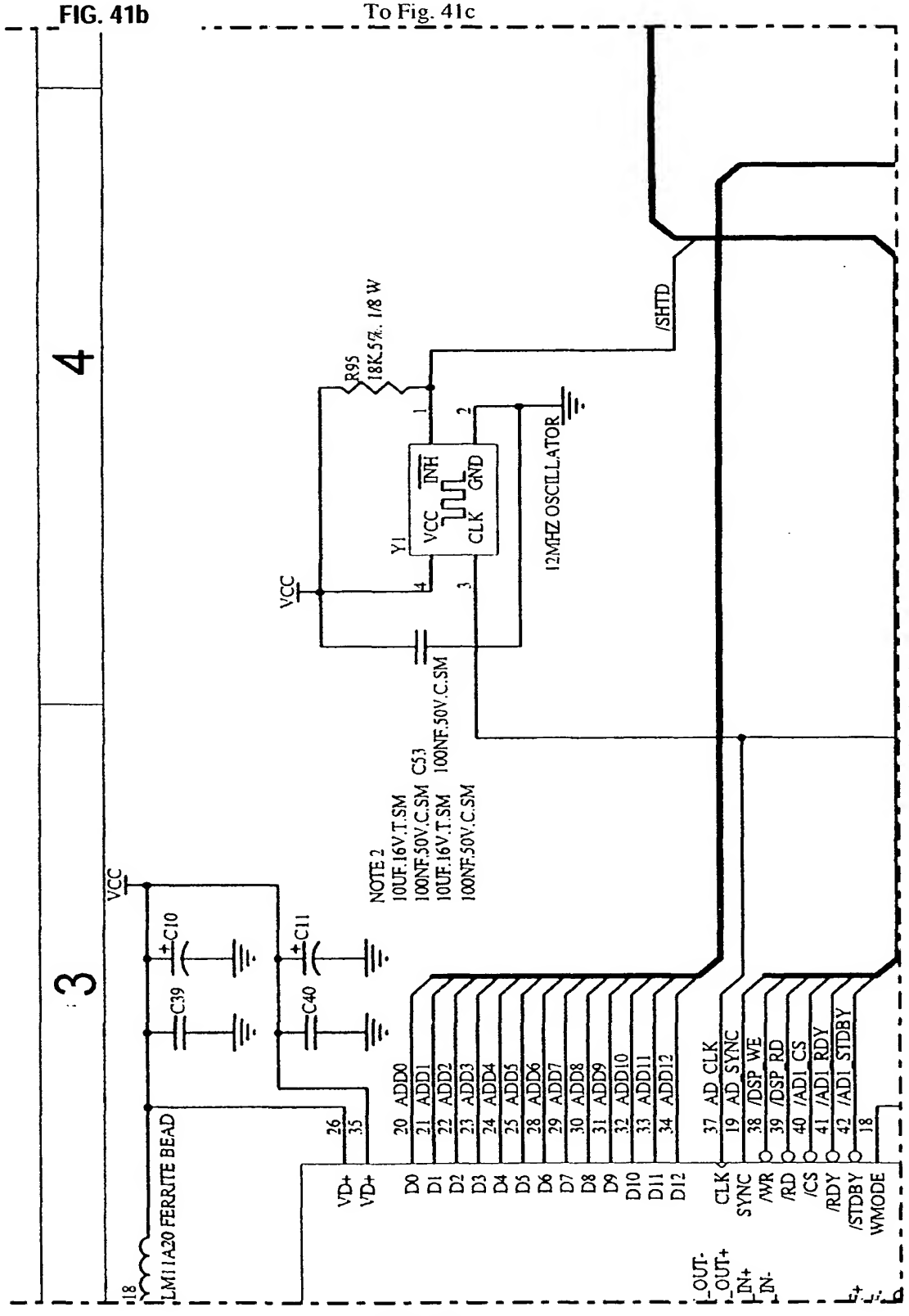

To Fig. 41c
To Fig. 41e
To Fig. 41a
4
3
/SHTD
R95
18K.5%. 1/8 W
Y1
VCC
INH
CLK
GND
12MHZ OSCILLATOR
NOTE 2
10UF.16V.T.SM
100NF.50V.C.SM
C53
100NF.50V.C.SM
10UF.16V.T.SM
100NF.50V.C.SM
C10
C11
C39
C40
LM11A20 FERRITE BEAD
VD+
VD+
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
CLK
SYNC
/WR
/RD
/CS
/RDY
/STDBY
WMODE
ADD0
ADD1
ADD2
ADD3
ADD4
ADD5
ADD6
ADD7
ADD8
ADD9
ADD10
ADD11
ADD12
AD_CLK
AD_SYNC
/DSP_WE
/DSP_RD
/AD1_CS
/AD1_RDY
/AD1_STDBY
_OUT-
_OUT+
IN+
IN-

FIG. 41c

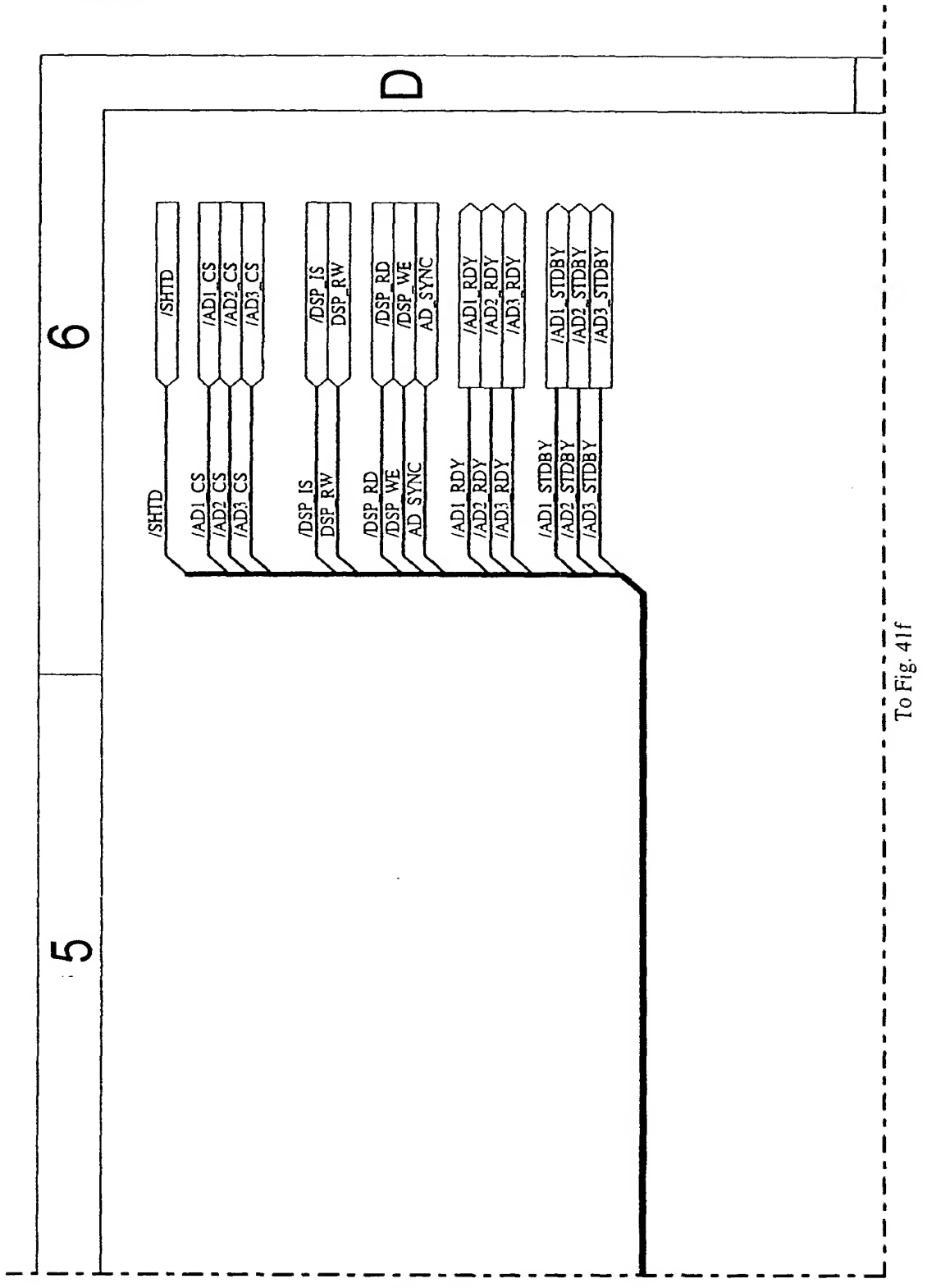

D
6
5
/SHTD
/AD1_CS
/AD2_CS
/AD3_CS
/DSP_IS
DSP_RW
/DSP_RD
/DSP_WE
AD_SYNC
/AD1_RDY
/AD2_RDY
/AD3_RDY
/AD1_STDBY
/AD2_STDBY
/AD3_STDBY
To Fig. 41f
To Fig. 41b

FIG. 41d

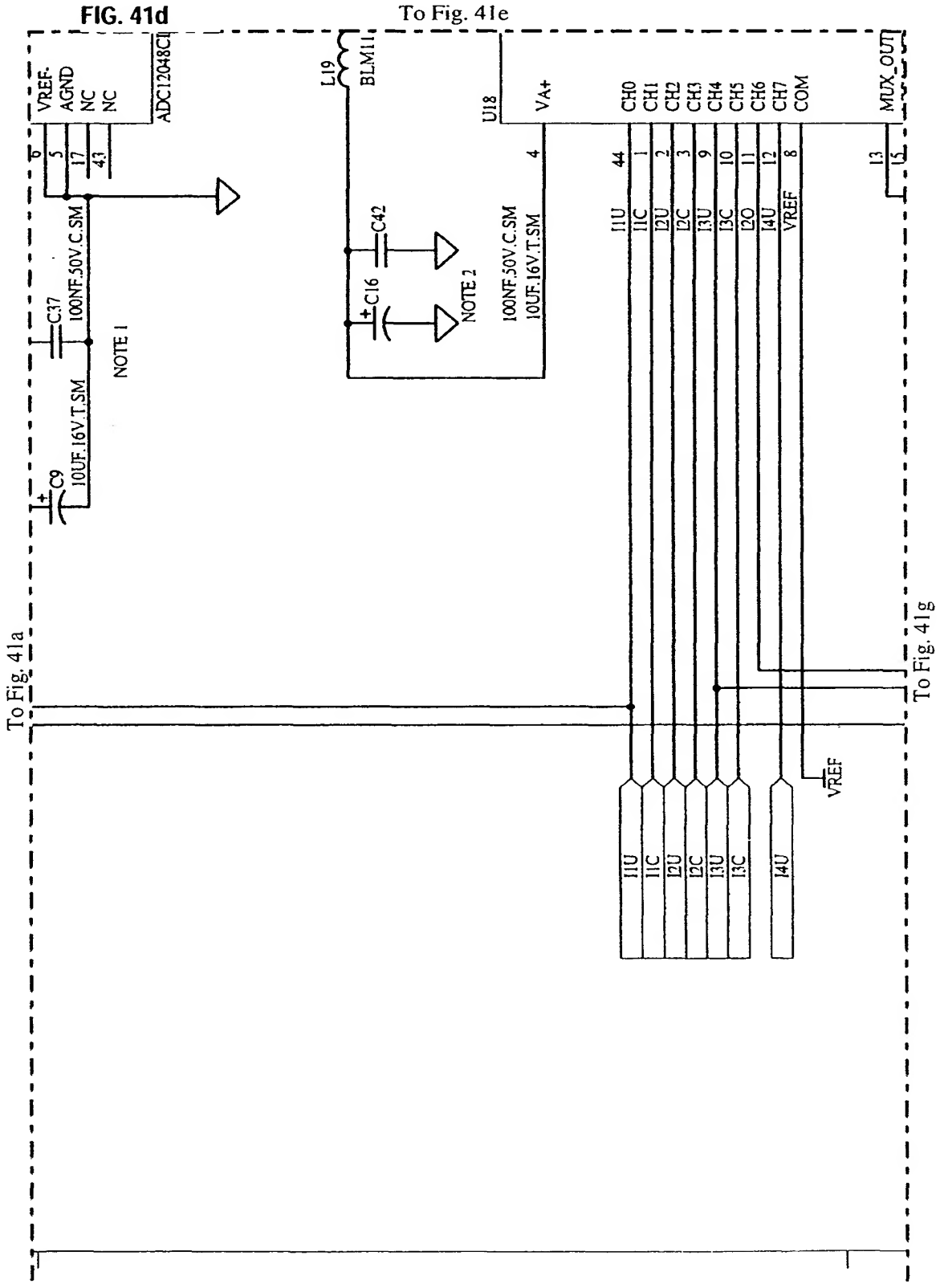

To Fig. 41e
To Fig. 41a
To Fig. 41g
ADC12048CI
VREF-
AGND
NC
NC
6
5
17
43
C37
100NF.50V.C.SM
C9
10UF.16V.T.SM
NOTE 1
L19
BLM11
C42
C16
NOTE 2
100NF.50V.C.SM
10UF.16V.T.SM
U18
VA+
4
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
44
1
2
3
9
10
11
12
8
I1U
I1C
I2U
I2C
I3U
I3C
I4U
I4C
VREF
MUX_OUT
13
15

FIG. 41e

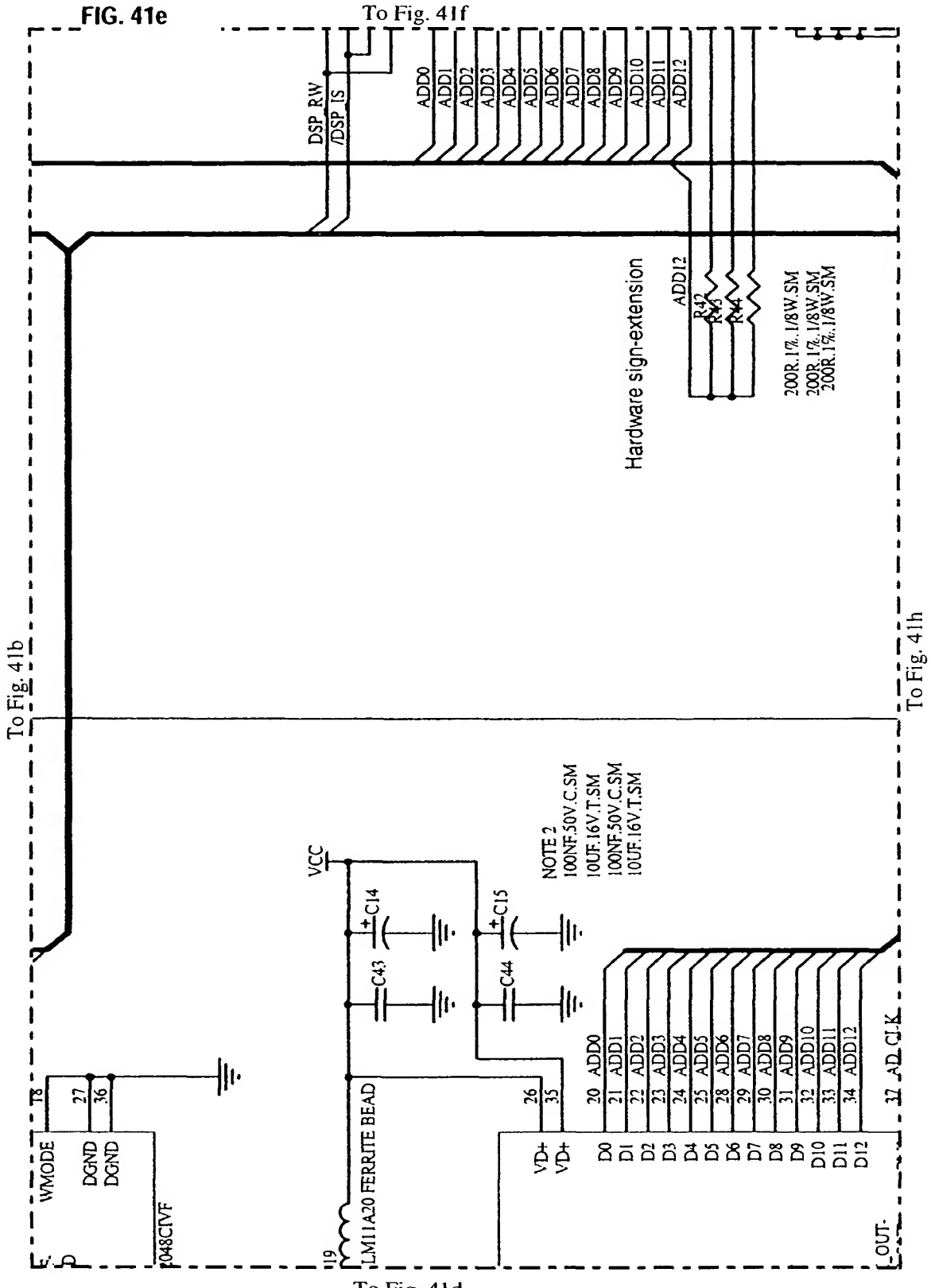

To Fig. 41f
DSP_RW
/DSP_IS
ADD0
ADD1
ADD2
ADD3
ADD4
ADD5
ADD6
ADD7
ADD8
ADD9
ADD10
ADD11
ADD12
Hardware sign-extension
R42
R43
R44
200R.1%.1/8W.SM
200R.1%.1/8W.SM
200R.1%.1/8W.SM
To Fig. 41b
To Fig. 41h
VCC
C14
C15
C43
C44
NOTE 2
100NF.50V.C.SM
10UF.16V.T.SM
100NF.50V.C.SM
10UF.16V.T.SM
WMODE
DGND
DGND
048CIVF
LM11A20 FERRITE BEAD
VD+
VD+
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
AD_CLK
OUT-
To Fig. 41d

FIG. 41f

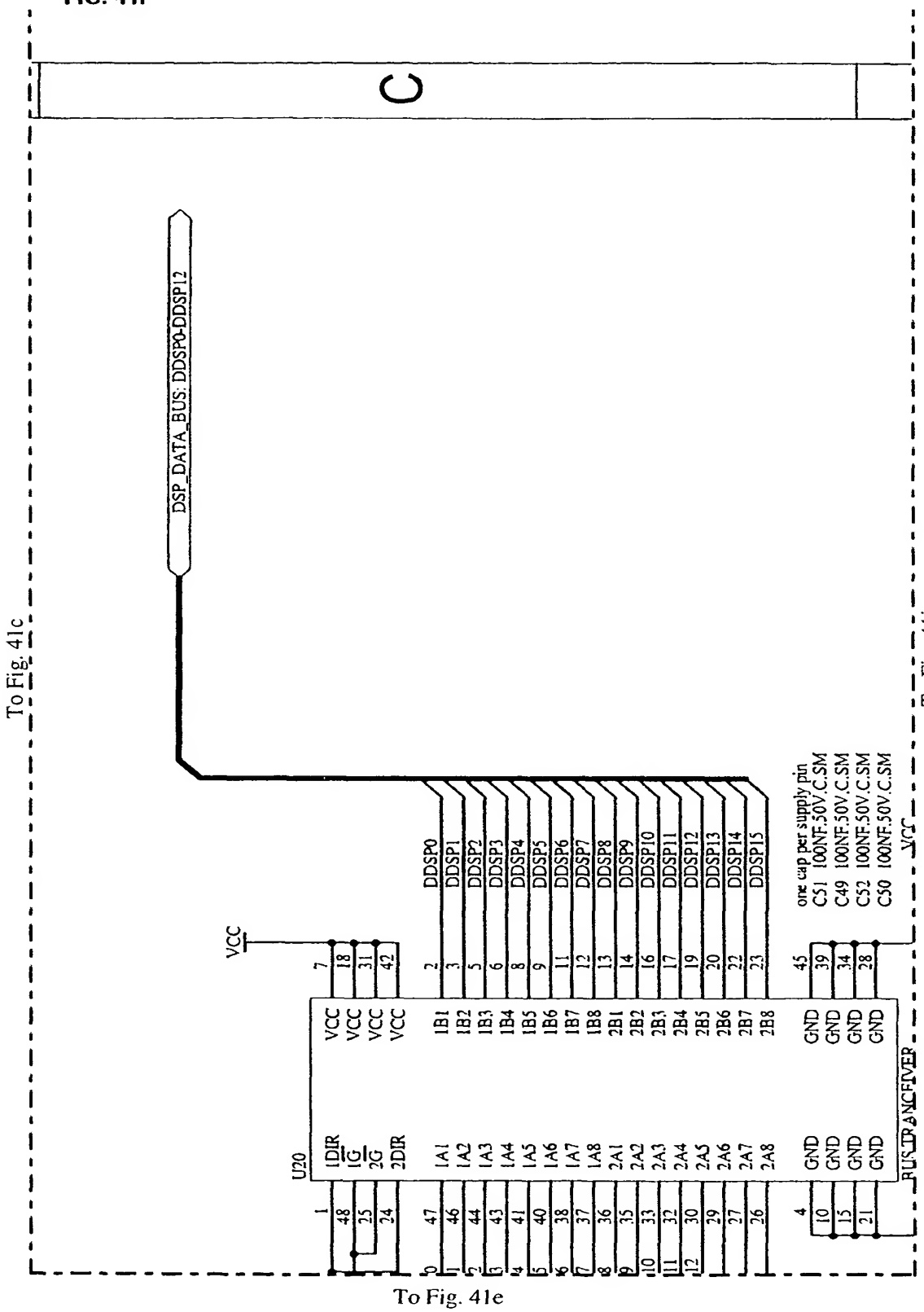

C
DSP_DATA_BUS: DDSP0-DDSP12
To Fig. 41c
To Fig. 41i
To Fig. 41e
VCC
U20
1DIR
1G
2G
2DIR
1A1
1A2
1A3
1A4
1A5
1A6
1A7
1A8
2A1
2A2
2A3
2A4
2A5
2A6
2A7
2A8
1B1
1B2
1B3
1B4
1B5
1B6
1B7
1B8
2B1
2B2
2B3
2B4
2B5
2B6
2B7
2B8
DDSP0
DDSP1
DDSP2
DDSP3
DDSP4
DDSP5
DDSP6
DDSP7
DDSP8
DDSP9
DDSP10
DDSP11
DDSP12
DDSP13
DDSP14
DDSP15
GND
one cap per supply pin
C51 100NF.50V.C.SM
C49 100NF.50V.C.SM
C52 100NF.50V.C.SM
C50 100NF.50V.C.SM
VCC

FIG. 41g

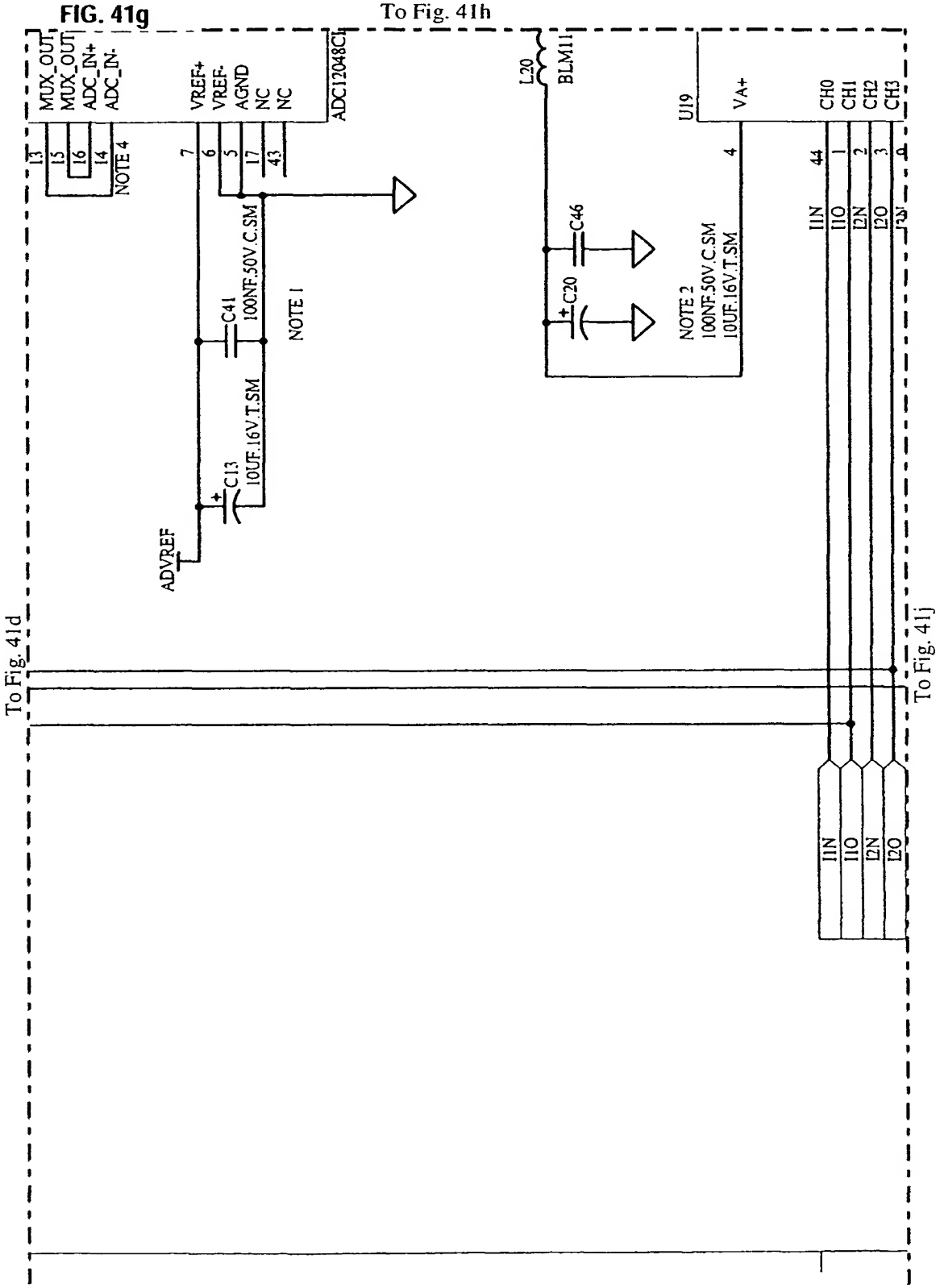

To Fig. 41h
To Fig. 41d
To Fig. 41j
ADC12048CI
MUX_OUT
MUX_OUT
ADC_IN+
ADC_IN-
VREF+
VREF-
AGND
NC
NC
NOTE 4
C41
100NF.50V.C.SM
NOTE 1
C13
10UF.16V.T.SM
ADVREF
L20
BLM11
C46
C20
U19
VA+
NOTE 2
100NF.50V.C.SM
10UF.16V.T.SM
CH0
CH1
CH2
CH3
I1N
I1O
I2N
I2O

FIG. 41h

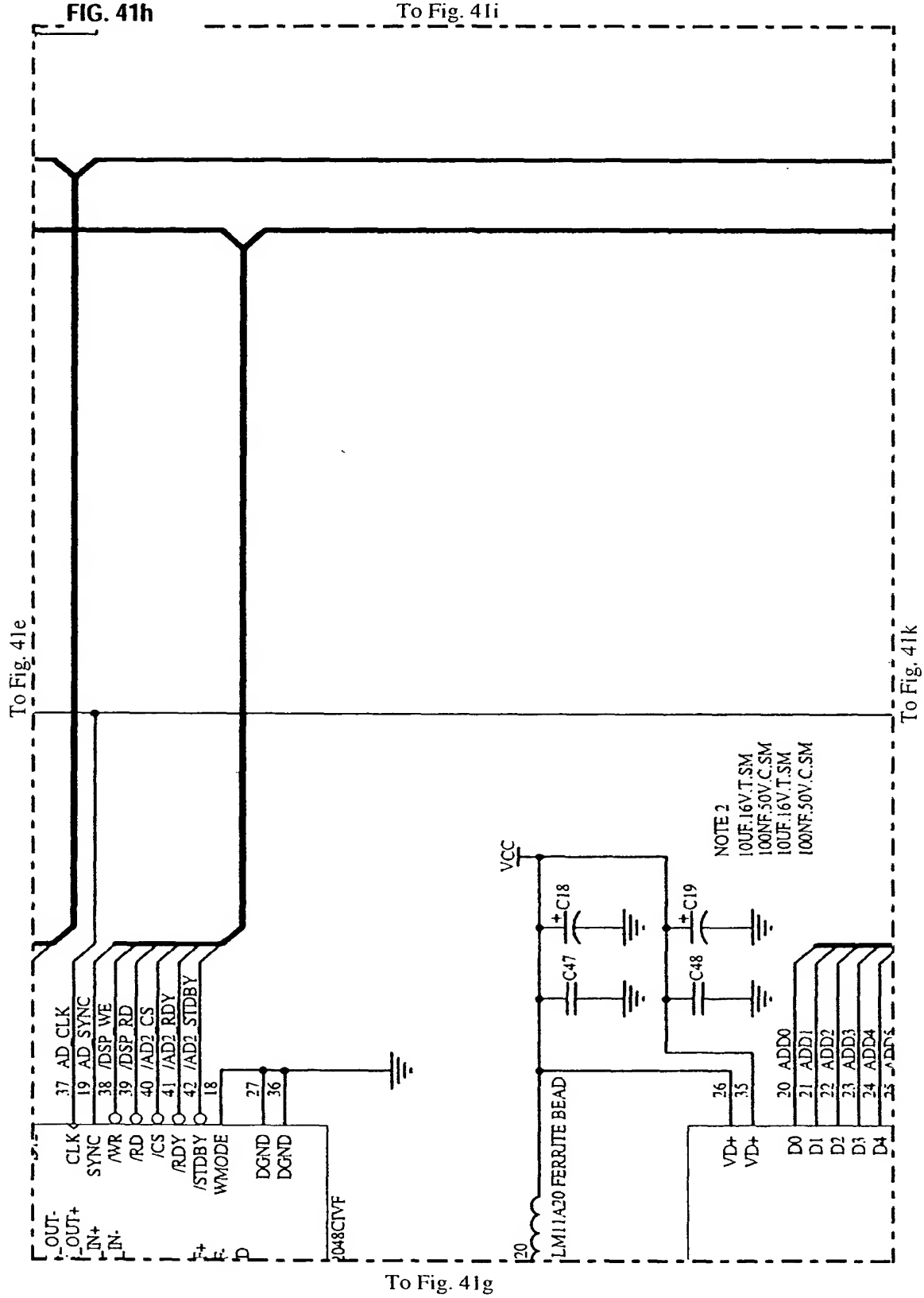
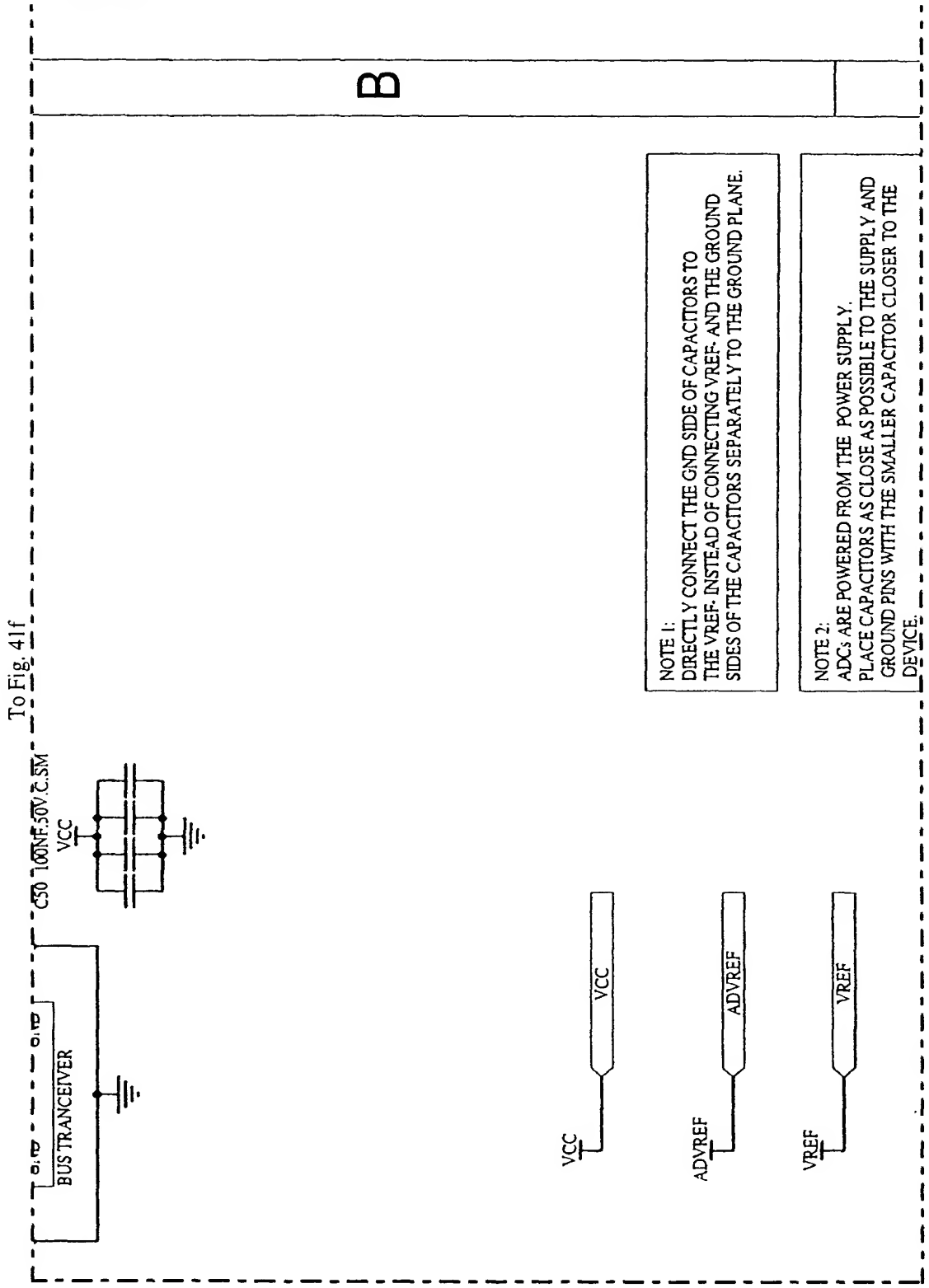

To Fig. 41i
To Fig. 41e
To Fig. 41k
To Fig. 41g
VCC
C18
C19
C47
C48
NOTE 2
10UF.16V.T.SM
100NF.50V.C.SM
10UF.16V.T.SM
100NF.50V.C.SM
37 AD_CLK
19 AD_SYNC
38 /DSP_WE
39 /DSP_RD
40 /AD2_CS
41 /AD2_RDY
42 /AD2_STDBY
18
27
36
CLK
SYNC
/WR
/RD
/CS
/RDY
/STDBY
WMODE
DGND
DGND
2048CTVF
OUT-
OUT+
IN+
IN-
LM11A20 FERRITE BEAD
20
26
35
VD+
VD+
20 ADD0
21 ADD1
22 ADD2
23 ADD3
24 ADD4
D0
D1
D2
D3
D4

FIG. 41i



To Fig. 41h

FIG. 41j

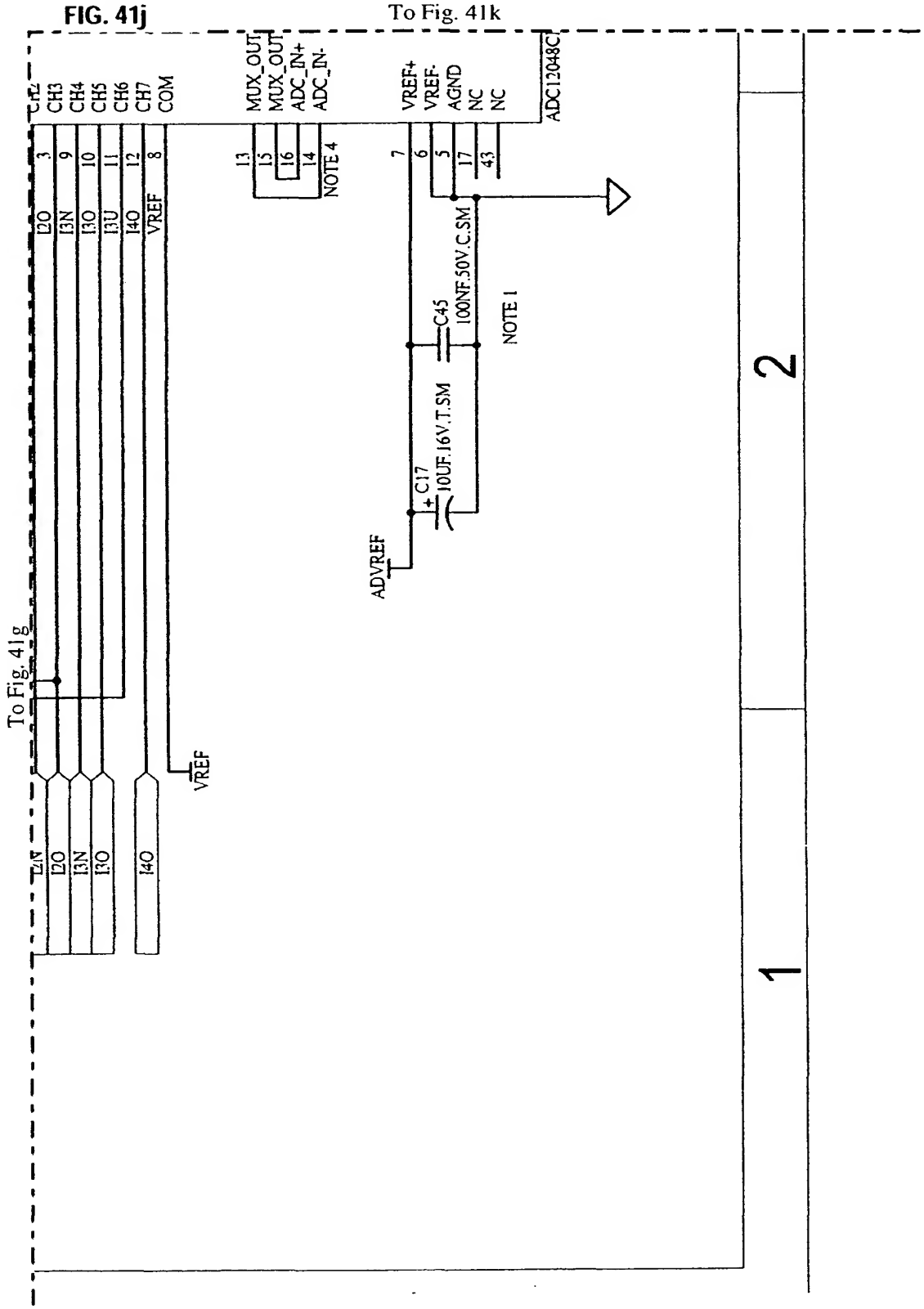

To Fig. 41k
To Fig. 41g
CH2
CH3
CH4
CH5
CH6
CH7
COM
MUX_OUT
MUX_OUT
ADC_IN+
ADC_IN-
VREF+
VREF-
AGND
NC
NC
ADC12048C
3
9
10
11
12
8
13
15
16
14
NOTE 4
7
6
5
17
43
I2O
I3N
I3O
I3U
I4O
VREF
C45
100NF.50V.C.SM
NOTE 1
C17
10UF.16V.T.SM
ADVREF
VREF
I4O
I3O
I3N
I2O
2
1

FIG. 41k

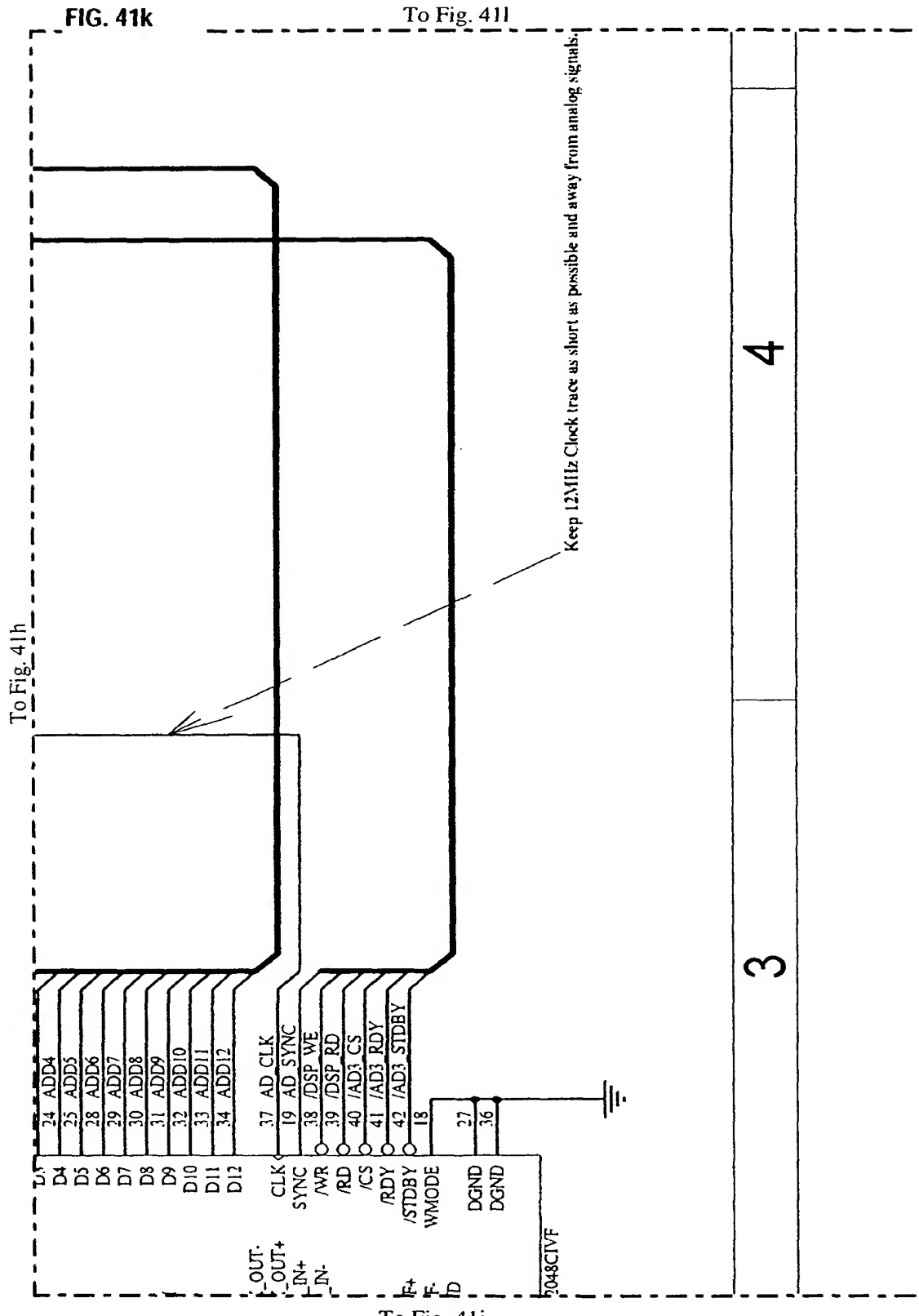

To Fig. 41l
Keep 12MHz Clock trace as short as possible and away from analog signals.
To Fig. 41h
4
3
24 ADD4
25 ADD5
28 ADD6
29 ADD7
30 ADD8
31 ADD9
32 ADD10
33 ADD11
34 ADD12
37 AD_CLK
19 AD_SYNC
38 /DSP_WE
39 /DSP_RD
40 /AD1_CS
41 /AD3_RDY
42 /AD3_STDBY
18
27
36
D4
D5
D6
D7
D8
D9
D10
D11
D12
CLK
SYNC
/WR
/RD
/CS
/RDY
/STDBY
WMODE
DGND
DGND
-OUT-
-OUT+
IN+
IN-
E+
E-
2048CIVF
To Fig. 41j

FIG. 41l

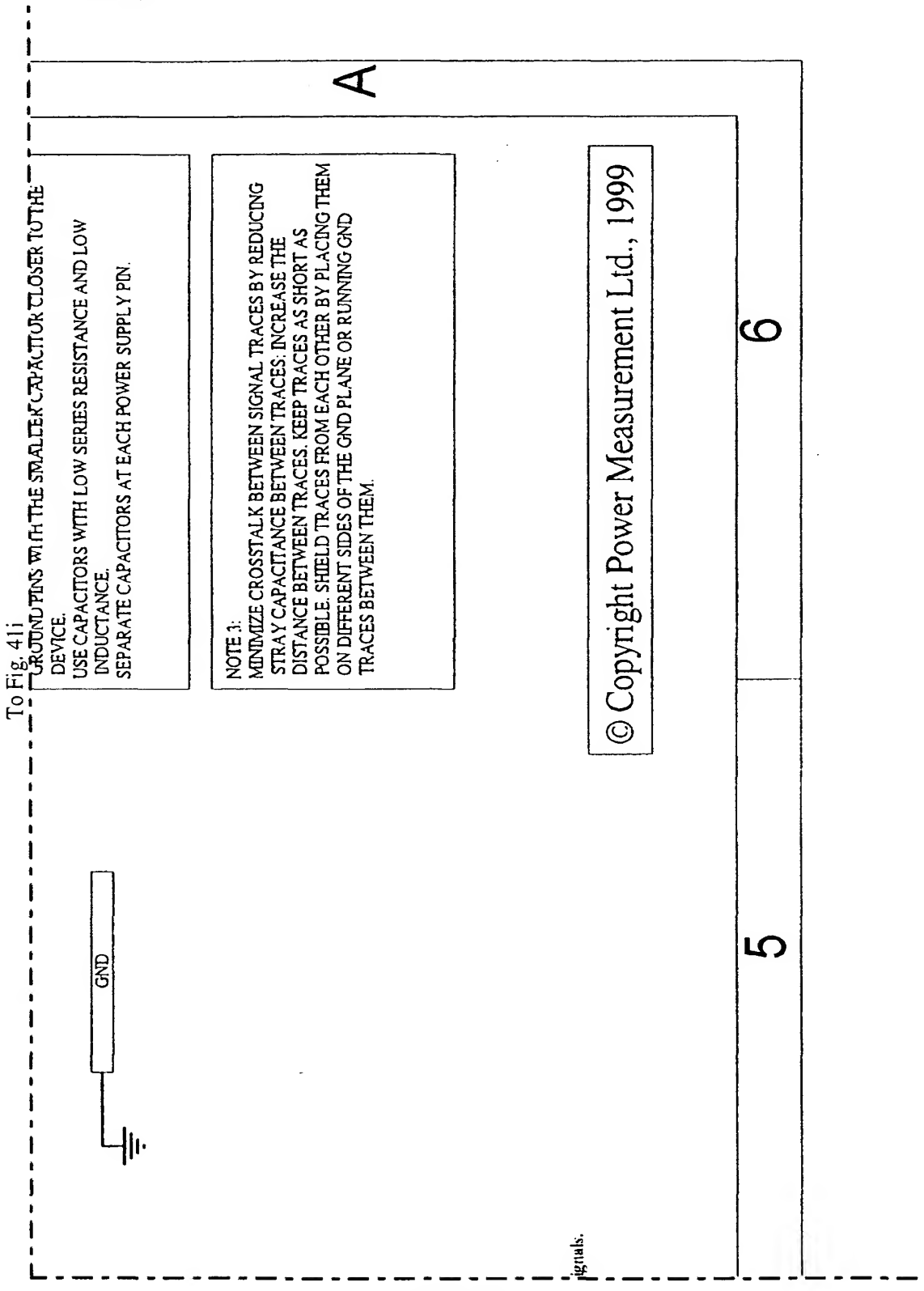

To Fig. 41i
GROUND PINS WITH THE SMALLER CAPACITOR CLOSER TO THE DEVICE.
USE CAPACITORS WITH LOW SERIES RESISTANCE AND LOW INDUCTANCE.
SEPARATE CAPACITORS AT EACH POWER SUPPLY PIN.
NOTE 3:
MINIMIZE CROSSTALK BETWEEN SIGNAL TRACES BY REDUCING STRAY CAPACITANCE BETWEEN TRACES. INCREASE THE DISTANCE BETWEEN TRACES. KEEP TRACES AS SHORT AS POSSIBLE. SHIELD TRACES FROM EACH OTHER BY PLACING THEM ON DIFFERENT SIDES OF THE GND PLANE OR RUNNING GND TRACES BETWEEN THEM.
GND
© Copyright Power Measurement Ltd., 1999
A
6
5
signals.
To Fig. 41k

FIG. 42a

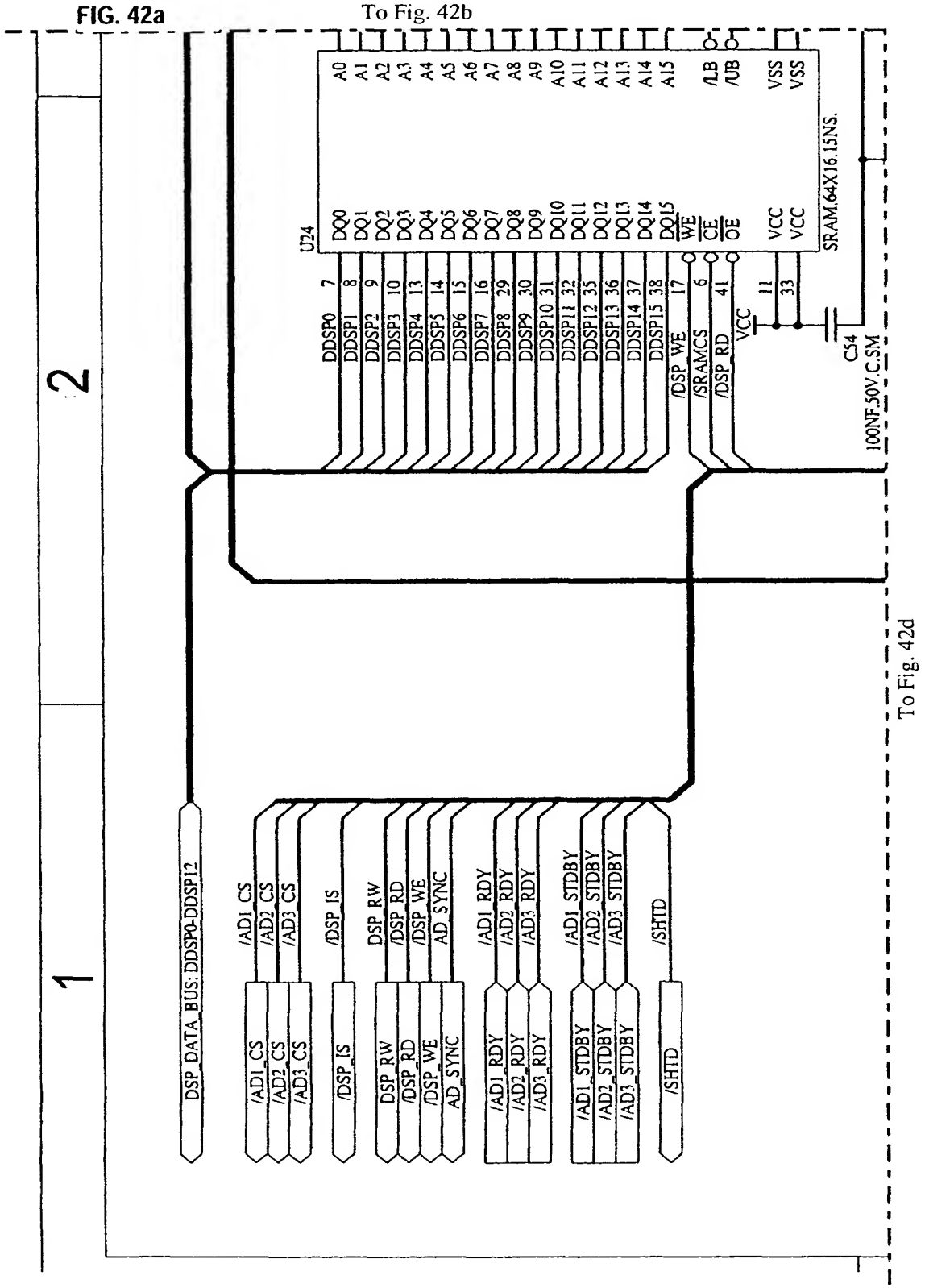

To Fig. 42b
U24
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
/LB
/UB
VSS
VSS
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
WE
CE
OE
VCC
VCC
SRAM.64X16.15NS.
DDSP0 7
DDSP1 8
DDSP2 9
DDSP3 10
DDSP4 13
DDSP5 14
DDSP6 15
DDSP7 16
DDSP8 29
DDSP9 30
DDSP10 31
DDSP11 32
DDSP12 35
DDSP13 36
DDSP14 37
DDSP15 38
/DSP_WE 17
/SRAMCS 6
/DSP_RD 41
VCC 11
33
C54
100NF.50V.C.SM
2
1
DSP_DATA_BUS:DDSP0-DDSP12
/AD1_CS
/AD2_CS
/AD3_CS
/DSP_IS
DSP_RW
/DSP_RD
/DSP_WE
AD_SYNC
/AD1_RDY
/AD2_RDY
/AD3_RDY
/AD1_STDBY
/AD2_STDBY
/AD3_STDBY
/SHTD
To Fig. 42d

FIG. 42b

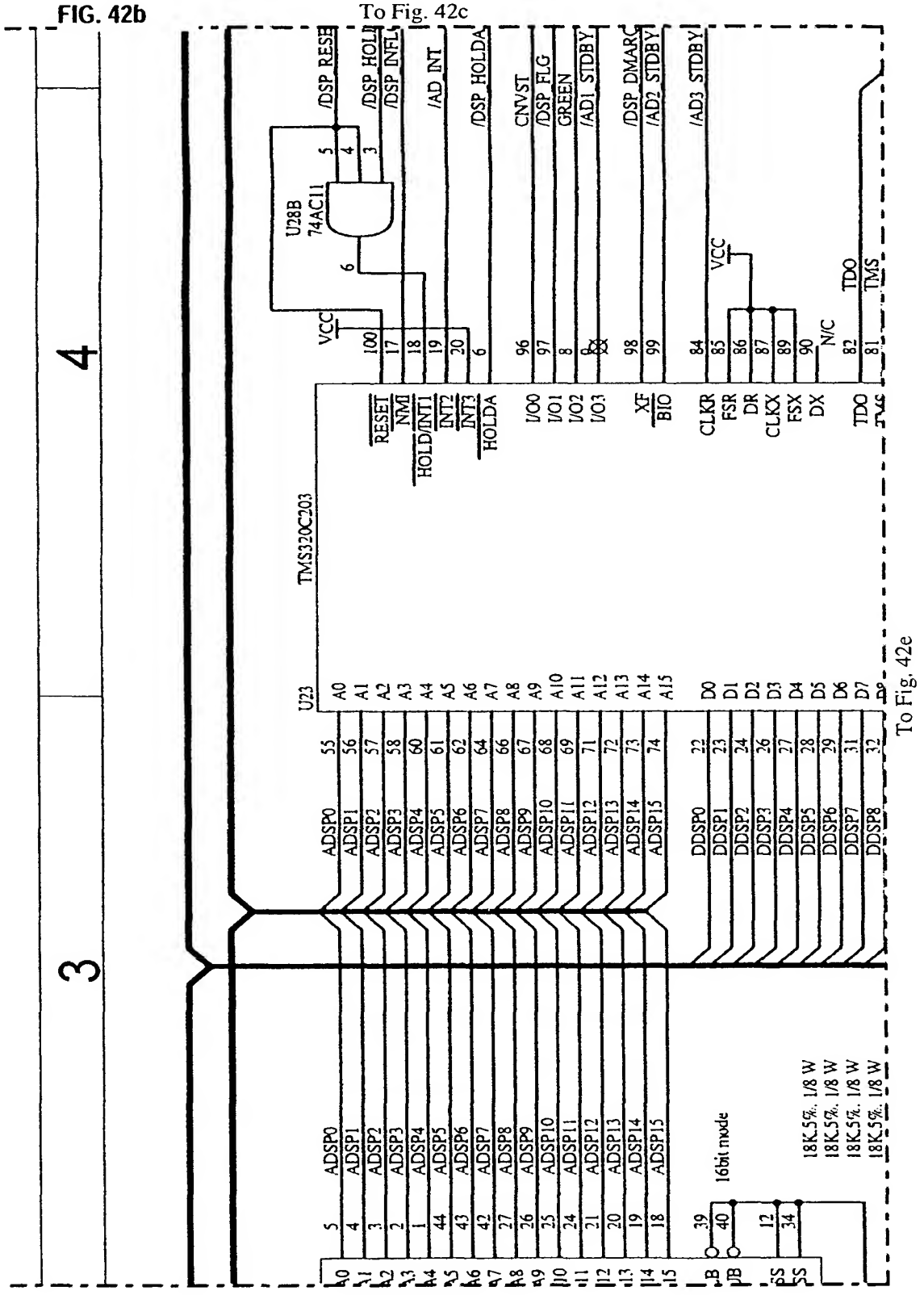

To Fig. 42c
/DSP RESET
/DSP HOLD
/DSP INFL
/AD INT
/DSP HOLDA
CNVST
/DSP FLG
GREEN
/AD1 STDBY
/DSP DMARQ
/AD2 STDBY
/AD3 STDBY
VCC
TDO
TMS
U28B
74AC11
TMS320C203
U23
RESET
NMI
HOLD/INT1
INT2
INT3
HOLDA
I/O0
I/O1
I/O2
I/O3
XF
BIO
CLKR
FSR
DR
CLKX
FSX
DX
TDO
N/C
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
ADSP0
ADSP1
ADSP2
ADSP3
ADSP4
ADSP5
ADSP6
ADSP7
ADSP8
ADSP9
ADSP10
ADSP11
ADSP12
ADSP13
ADSP14
ADSP15
DDSP0
DDSP1
DDSP2
DDSP3
DDSP4
DDSP5
DDSP6
DDSP7
DDSP8
16bit mode
18K.5%. 1/8 W
18K.5%. 1/8 W
18K.5%. 1/8 W
18K.5%. 1/8 W
To Fig. 42e
To Fig. 42a

FIG. 42c

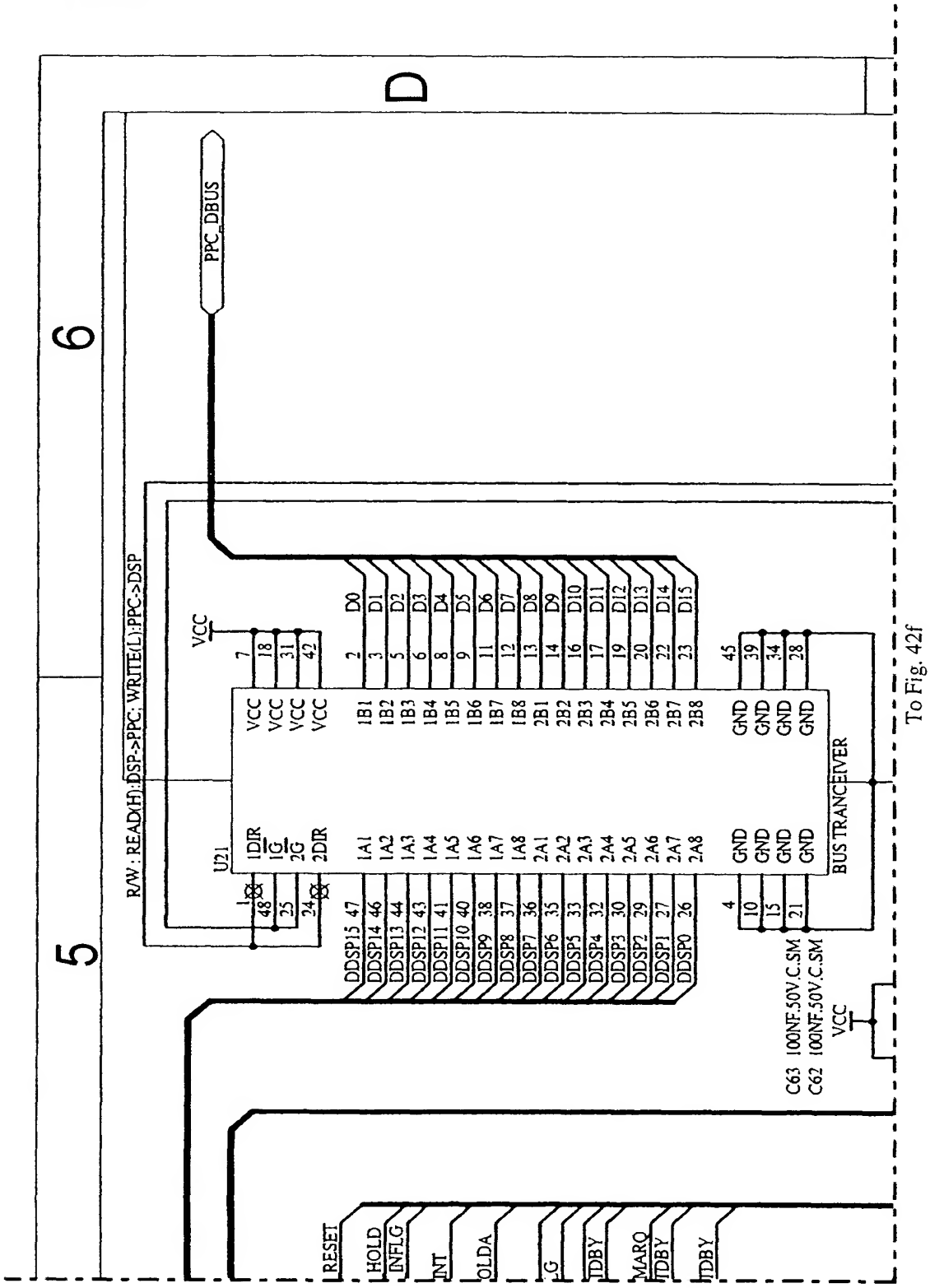

D
6
5
PPC_DBUS
R/W : READ(H):DSP->PPC; WRITE(L):PPC->DSP
U21
1DIR
1G
2G
2DIR
BUS TRANCEIVER
VCC
GND
C63 100NF.50V.C.SM
C62 100NF.50V.C.SM
RESET
HOLD
INFLG
INT
QLDA
TDBY
MARQ
To Fig. 42f
To Fig. 42b

FIG. 42d

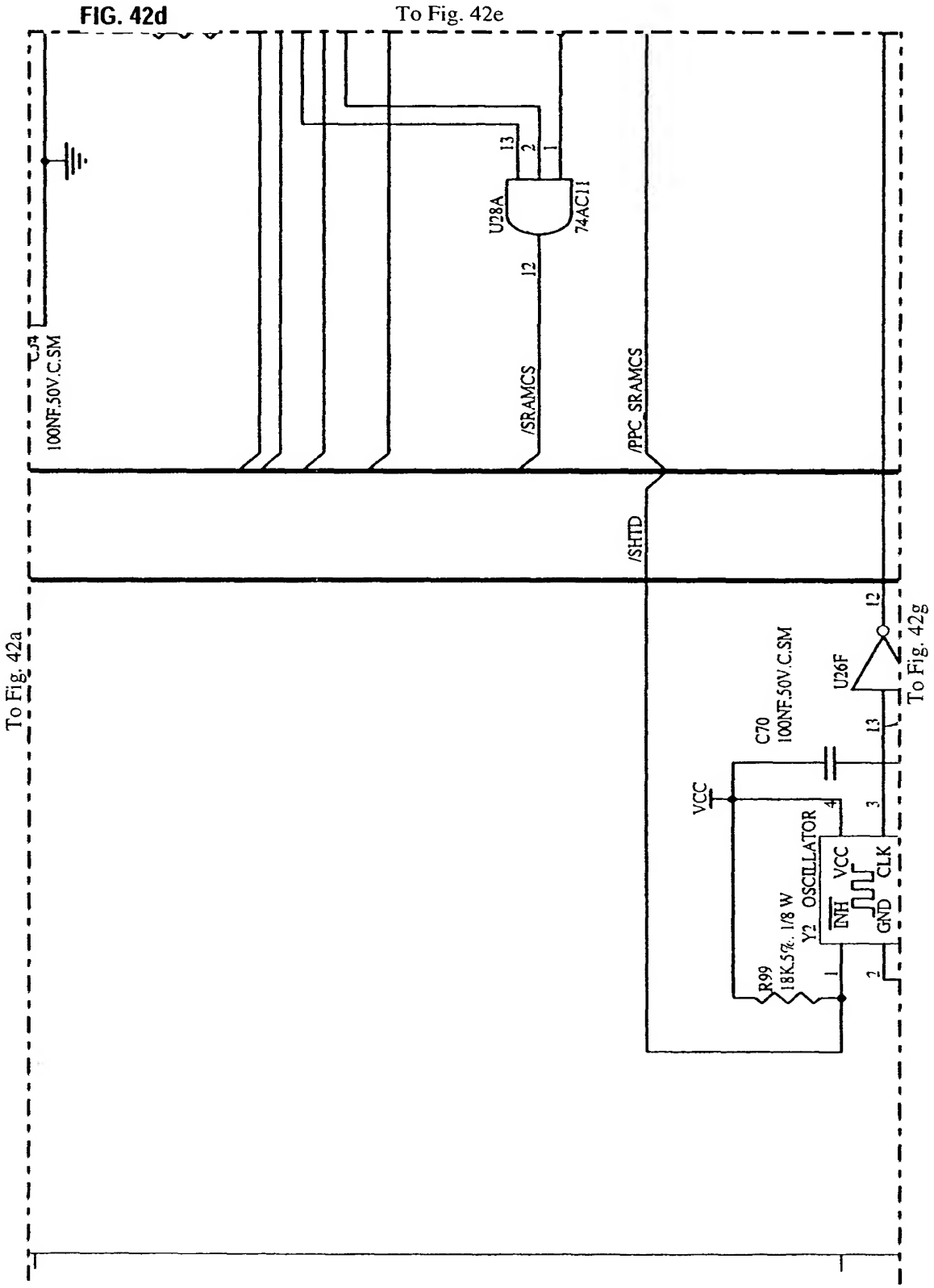

To Fig. 42e
To Fig. 42a
To Fig. 42g
U28A
74AC11
13
2
1
12
C54
100NF.50V.C.SM
/SRAMCS
/PPC_SRAMCS
/SHTD
U26F
12
13
C70
100NF.50V.C.SM
VCC
4
3
Y2 OSCILLATOR
INH
VCC
GND
CLK
R99
18K.5%. 1/8 W
1
2

FIG. 42e

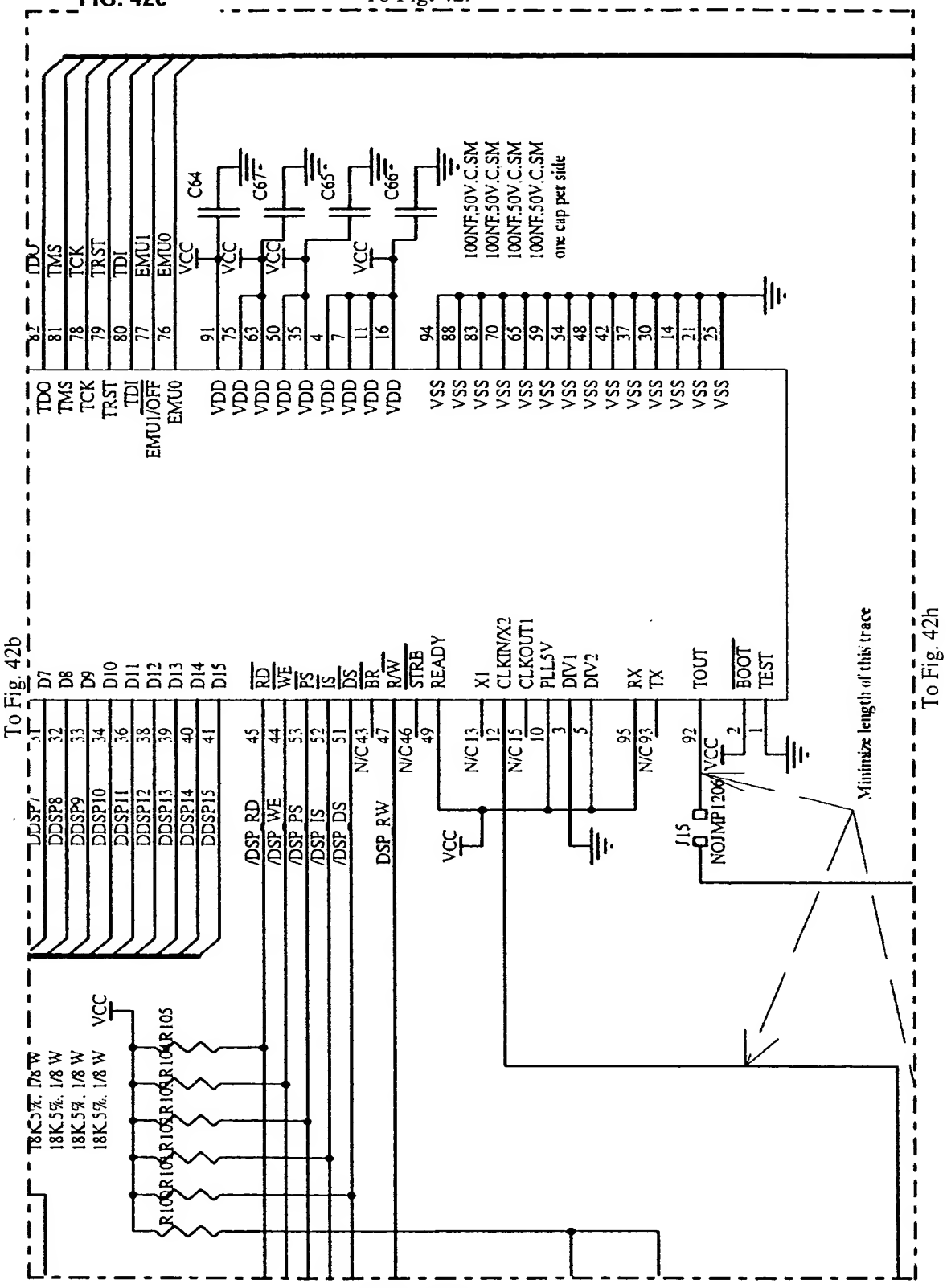

To Fig. 42f
To Fig. 42b
To Fig. 42h
To Fig. 42d
TDO
TMS
TCK
TRST
TDI
EMU1
EMU0
VCC
C64
C67
C65
C66
100NF.50V.C.SM
one cap per side
VDD
VSS
D7
D8
D9
D10
D11
D12
D13
D14
D15
RD
WE
PS
IS
DS
BR
R/W
STRB
READY
X1
CLKIN/X2
CLKOUT1
PLL5V
DIV1
DIV2
RX
TX
TOUT
BOOT
TEST
/DSP RD
/DSP WE
/DSP PS
/DSP IS
/DSP DS
DSP R/W
N/C
VCC
J15
NOJMP1206
Minimize length of this trace
18K5%. 1/8 W
R100
R105

FIG. 42f

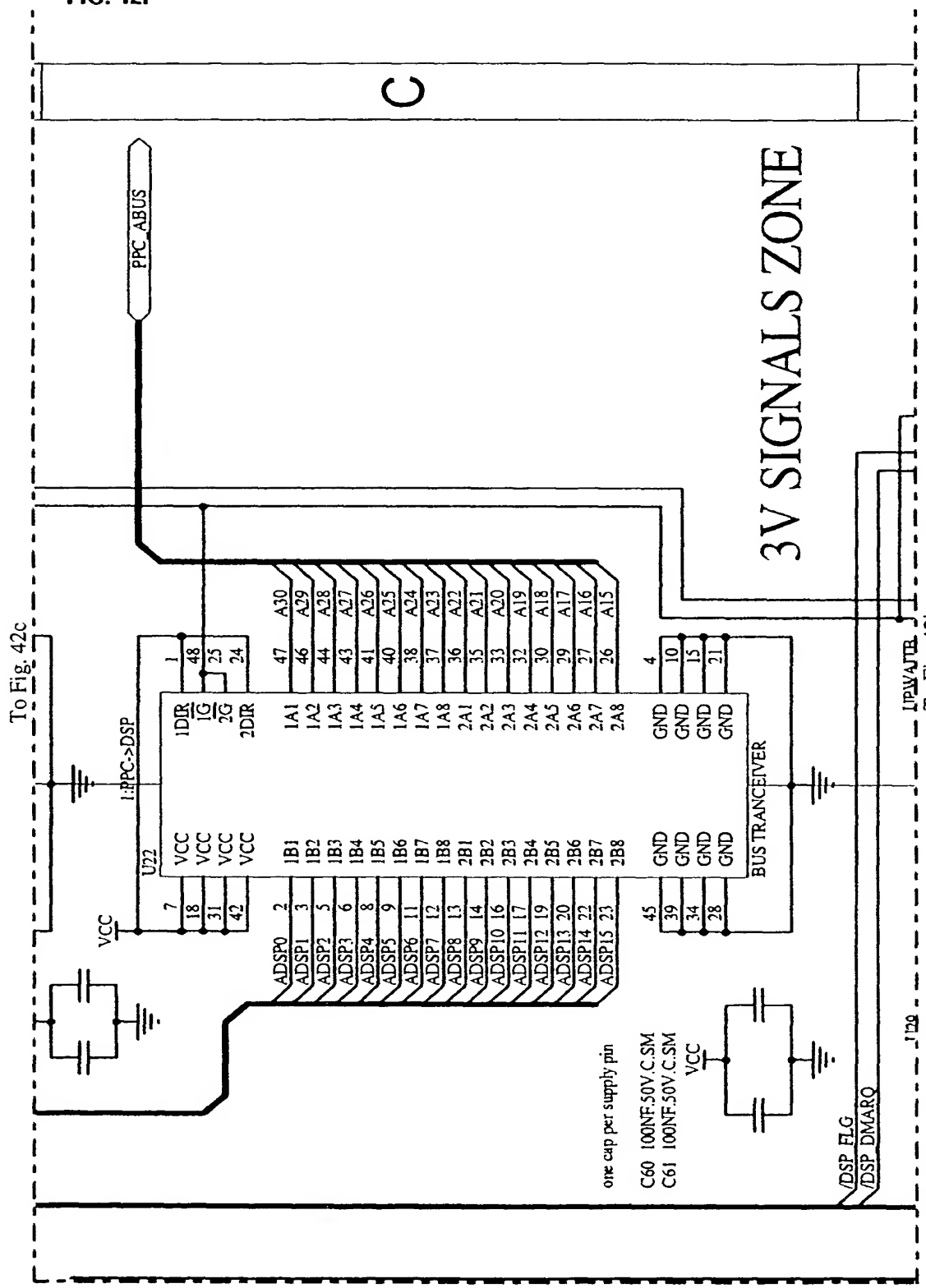

C
3V SIGNALS ZONE
PPC_ABUS
To Fig. 42c
To Fig. 42i
To Fig. 42e
U22
BUS TRANCEIVER
1DIR
1G
2G
2DIR
1:PPC->DSP
VCC
GND
C60 100NF.50V.C.SM
C61 100NF.50V.C.SM
one cap per supply pin
/DSP FLG
/DSP DMARQ

FIG. 42g

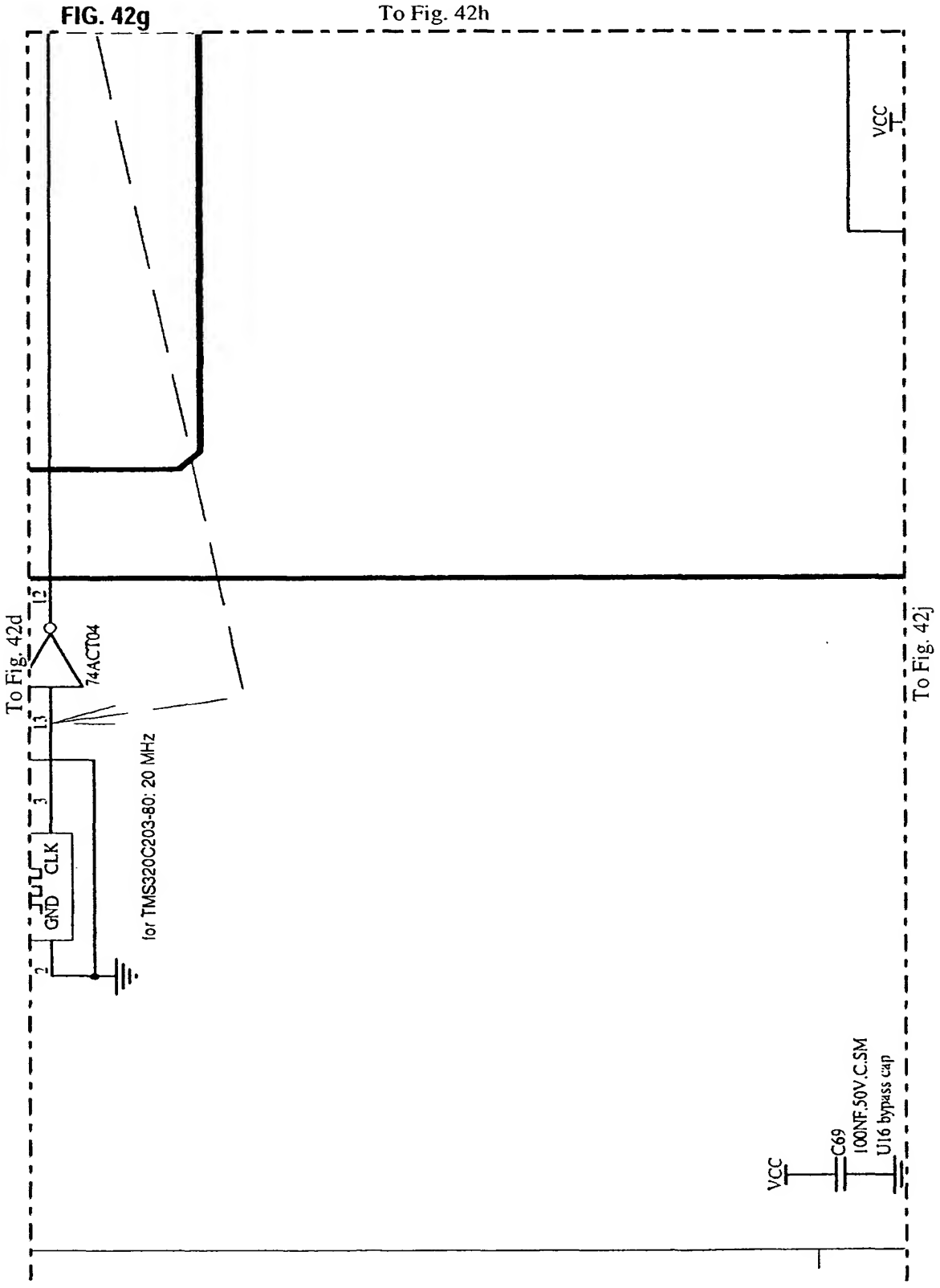

To Fig. 42h
VCC
To Fig. 42d
12
74ACT04
13
3
GND CLK
2
for TMS320C203-80: 20 MHz
To Fig. 42j
VCC
C69
100NF.50V.C.SM
U16 bypass cap

FIG. 42h

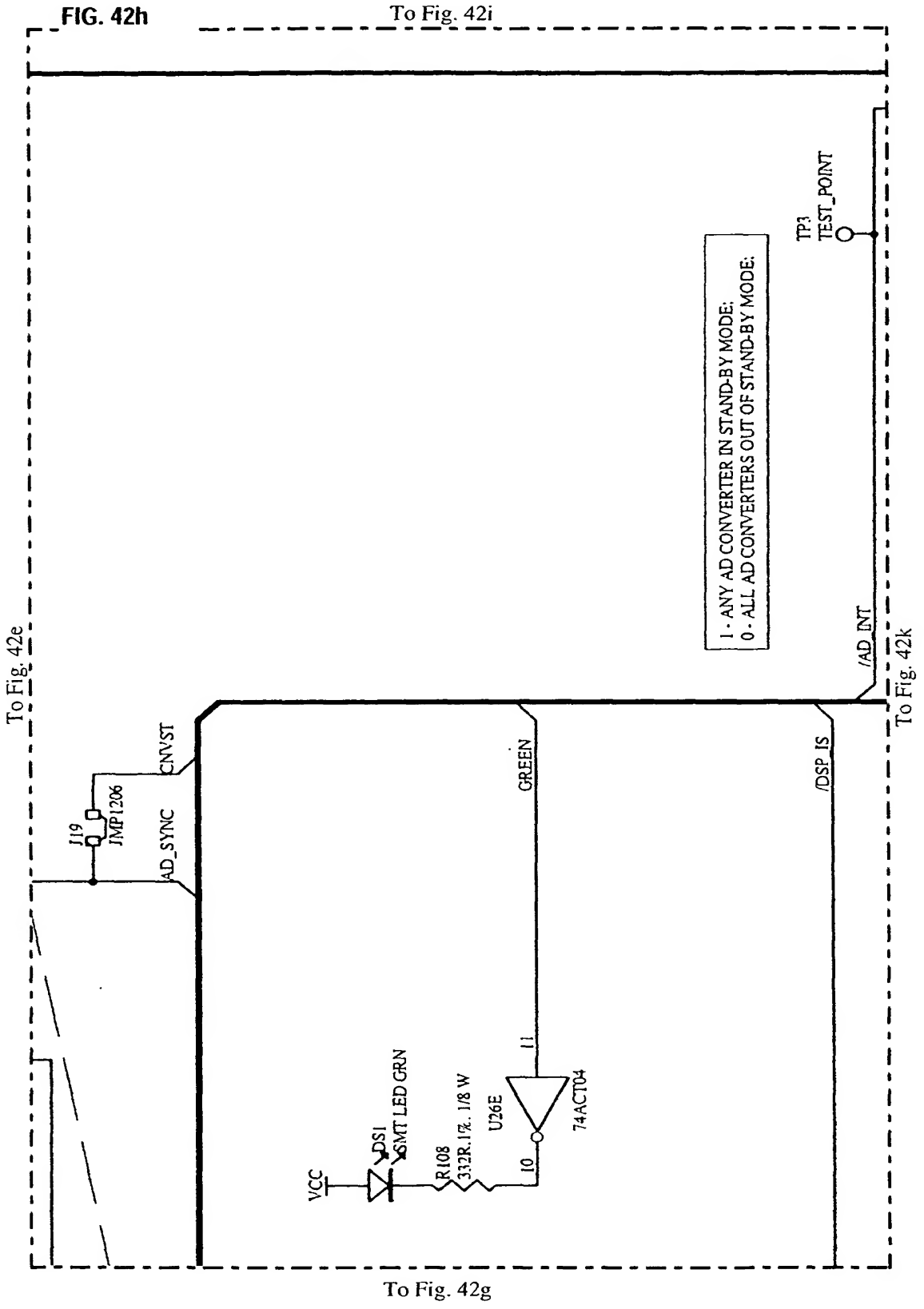

To Fig. 42i
To Fig. 42e
To Fig. 42k
To Fig. 42g
TP3
TEST_POINT
1 - ANY AD CONVERTER IN STAND-BY MODE;
0 - ALL AD CONVERTERS OUT OF STAND-BY MODE;
/AD_INT
/DSP_IS
GREEN
CNVST
AD_SYNC
J19
JMP1206
DS1
SMT LED GRN
R108
332R.1%, 1/8 W
U26E
74ACT04
11
10
VCC

FIG. 42i

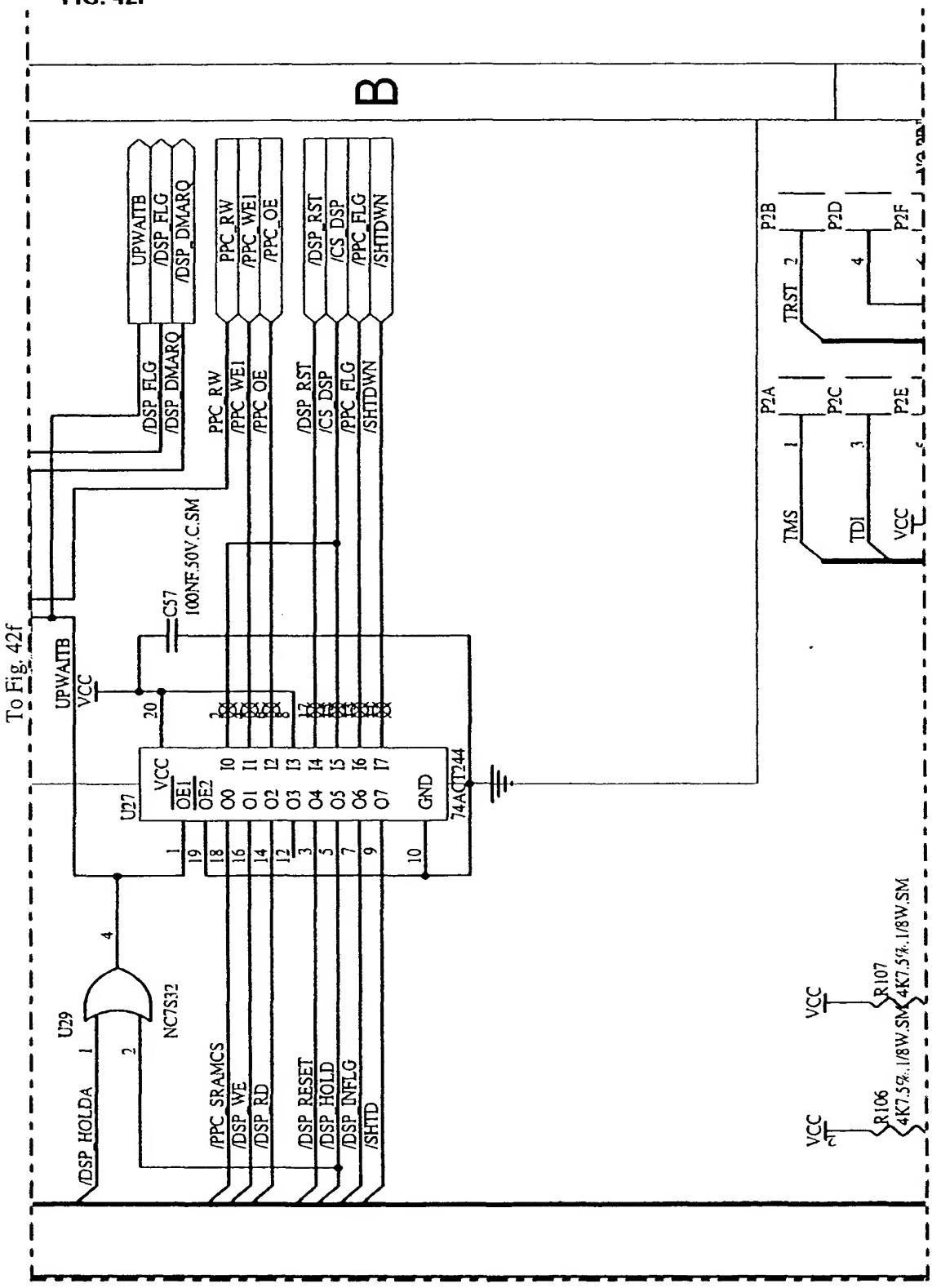

B
UPWAITB
/DSP_FLG
/DSP_DMARQ
PPC_RW
/PPC_WE1
/PPC_OE
/DSP_RST
/CS_DSP
/PPC_FLG
/SHTDWN
P2B
P2D
P2F
TRST
P2A
P2C
P2E
TMS
TDI
VCC
C57
100NF.50V.C.SM
U27
74ACT244
GND
U29
NC7S32
/DSP_HOLDA
/PPC_SRAMCS
/DSP_WE
/DSP_RD
/DSP_RESET
/DSP_HOLD
/DSP_INFLG
/SHTD
R107
4K7.5%.1/8W.SM
R106
4K7.5%.1/8W.SM
To Fig. 42f
To Fig. 42l
To Fig. 42h

FIG. 42j

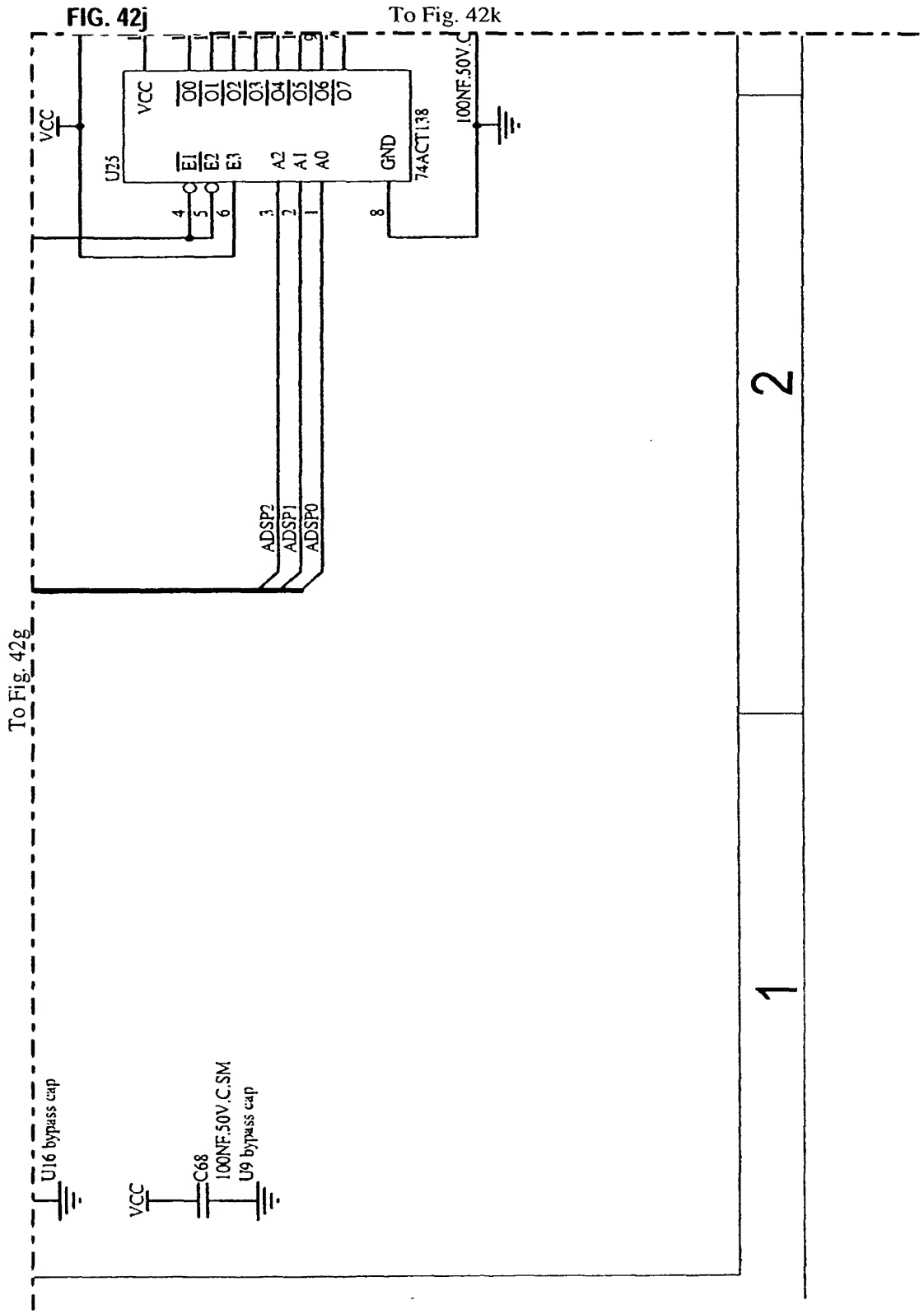
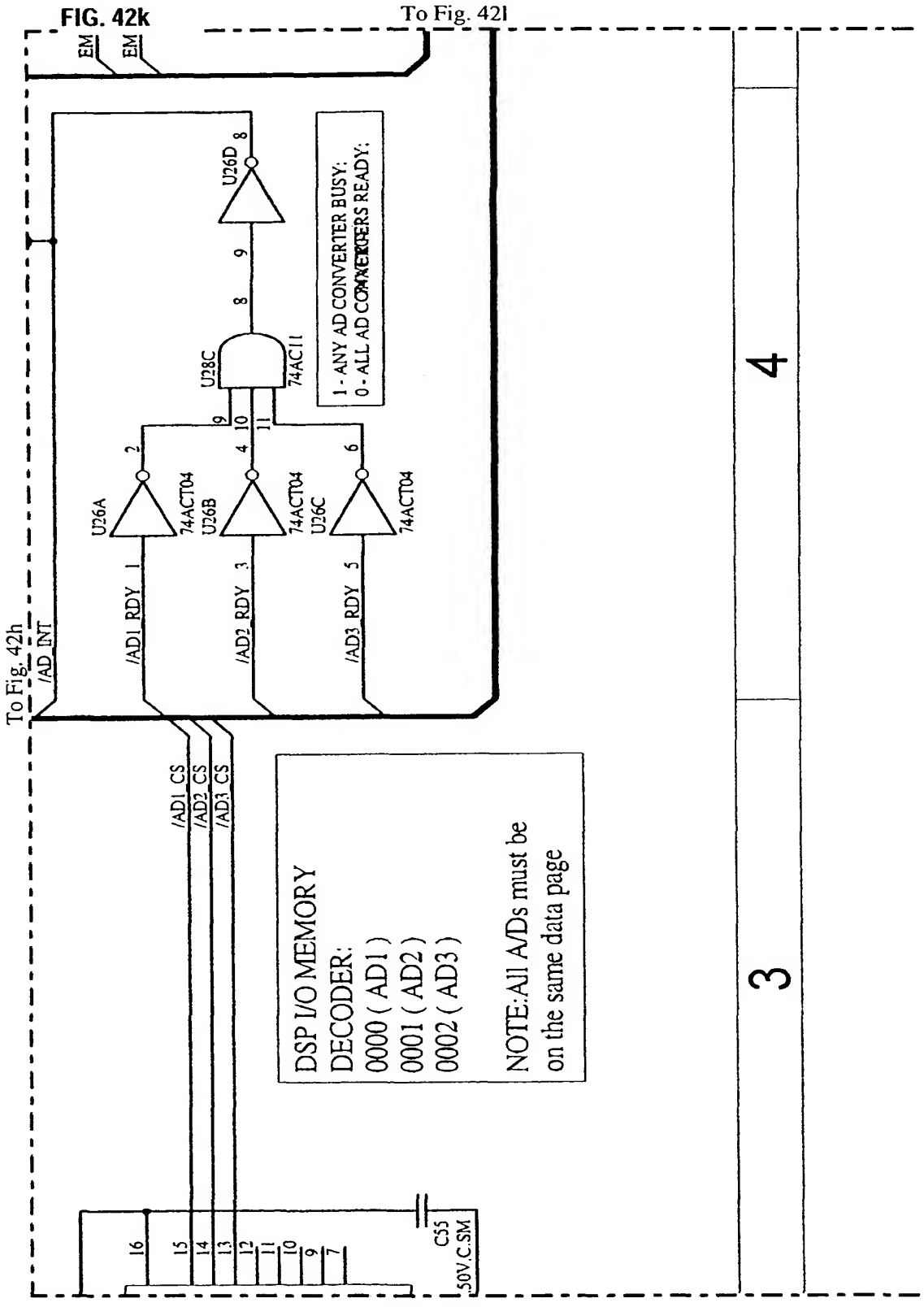

To Fig. 42k
To Fig. 42g
VCC
U25
VCC
O0
O1
O2
O3
O4
O5
O6
O7
E1
E2
E3
A2
A1
A0
GND
74ACT138
100NF.50V.C
ADSP2
ADSP1
ADSP0
U16 bypass cap
C68
100NF.50V.C.SM
U9 bypass cap
2
1

FIG. 42k



To Fig. 42j

FIG. 42I

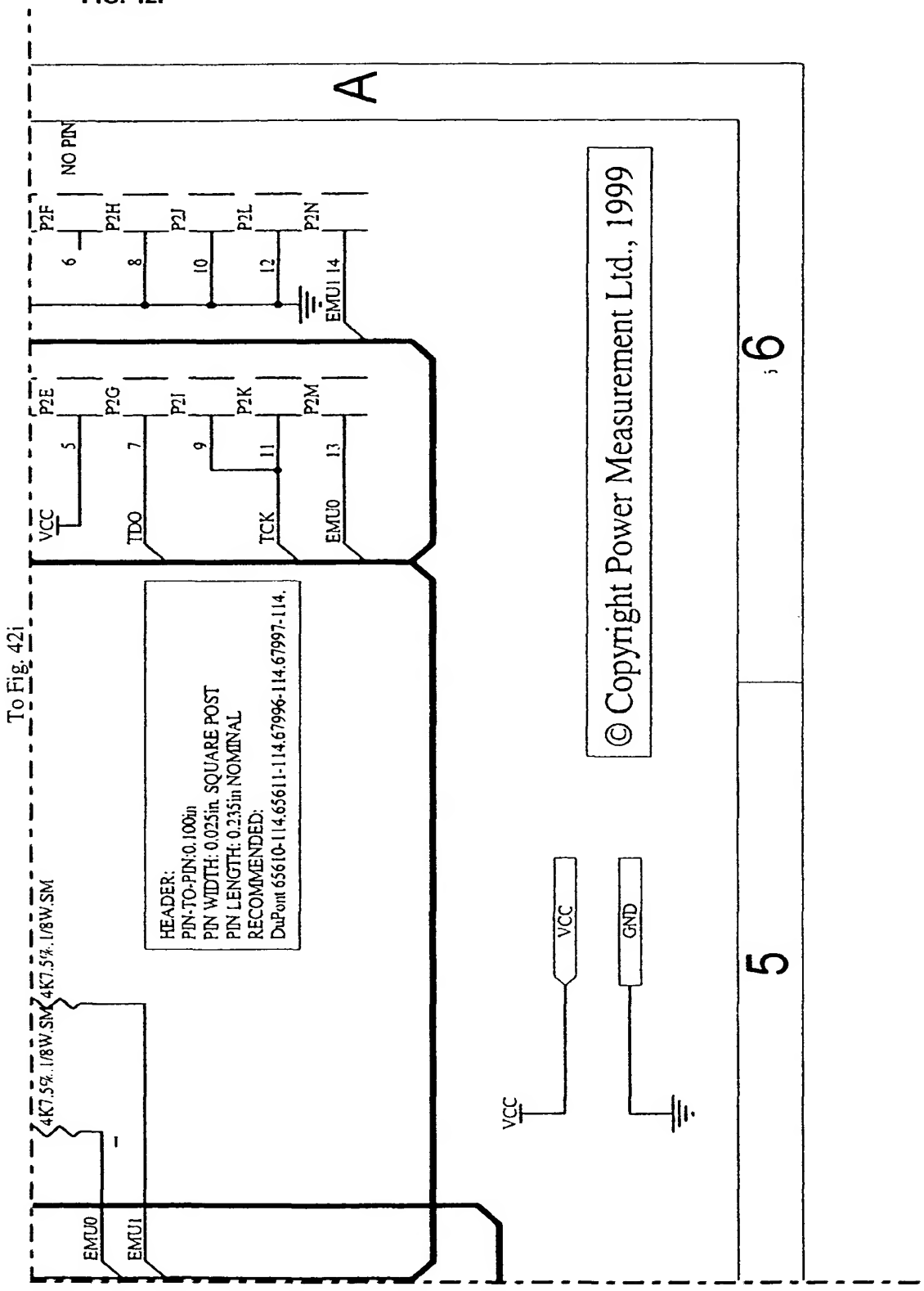

A
NO PIN
P2F
P2H
P2J
P2L
P2N
6
8
10
12
EMU1 14
P2E
P2G
P2I
P2K
P2M
5
7
9
11
13
VCC
TDO
TCK
EMU0
HEADER:
PIN-TO-PIN:0.100in
PIN WIDTH: 0.025in. SQUARE POST
PIN LENGTH: 0.235in NOMINAL
RECOMMENDED:
DuPont 65610-114,65611-114,67996-114,67997-114.
© Copyright Power Measurement Ltd., 1999
6
5
VCC
GND
VCC
4K7.5%..1/8W.SM
4K7.5%..1/8W.SM
4K7.5%..1/8W.SM
EMU0
EMU1
To Fig. 42i
To Fig. 42k

FIG. 43a

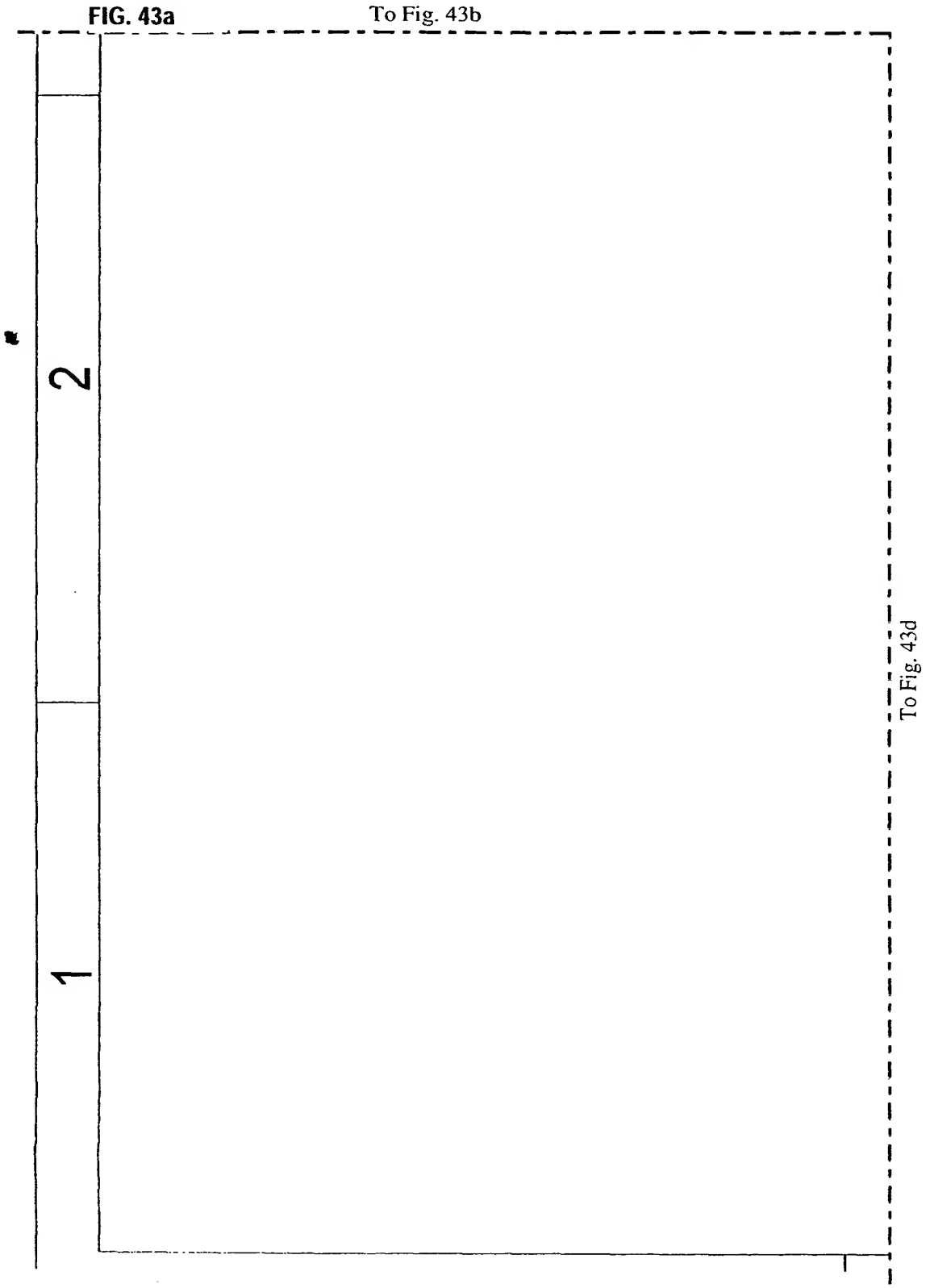


FIG. 43b

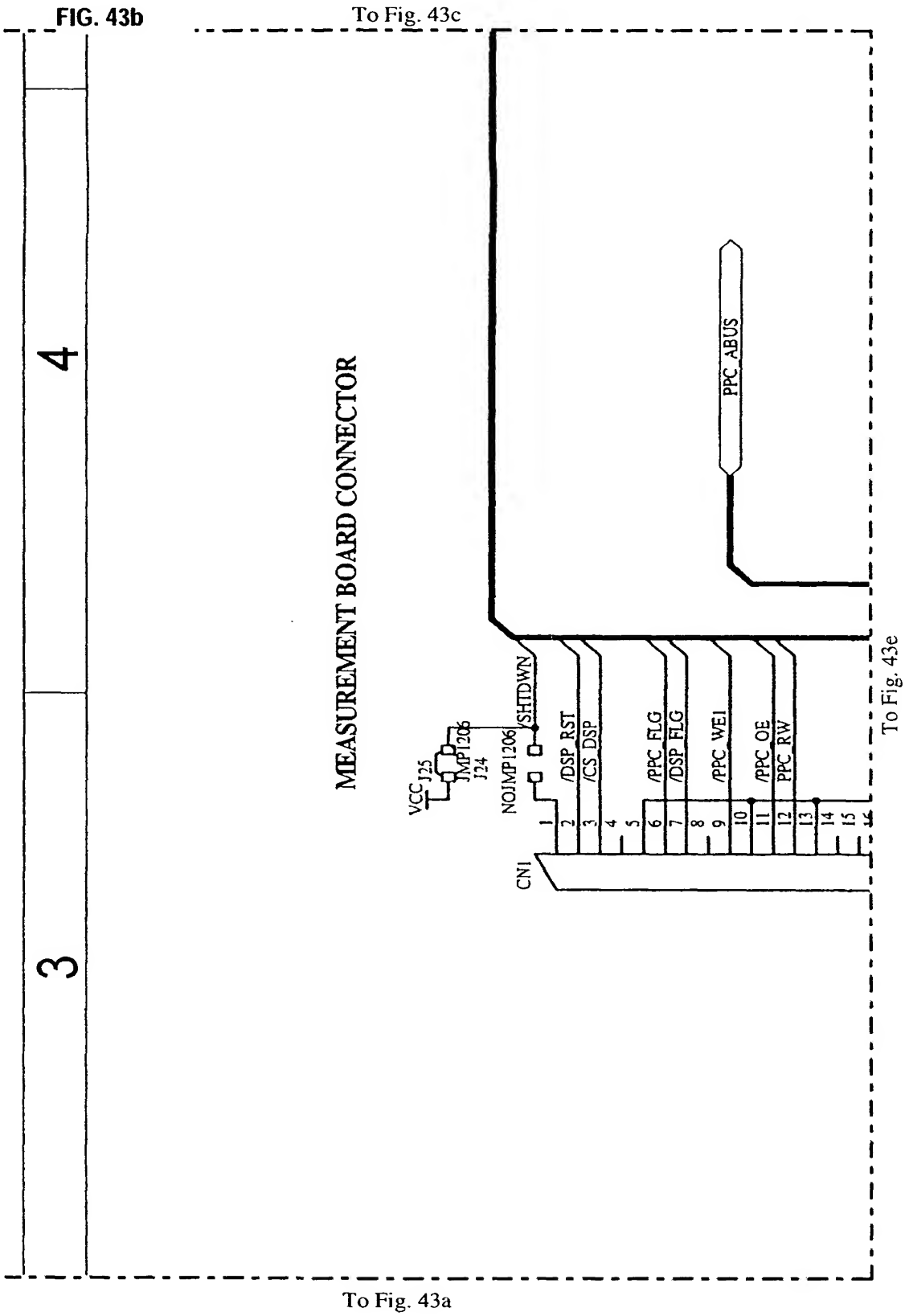

To Fig. 43c
4
3
MEASUREMENT BOARD CONNECTOR
PPC_ABUS
VCC
J25
JMP1206
J24
NOJMP1206
/SHTDWN
/DSP_RST
/CS_DSP
/PPC_FLG
/DSP_FLG
/PPC_WEI
/PPC_OE
PPC_RW
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
CN1
To Fig. 43e
To Fig. 43a

FIG. 43c

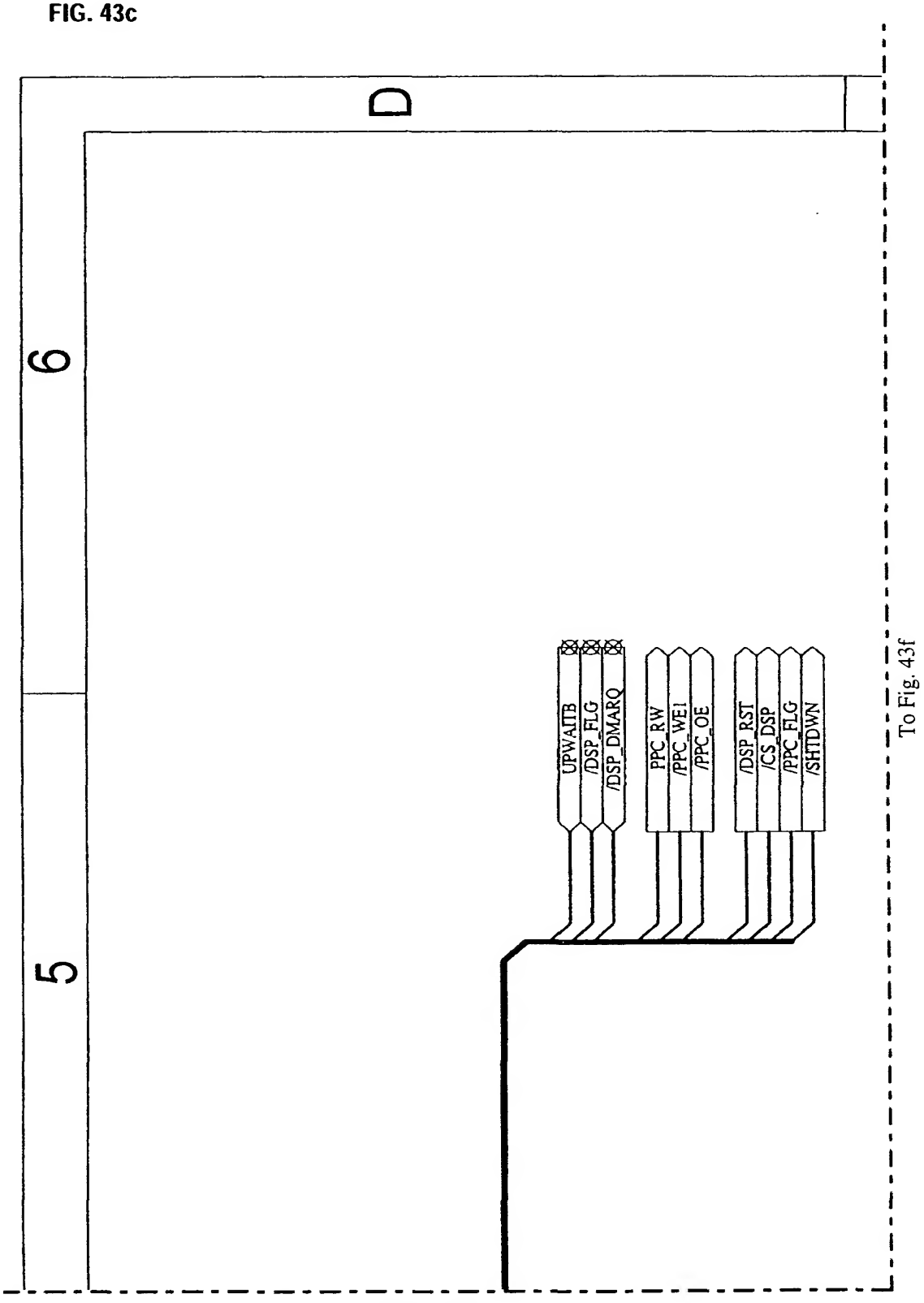
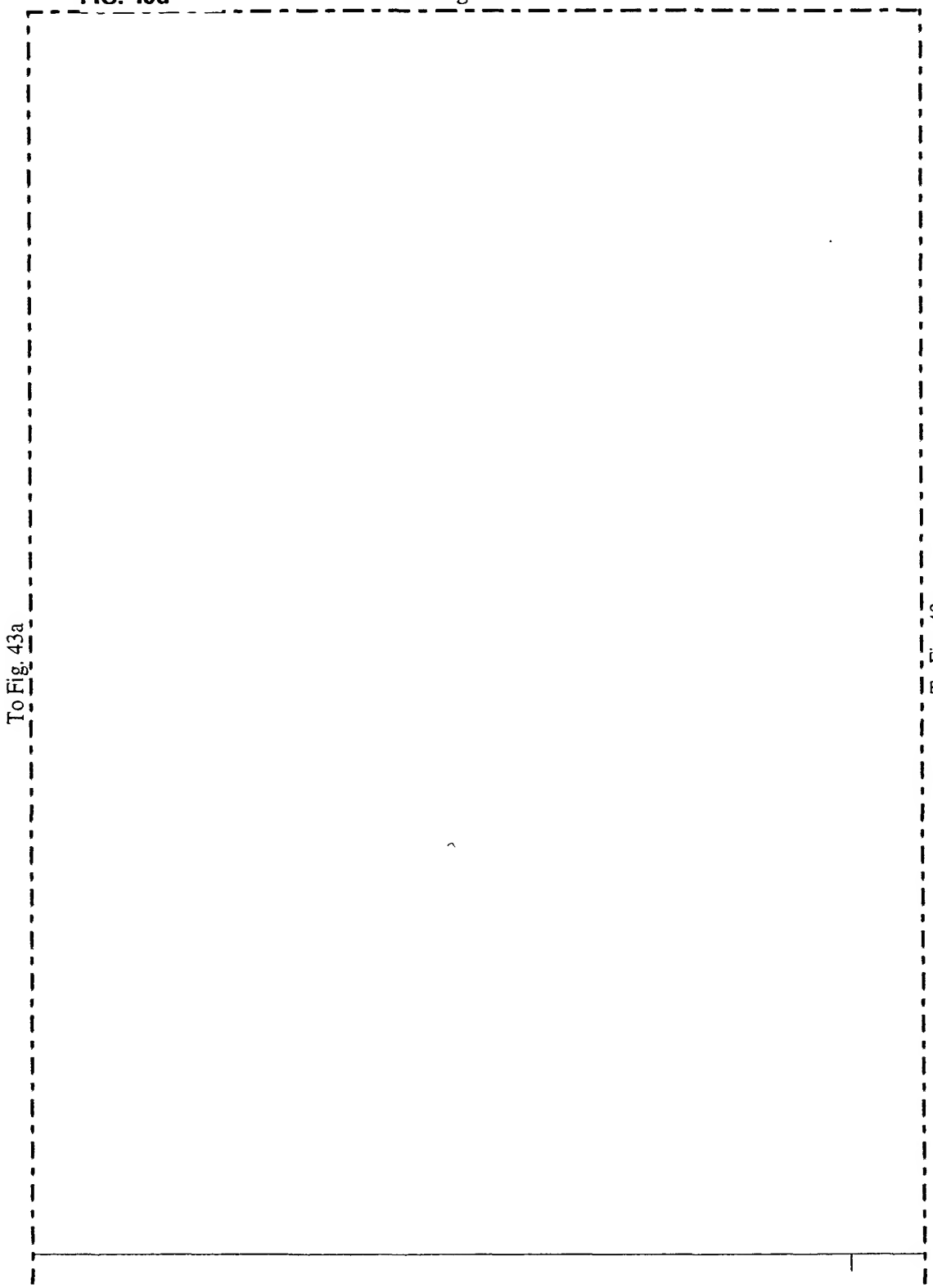

D
6
5
UPWAITB
/DSP_FLG
/DSP_DMARQ
PPC_RW
/PPC_WE1
/PPC_OE
/DSP_RST
/CS_DSP
/PPC_FLG
/SHTDWN
To Fig. 43f
To Fig. 43b

FIG. 43d

To Fig. 43e



To Fig. 43a

To Fig. 43g

FIG. 43e

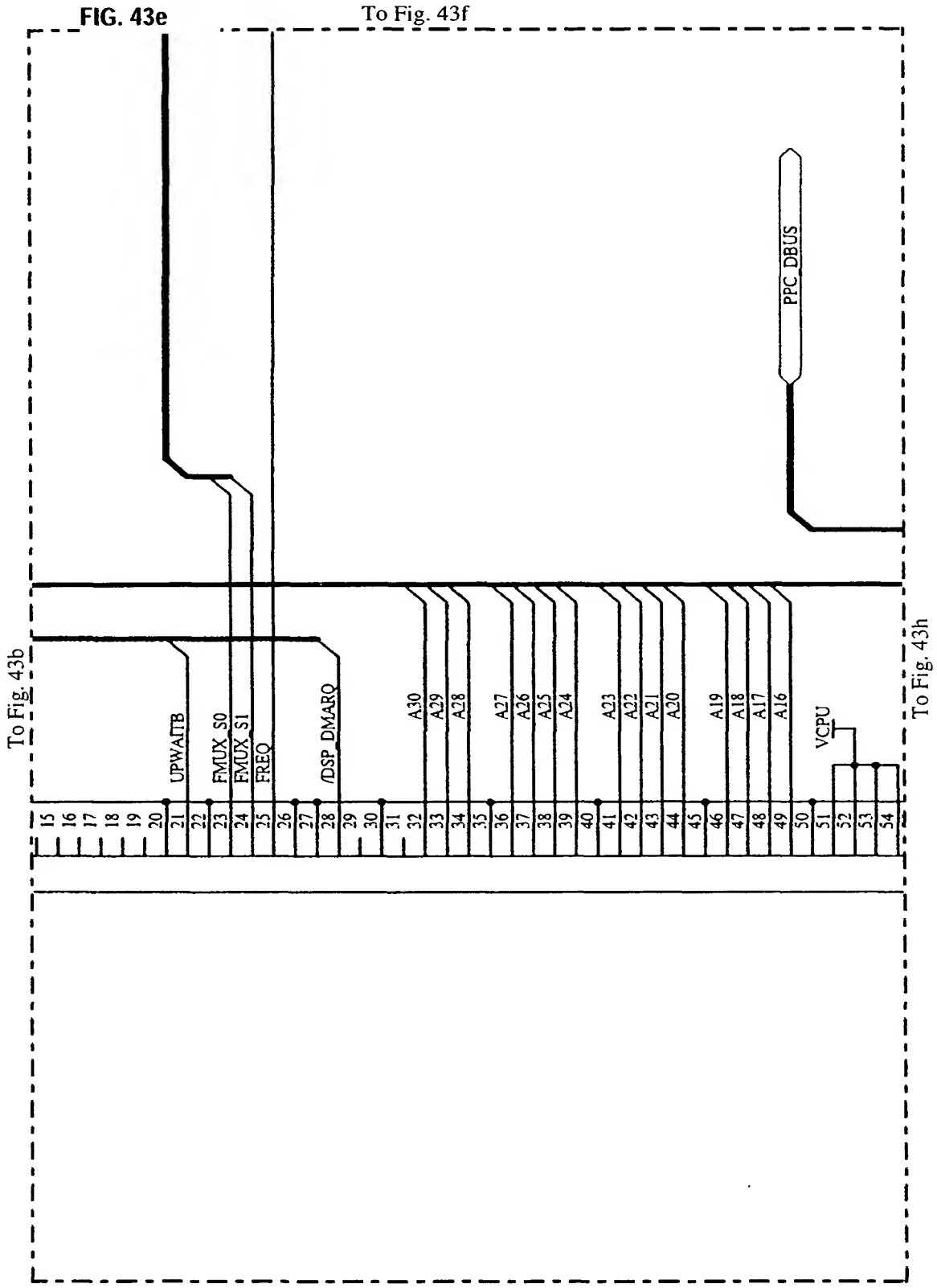
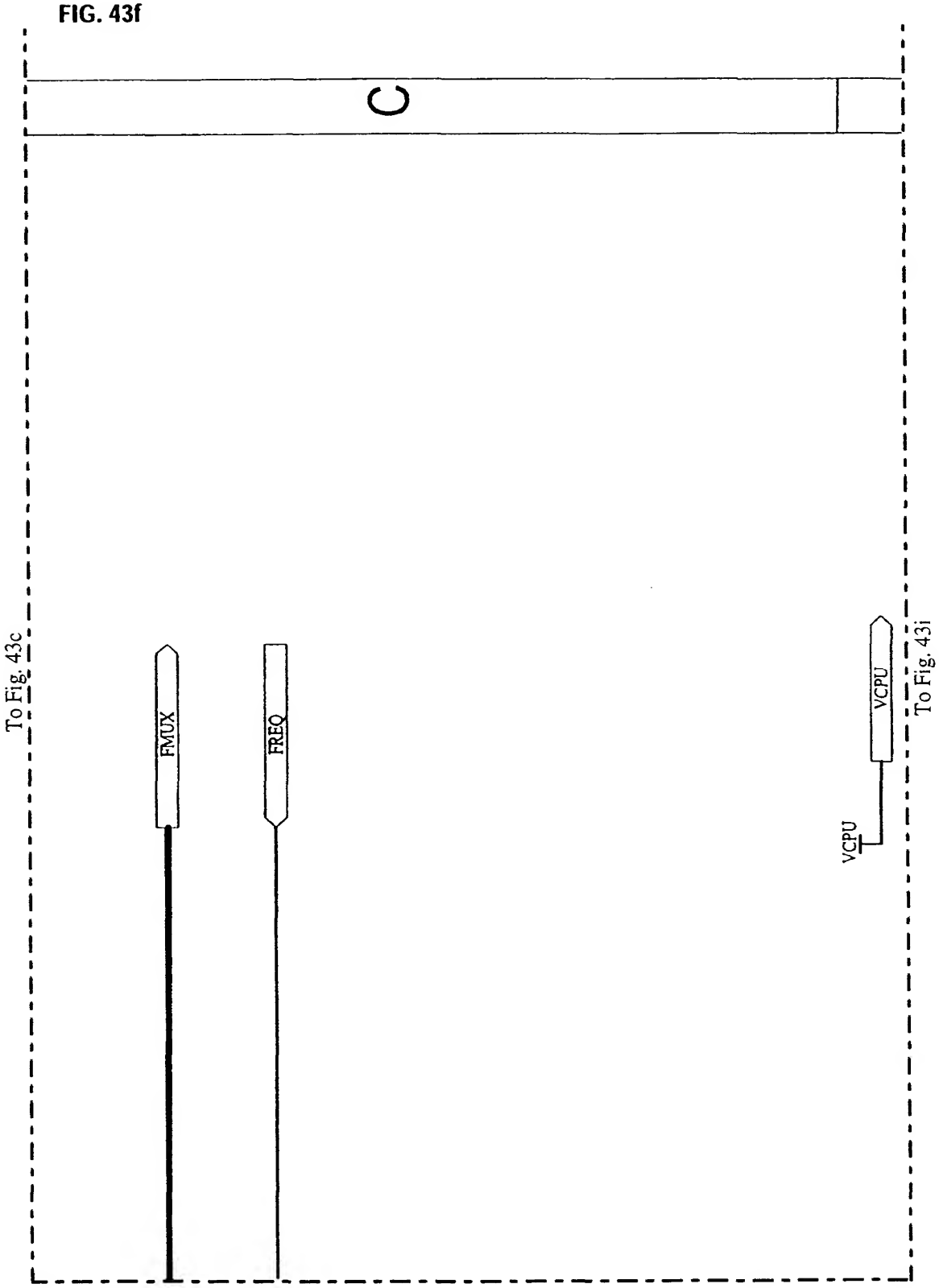

To Fig. 43f
To Fig. 43b
To Fig. 43h
To Fig. 43d
PPC_DBUS
UPWAITB
FMUX_S0
FMUX_S1
FREQ
/DSP_DMARQ
A30
A29
A28
A27
A26
A25
A24
A23
A22
A21
A20
A19
A18
A17
A16
VCPU
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54

FIG. 43f



To Fig. 43e

FIG. 43g

To Fig. 43h

To Fig. 43d

To Fig. 43j

FIG. 43h

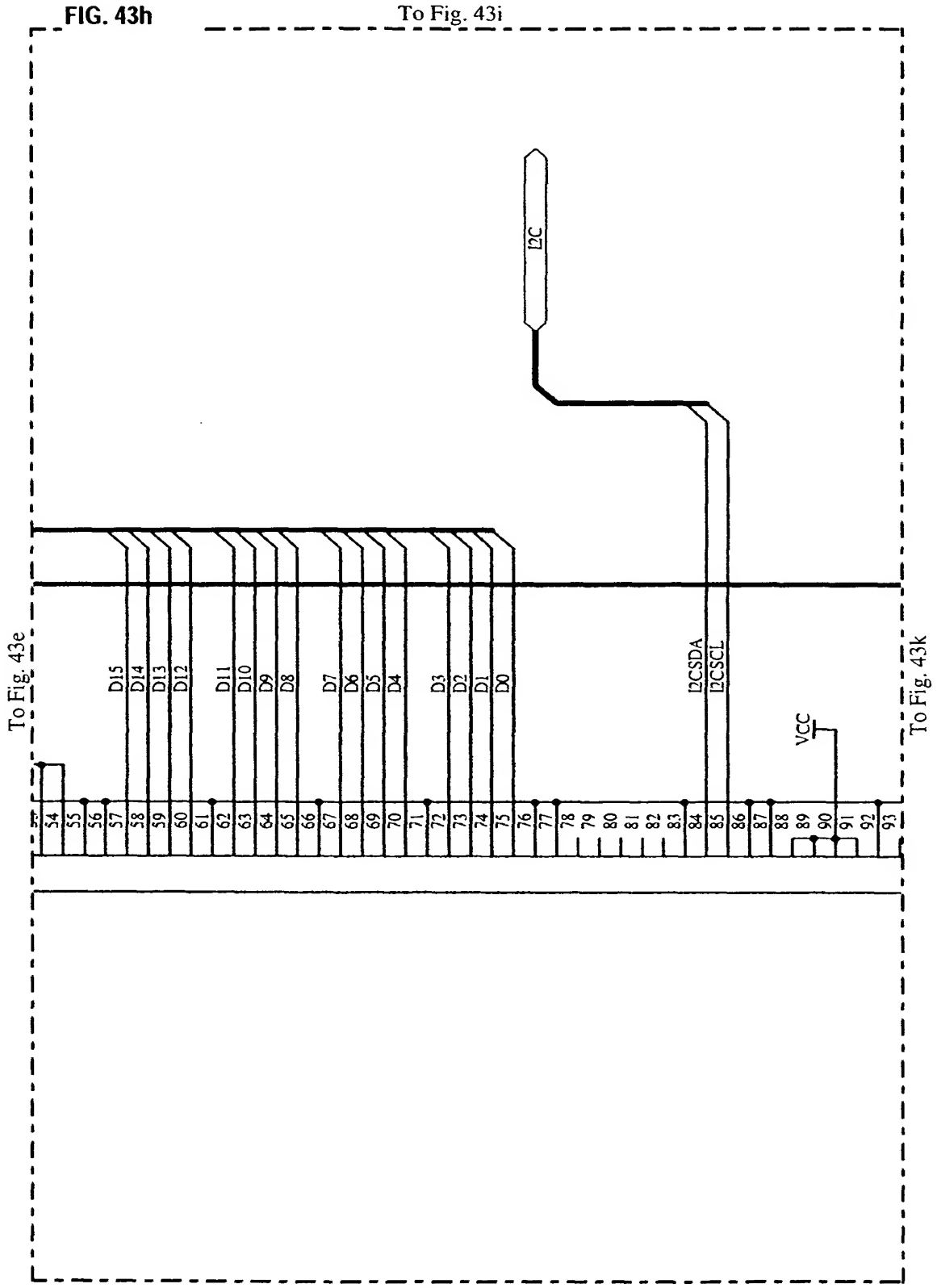
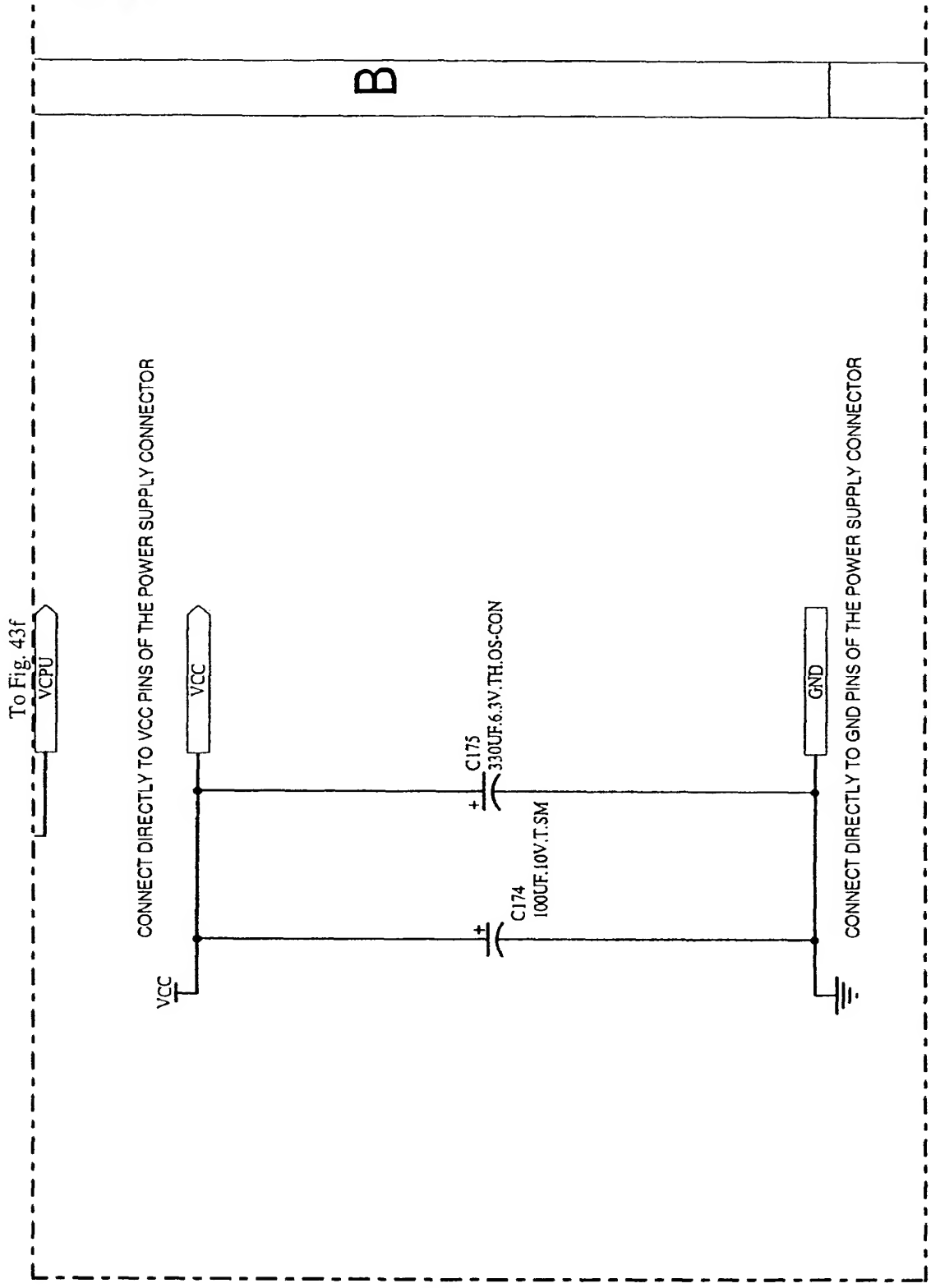

To Fig. 43i
I2C
To Fig. 43e
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
I2CSDA
I2CSCL
VCC
To Fig. 43k
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
To Fig. 43g

FIG. 43i



To Fig. 43h

FIG. 43j

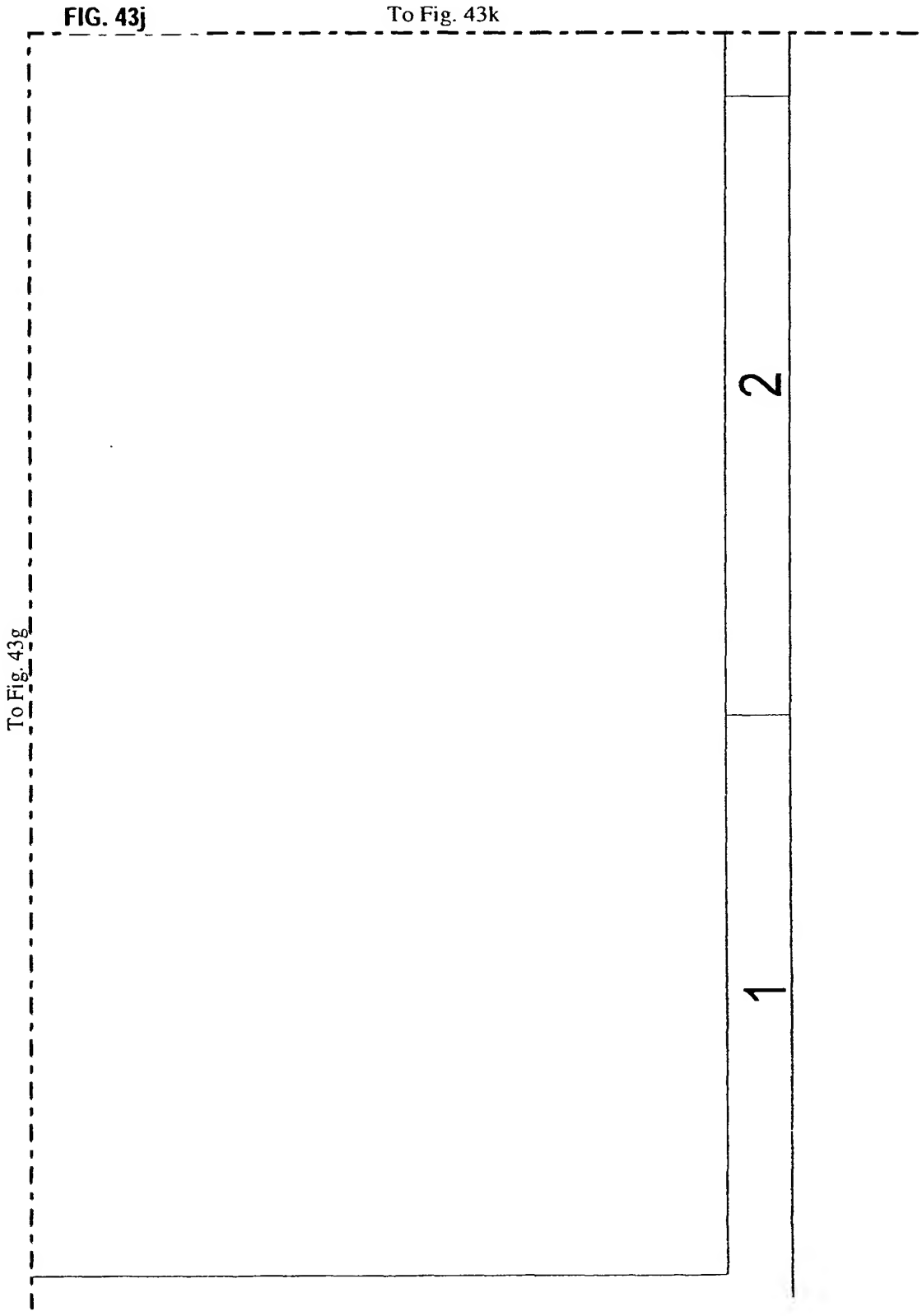


FIG. 43k

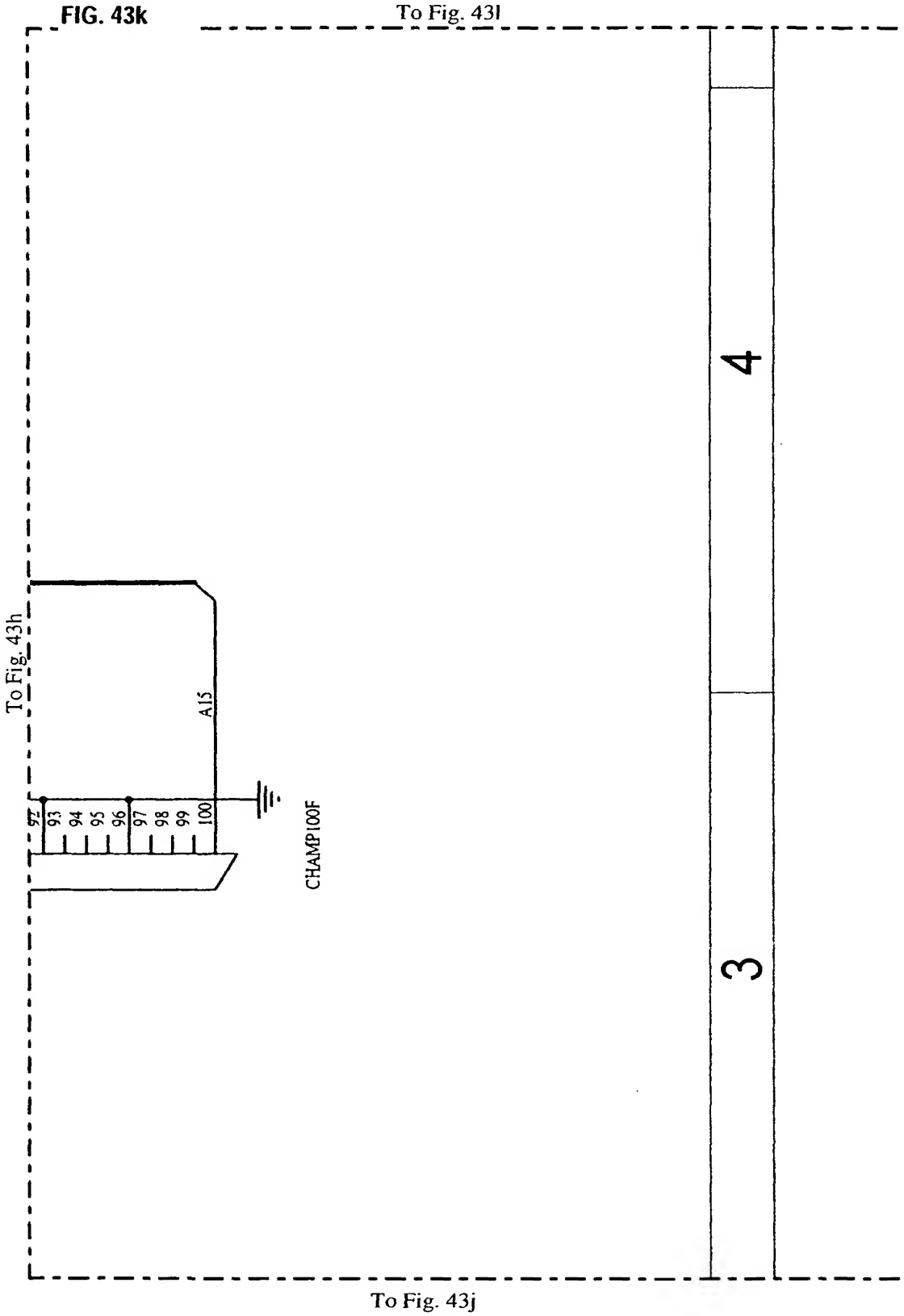

To Fig. 43l
To Fig. 43h
A15
93
94
95
96
97
98
99
100
CHAMP100F
4
3
To Fig. 43j

FIG. 43l

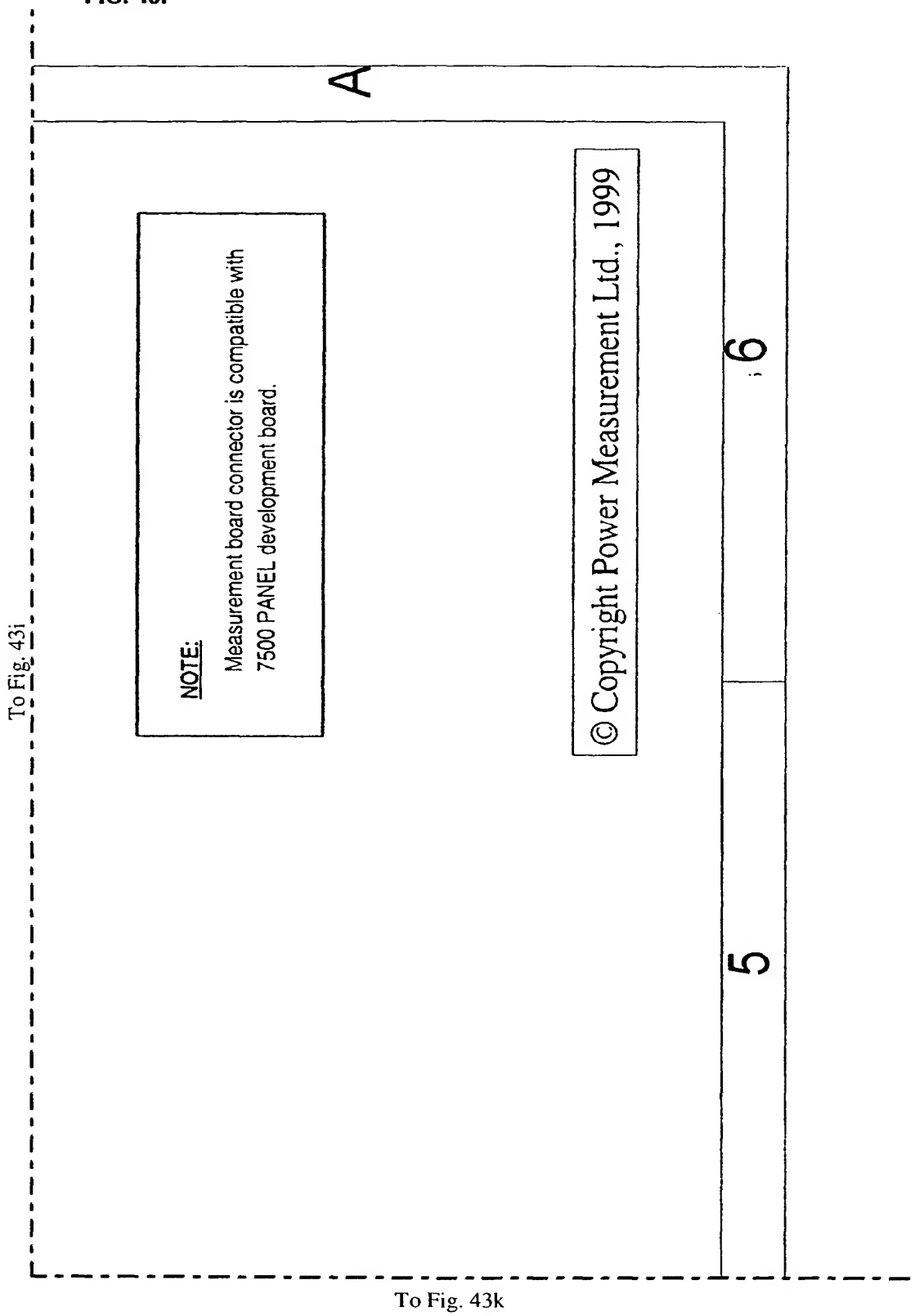
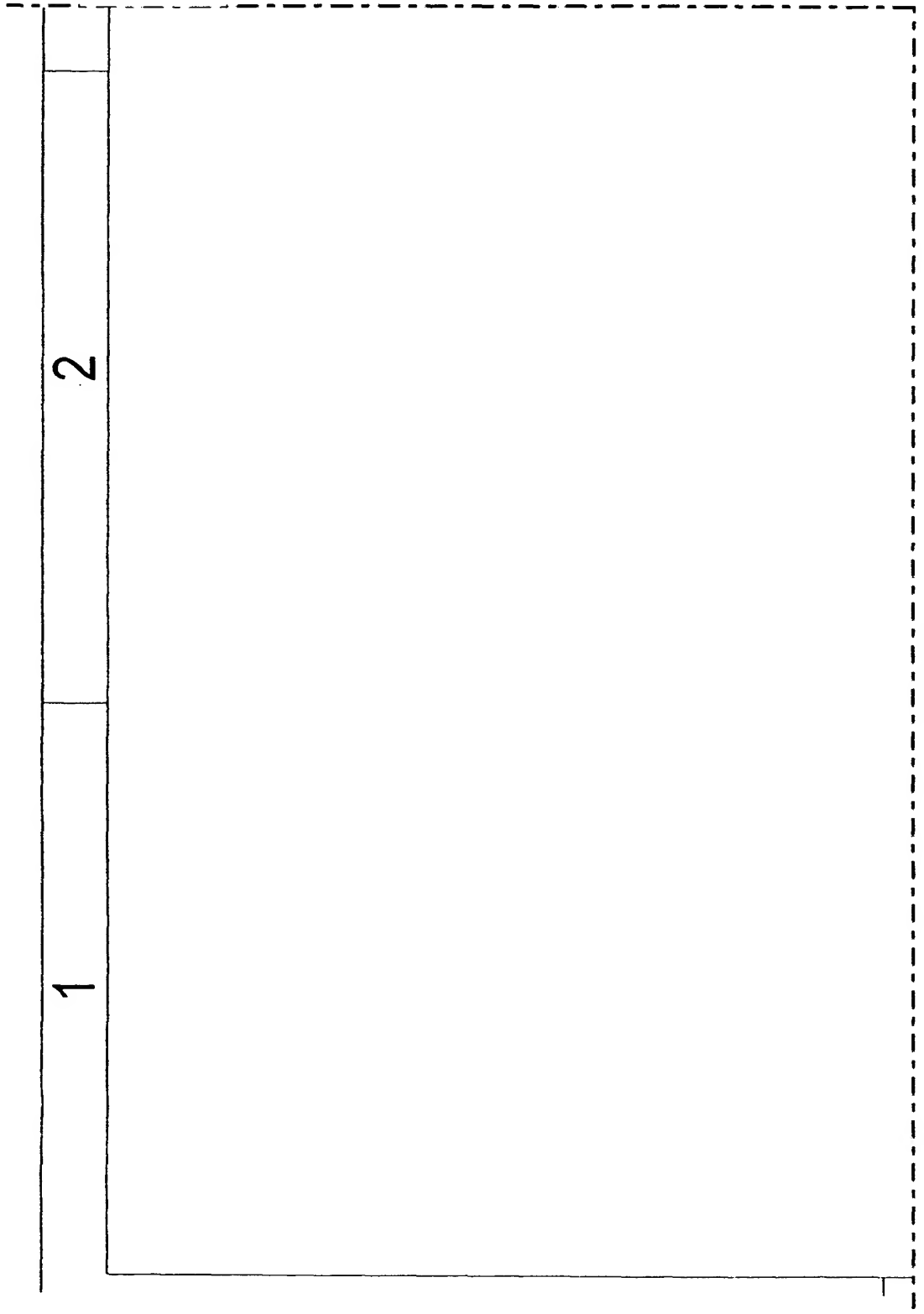

A
NOTE:
Measurement board connector is compatible with 7500 PANEL development board.
© Copyright Power Measurement Ltd., 1999
6
5
To Fig. 43i
To Fig. 43k

FIG. 44a

To Fig. 44b



To Fig. 44d

FIG. 44b

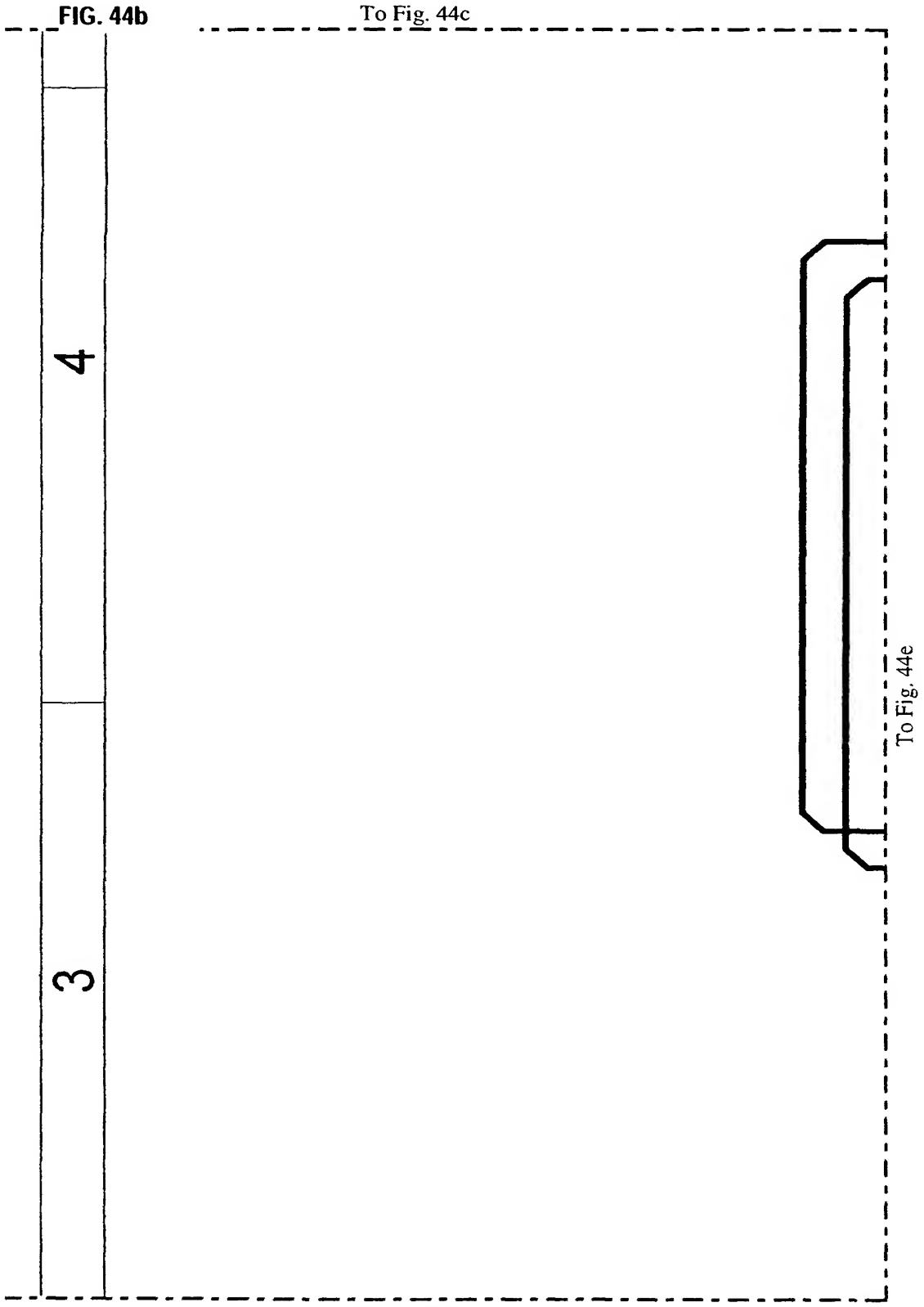


FIG. 44c

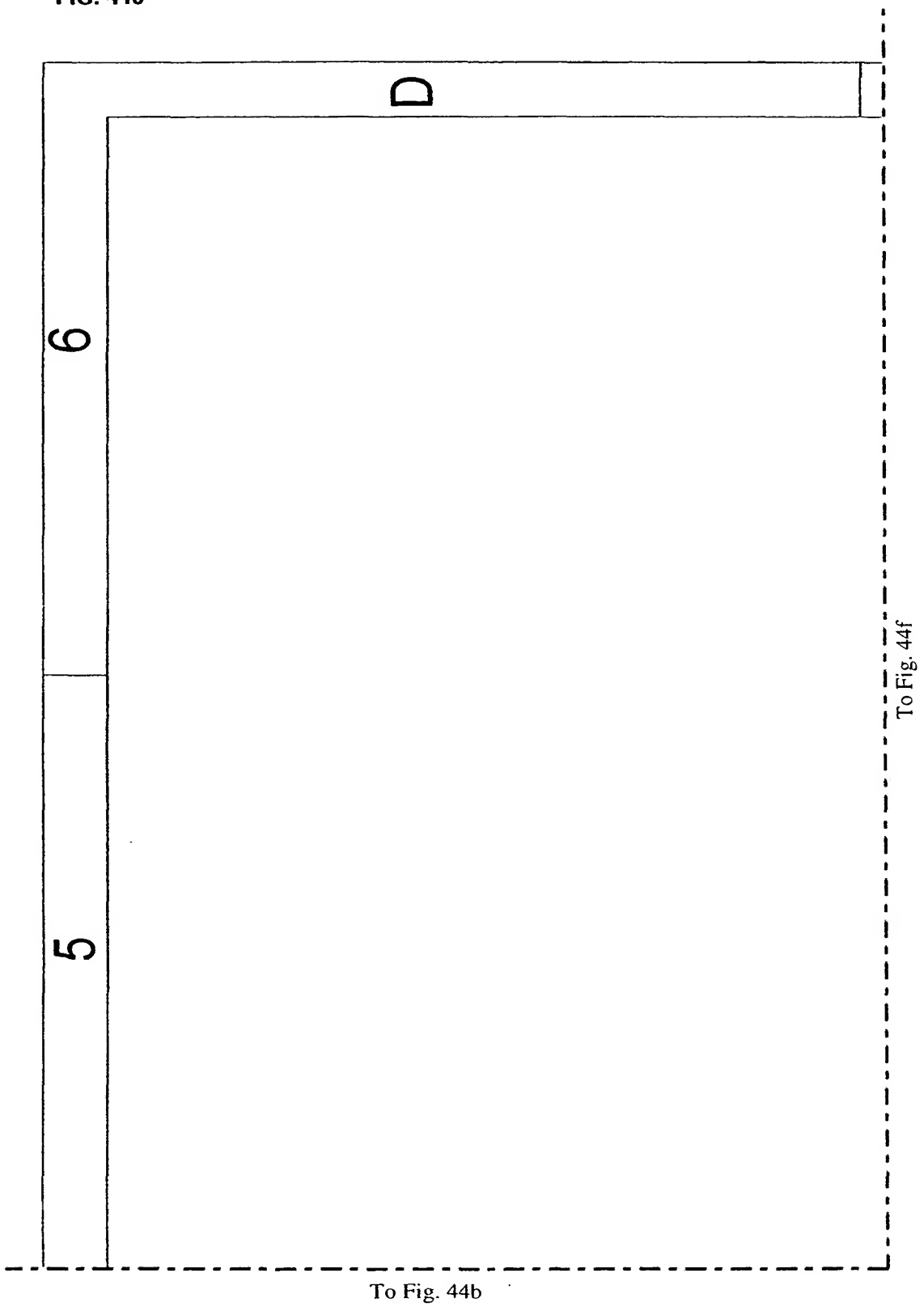


FIG. 44d

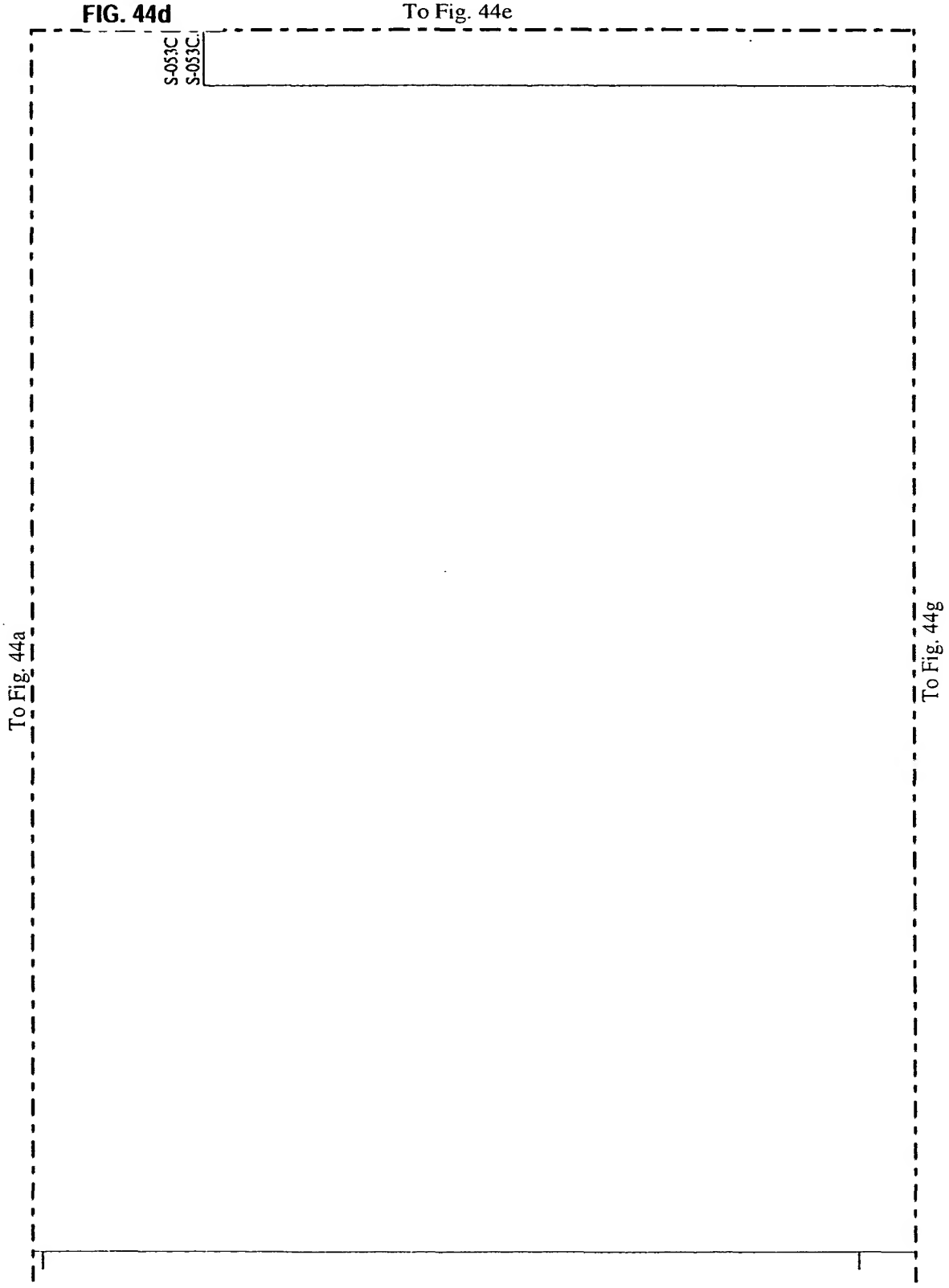


FIG. 44e

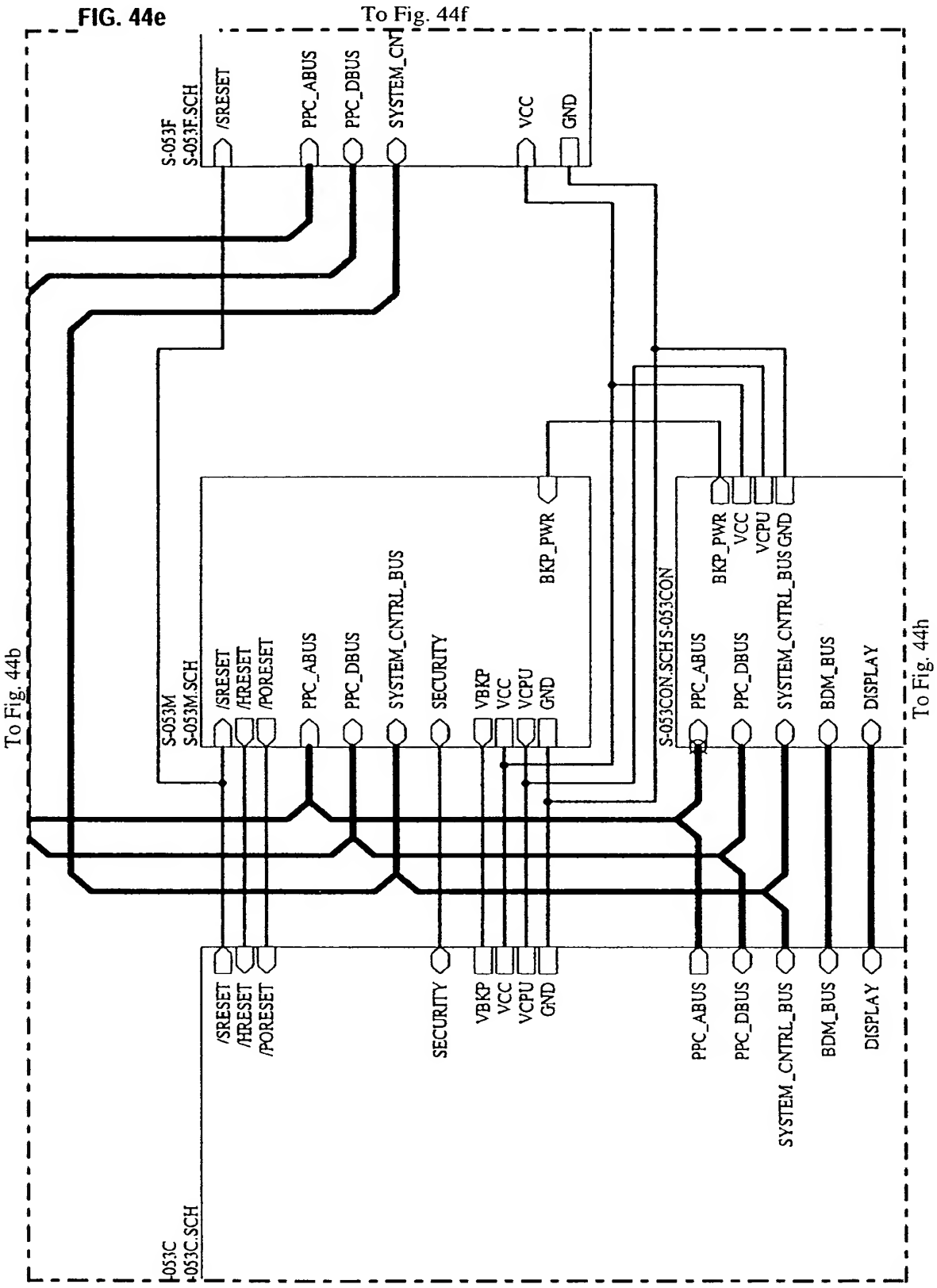
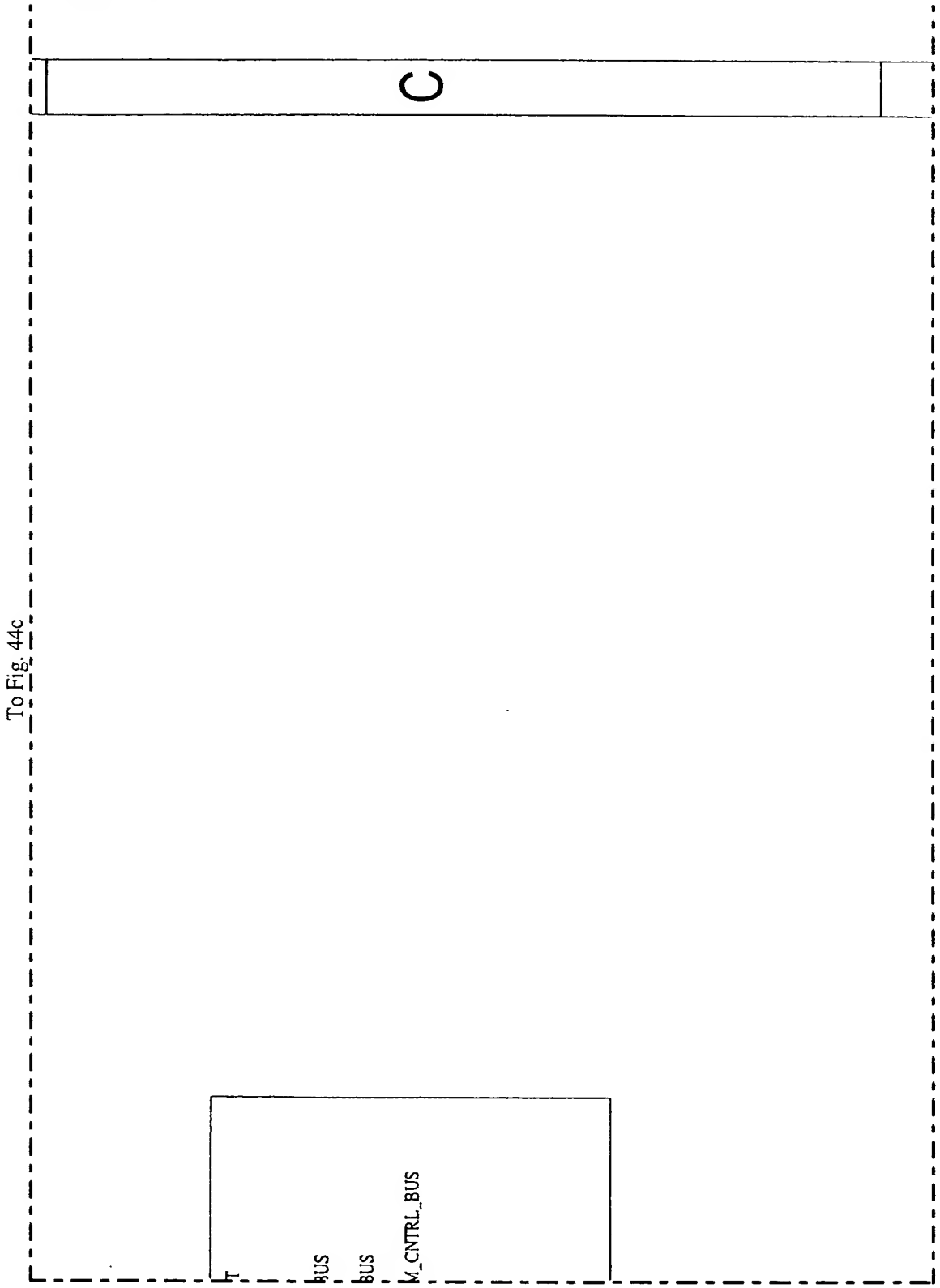

To Fig. 44f
To Fig. 44b
To Fig. 44h
To Fig. 44d
S-053F
S-053F.SCH
/SRESET
PPC_ABUS
PPC_DBUS
SYSTEM_CNTRL_BUS
VCC
GND
S-053M
S-053M.SCH
/SRESET
/HRESET
/PORESET
PPC_ABUS
PPC_DBUS
SYSTEM_CNTRL_BUS
SECURITY
VBKP
VCC
VCPU
GND
BKP_PWR
S-053CON.SCH S-053CON
PPC_ABUS
PPC_DBUS
SYSTEM_CNTRL_BUS
BDM_BUS
DISPLAY
BKP_PWR
VCC
VCPU
GND
S-053C
S-053C.SCH
/SRESET
/HRESET
/PORESET
SECURITY
VBKP
VCC
VCPU
GND
PPC_ABUS
PPC_DBUS
SYSTEM_CNTRL_BUS
BDM_BUS
DISPLAY

FIG. 44f



To Fig. 44e

FIG. 44g

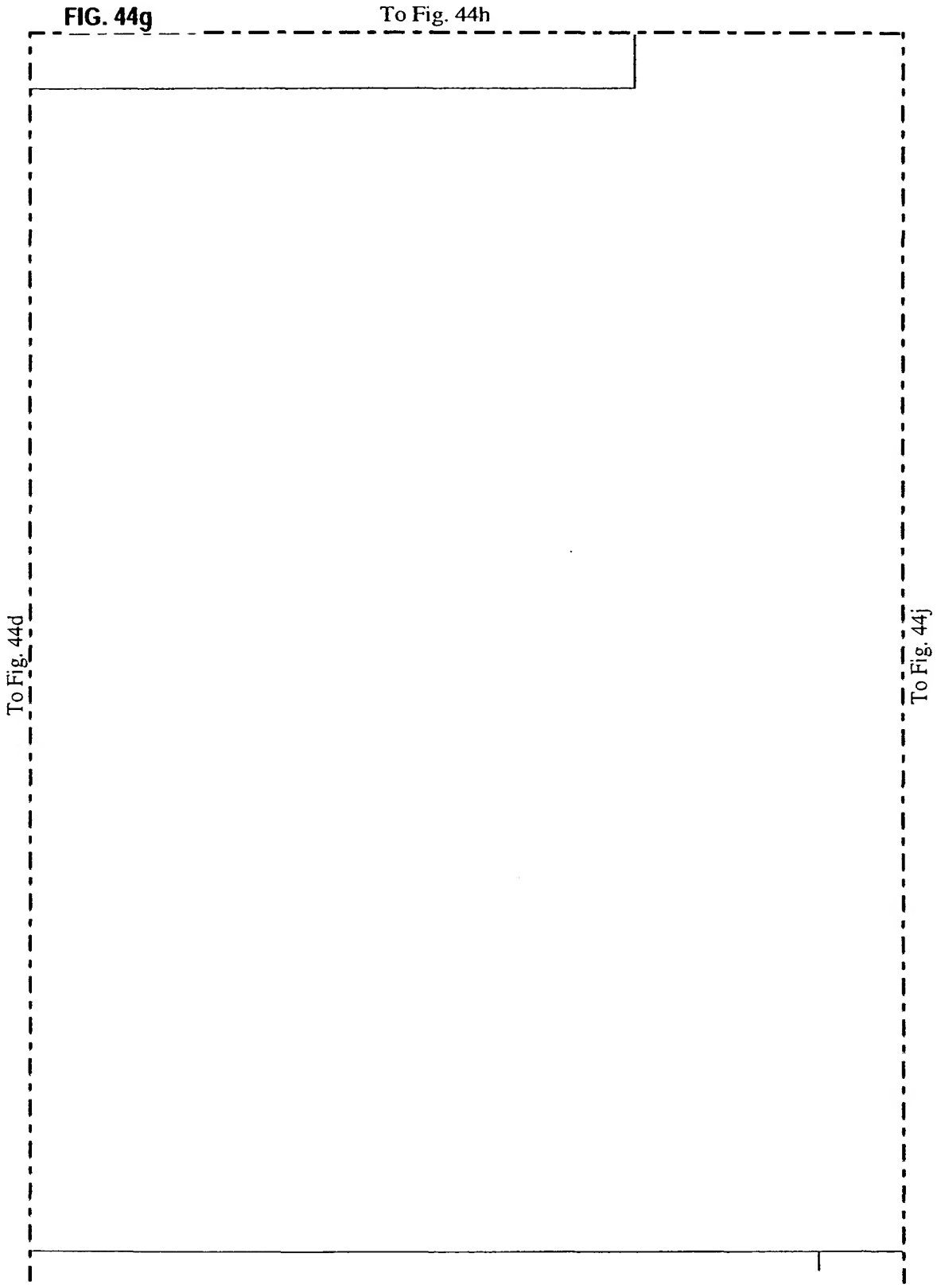


FIG. 44h

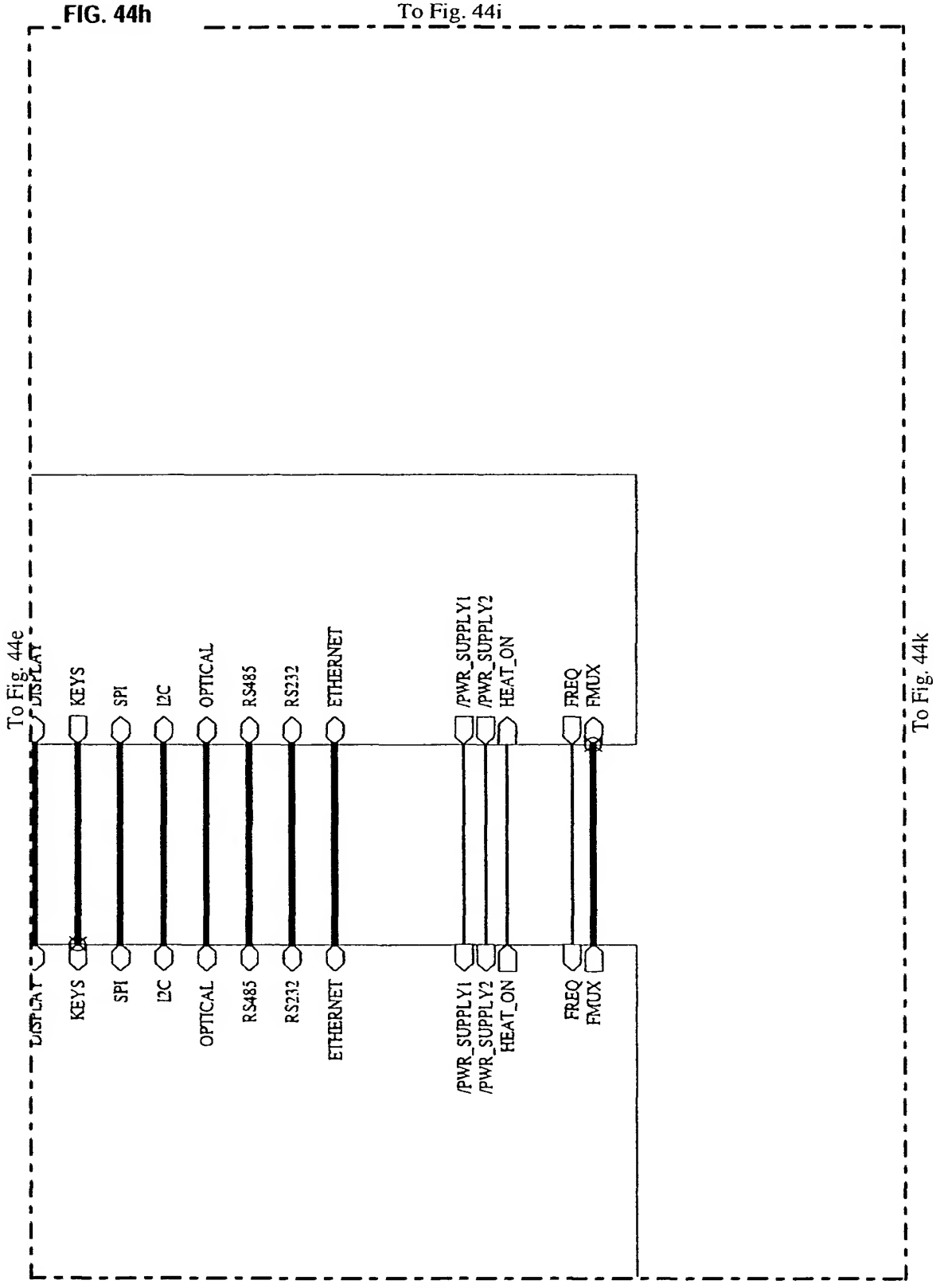

To Fig. 44i
To Fig. 44e
To Fig. 44k
To Fig. 44g
DISPLAY
KEYS
SPI
I2C
OPTICAL
RS485
RS232
ETHERNET
/PWR_SUPPLY1
/PWR_SUPPLY2
HEAT_ON
FREQ
FMUX

FIG. 44i

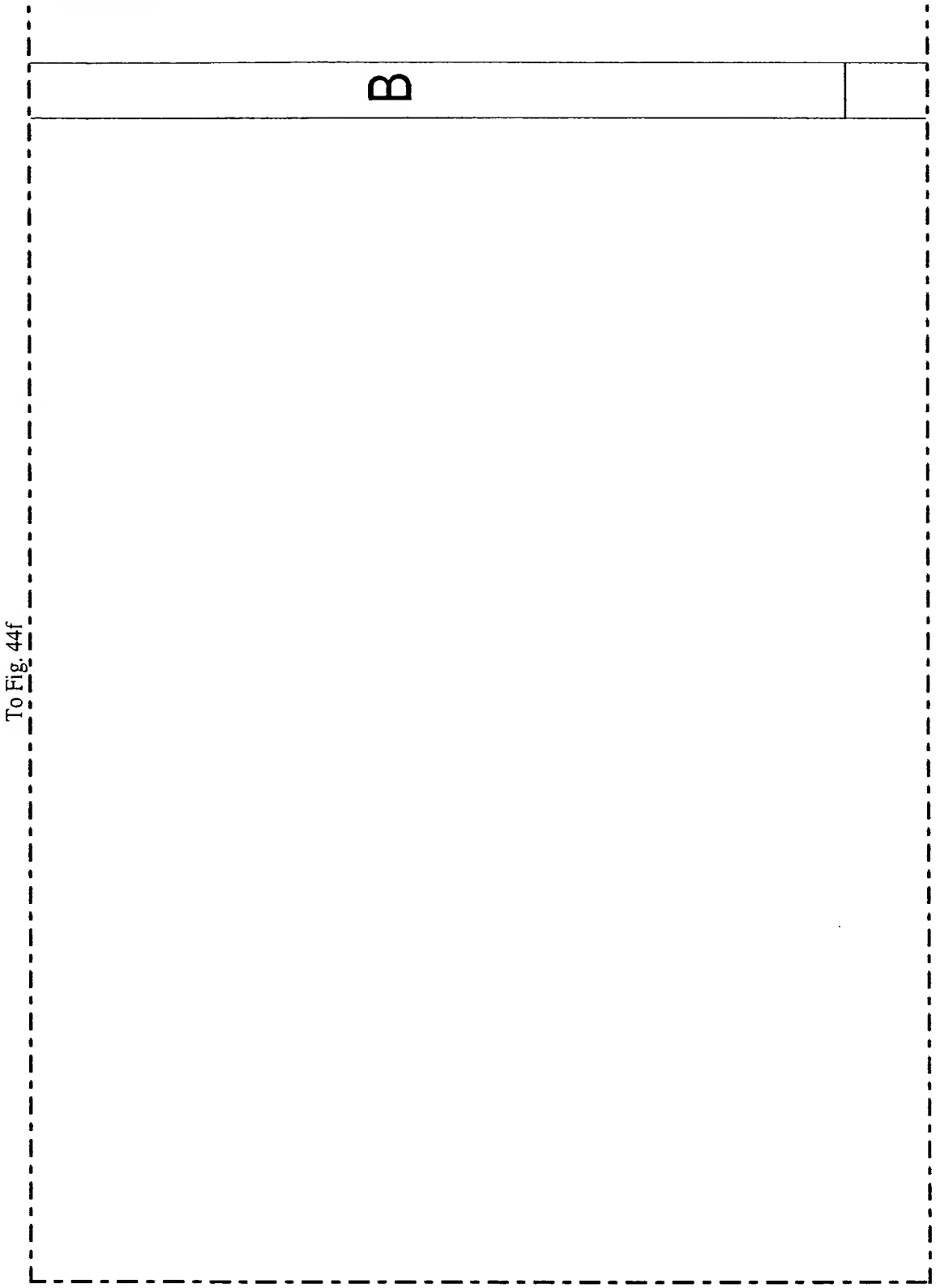
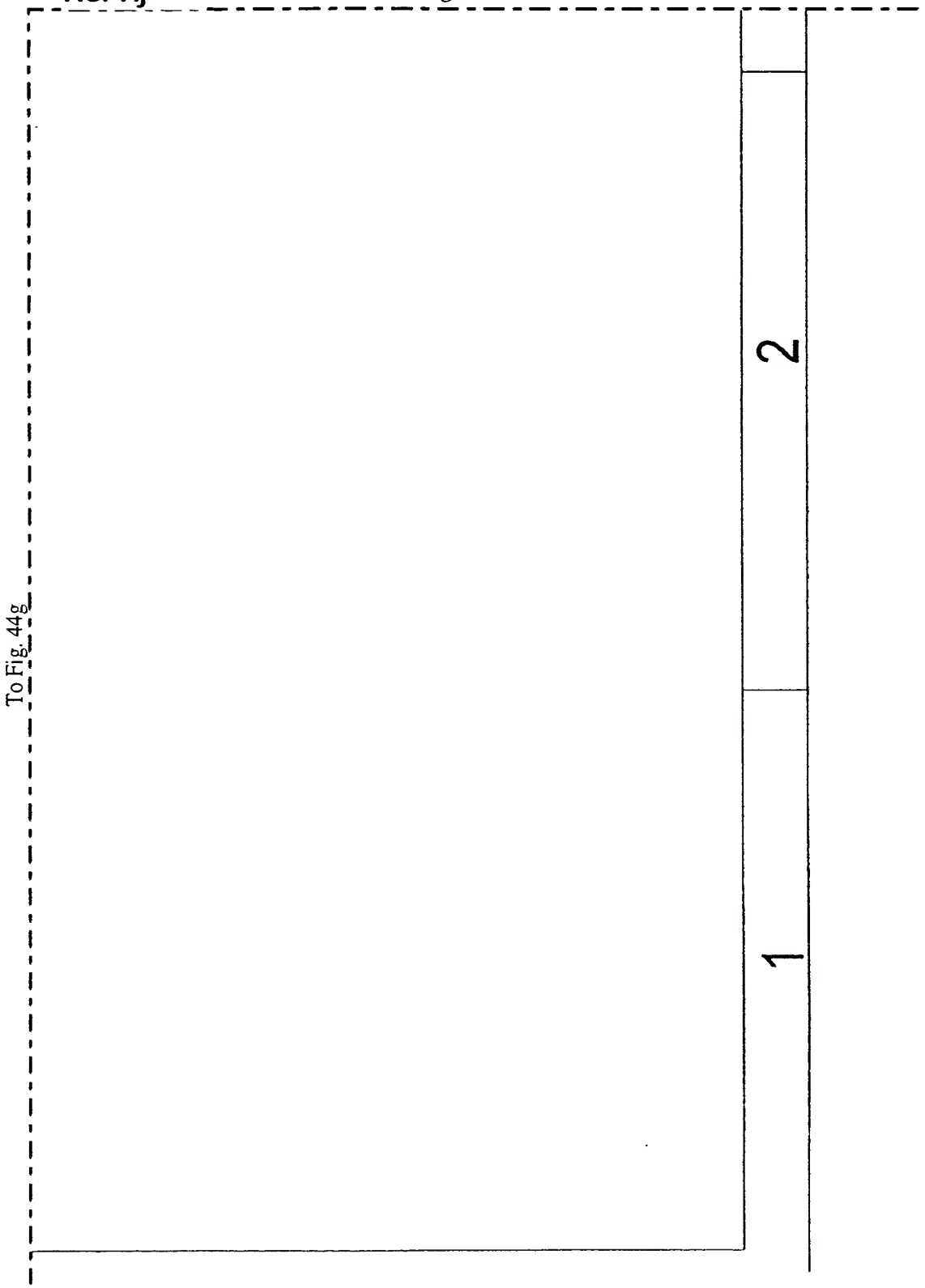


FIG. 44j

To Fig. 44k



To Fig. 44g

FIG. 44k

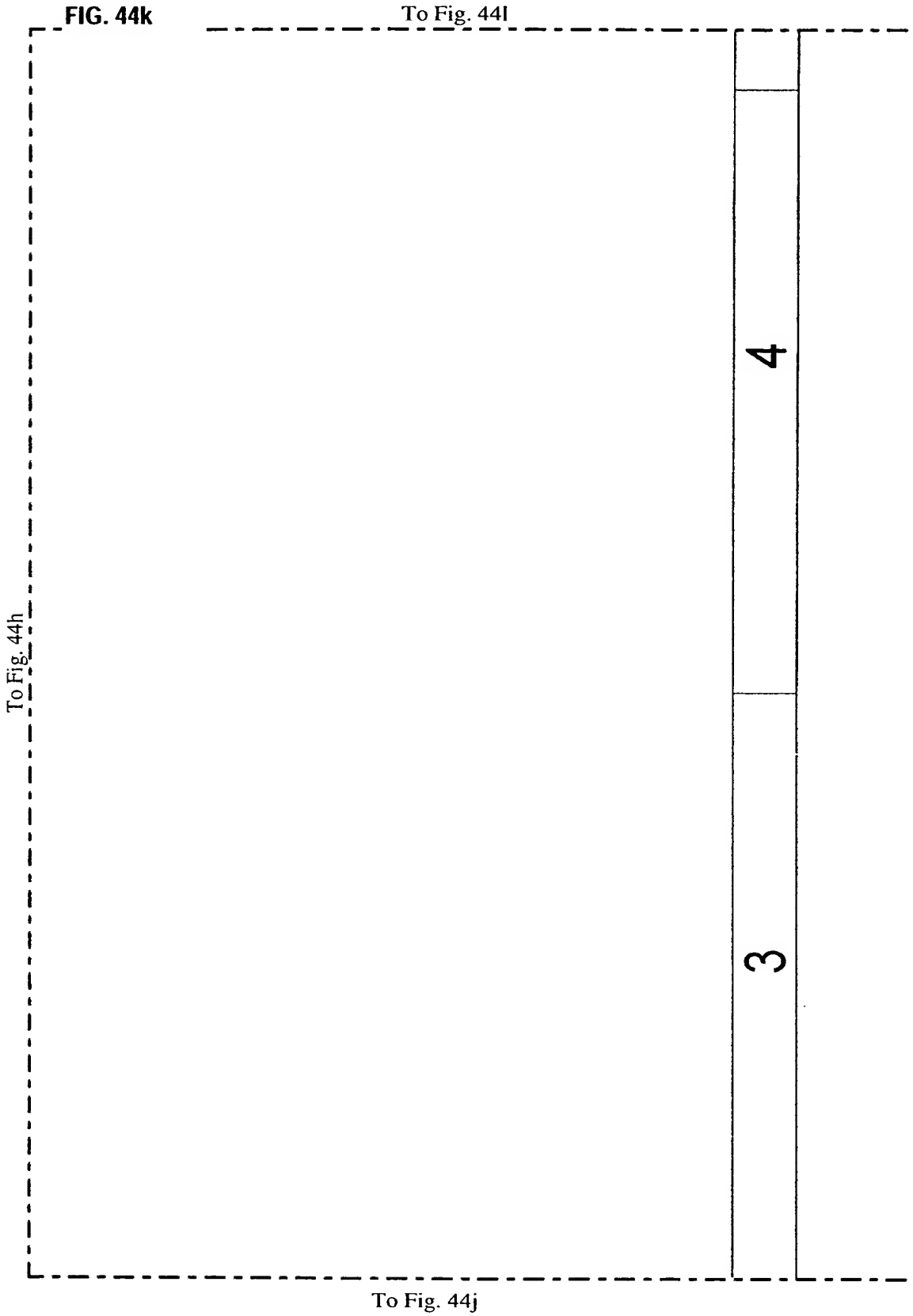


FIG. 44l

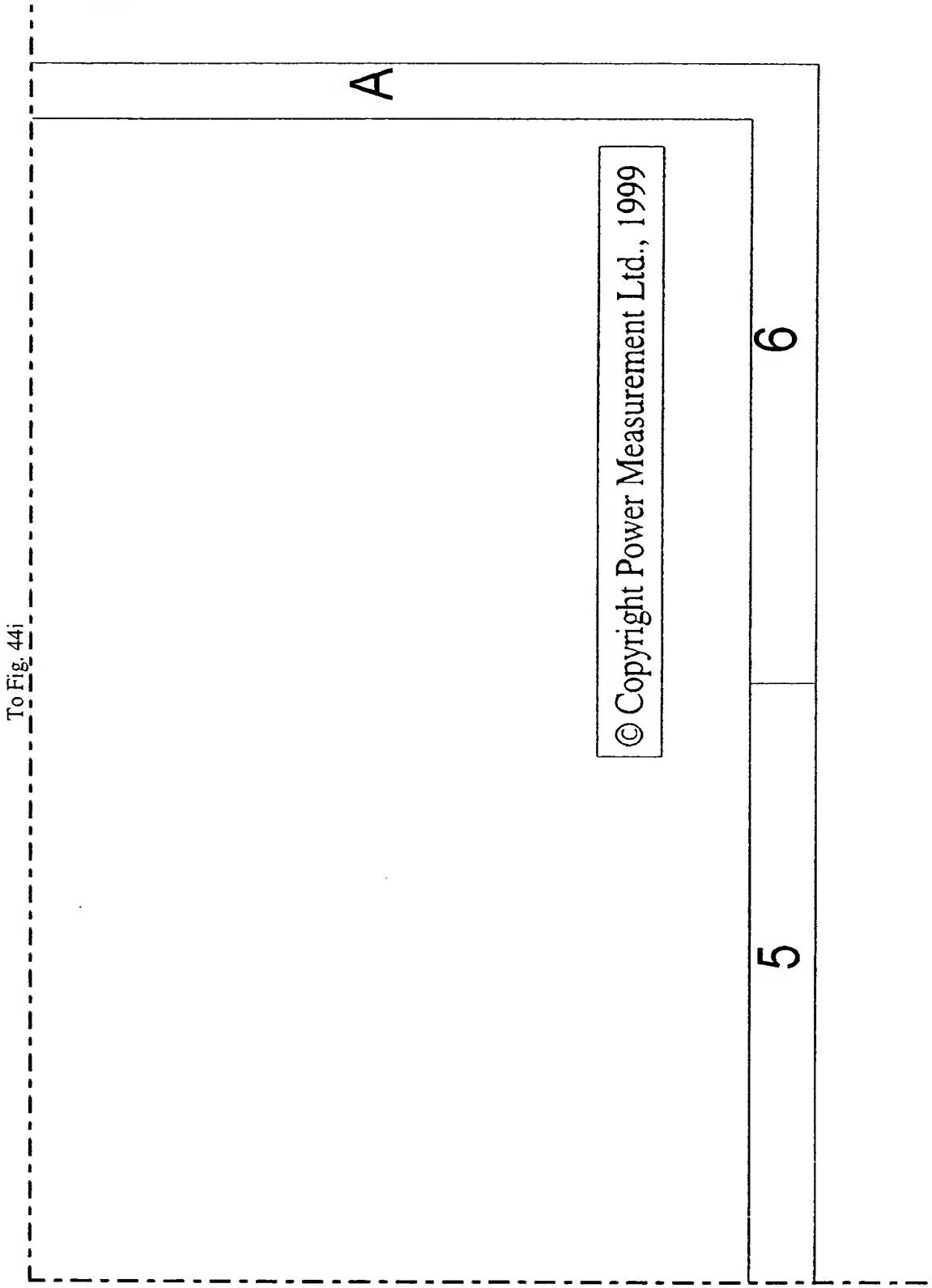

A
6
5
© Copyright Power Measurement Ltd., 1999
To Fig. 44i
To Fig. 44k

FIG. 45a

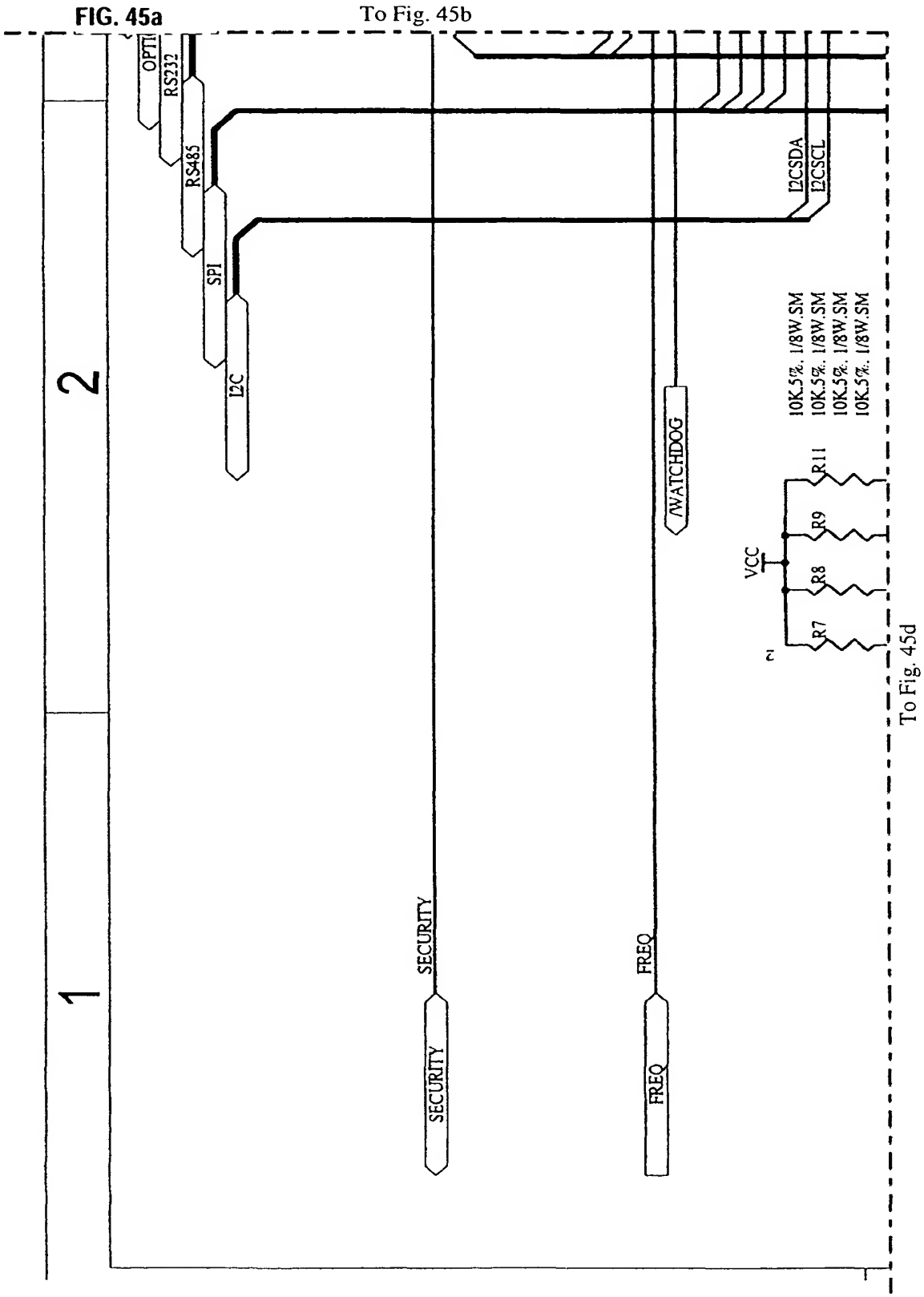
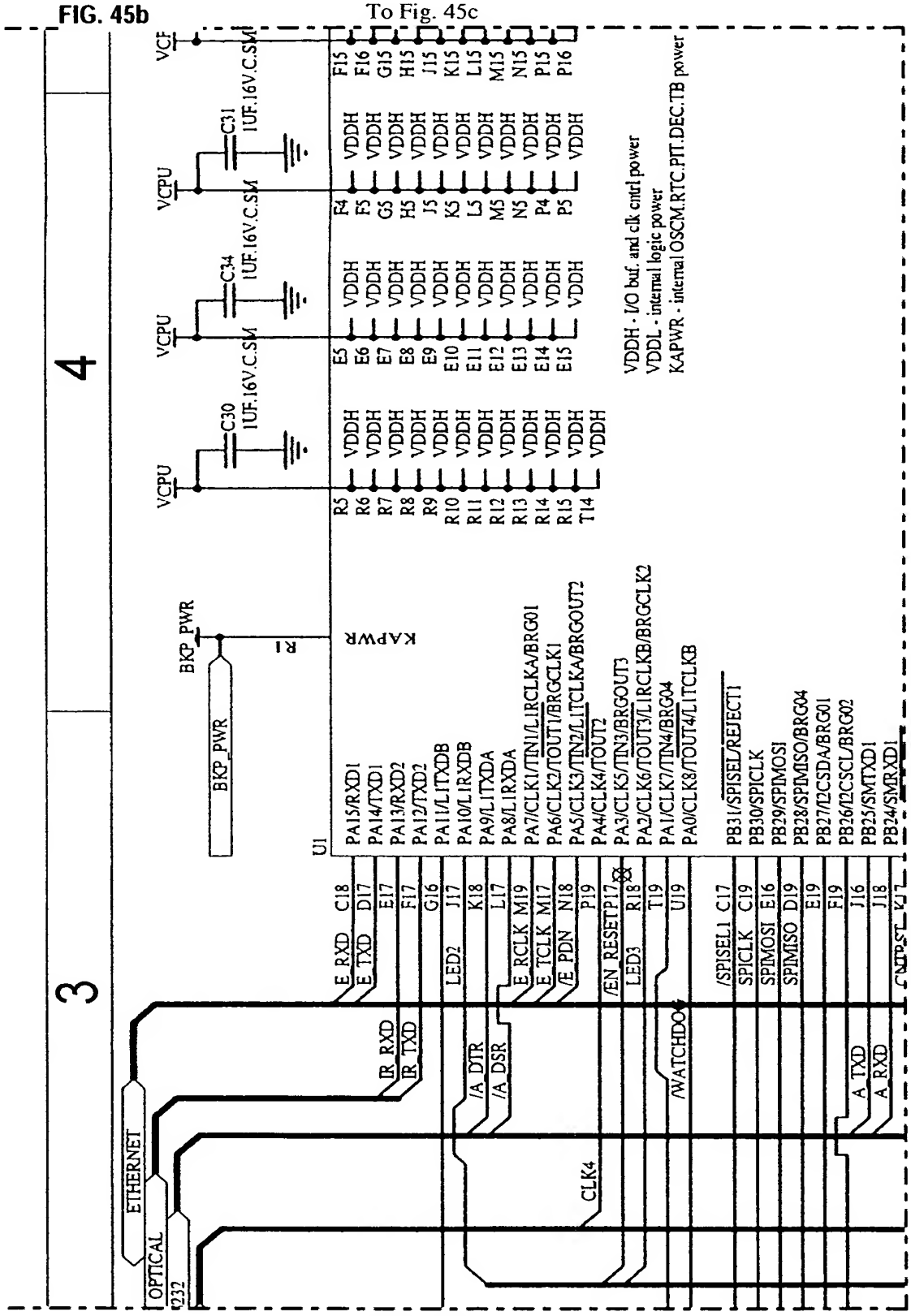

To Fig. 45b
OPTI
RS232
RS485
SPI
I2C
I2CSDA
I2CSCL
/WATCHDOG
10K.5%.1/8W.SM
10K.5%.1/8W.SM
10K.5%.1/8W.SM
10K.5%.1/8W.SM
R11
R9
R8
R7
VCC
SECURITY
SECURITY
FREQ
FREQ
2
1
To Fig. 45d

FIG. 45b



To Fig. 45a

FIG. 45c

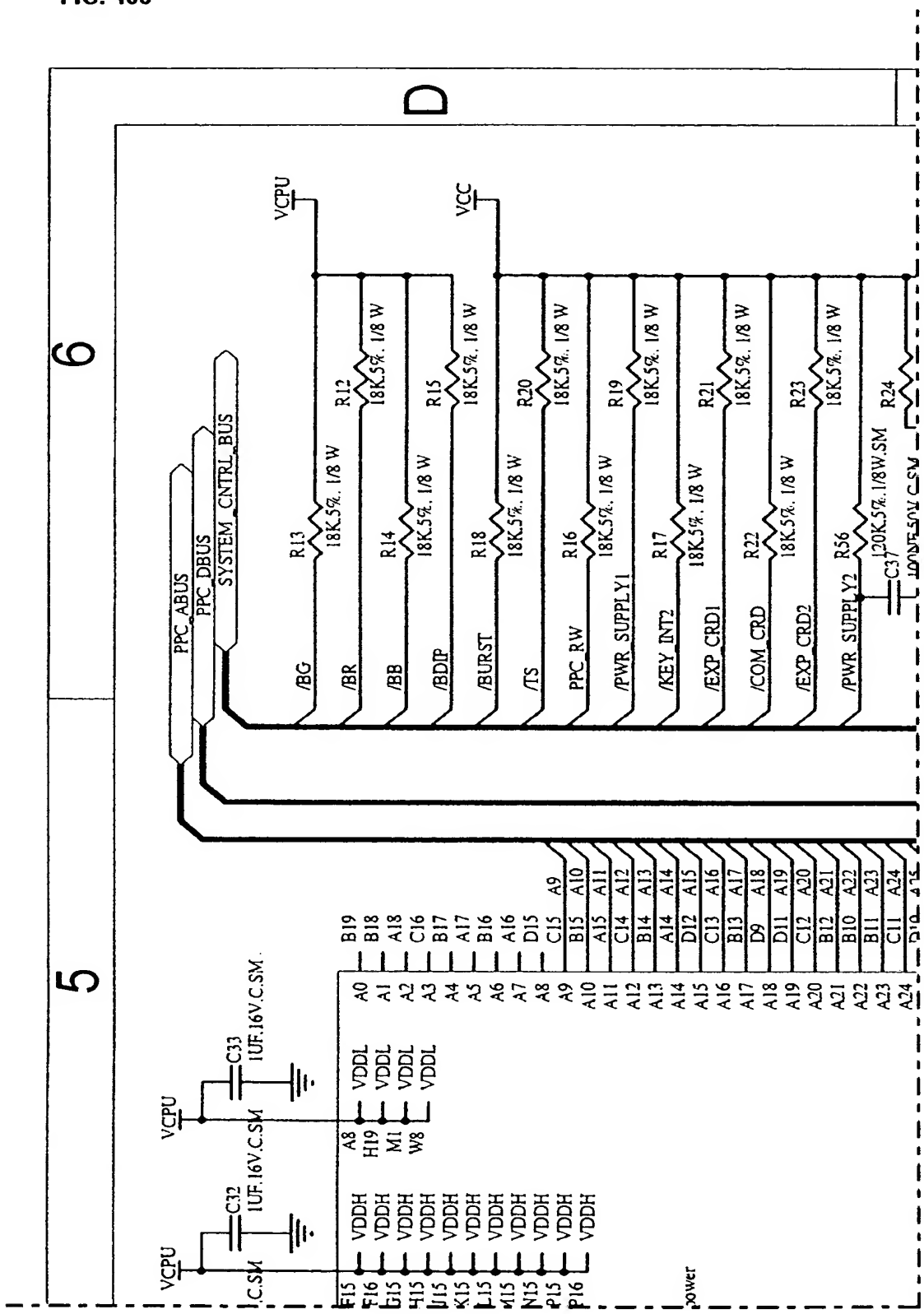

D
6
5
VCPU
VCC
PPC_ABUS
PPC_DBUS
SYSTEM_CNTRL_BUS
/BG
/BR
/BB
/BDIP
/BURST
/TS
PPC_RW
/PWR_SUPPLY1
/KEY_INT2
/EXP_CRD1
/COM_CRD
/EXP_CRD2
/PWR_SUPPLY2
R13
R14
R18
R16
R17
R22
R56
C37
R12
R15
R20
R19
R21
R23
R24
18K.5%. 1/8 W
120K.5%.1/8W.SM
C33
C32
1UF.16V.C.SM
VDDL
VDDH
To Fig. 45f
To Fig. 45b

FIG. 45d

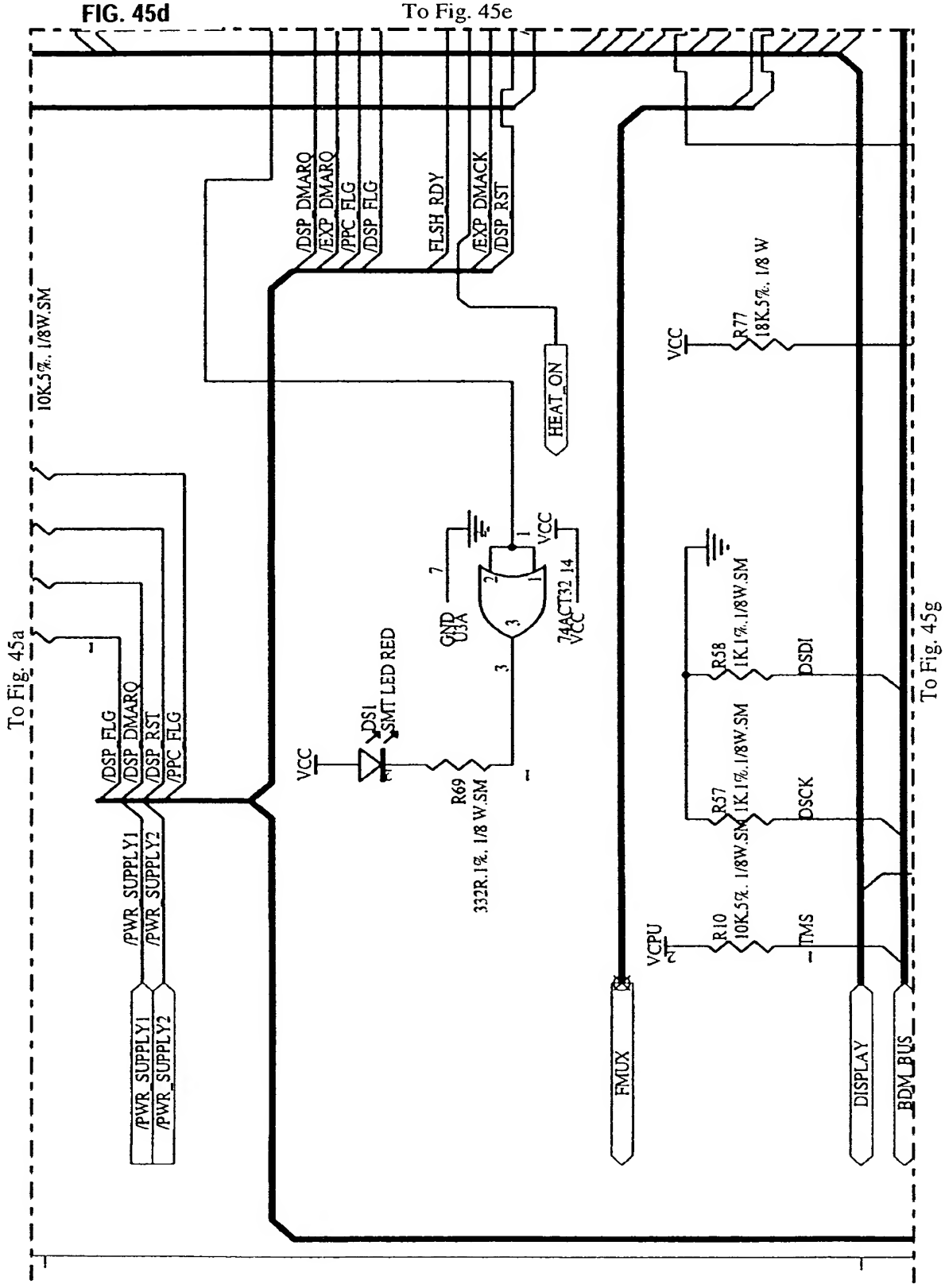

To Fig. 45e
To Fig. 45a
To Fig. 45g
10K.5%. 1/8W.SM
/DSP DMARQ
/EXP DMARQ
/PPC FLG
/DSP FLG
FLSH RDY
/EXP DMACK
/DSP RST
HEAT_ON
VCC
R77
18K.5%. 1/8 W
/DSP FLG
/DSP DMARQ
/DSP RST
/PPC FLG
/PWR_SUPPLY1
/PWR_SUPPLY2
DS1
SMT LED RED
R69
332R.1%. 1/8 W.SM
74ACT32_14
R58
1K.1%.1/8W.SM
DSDI
R57
1K.1%.1/8W.SM
DSCK
R10
10K.5%. 1/8W.SM
TMS
VCPU
FMUX
DISPLAY
BDM_BUS

FIG. 45e

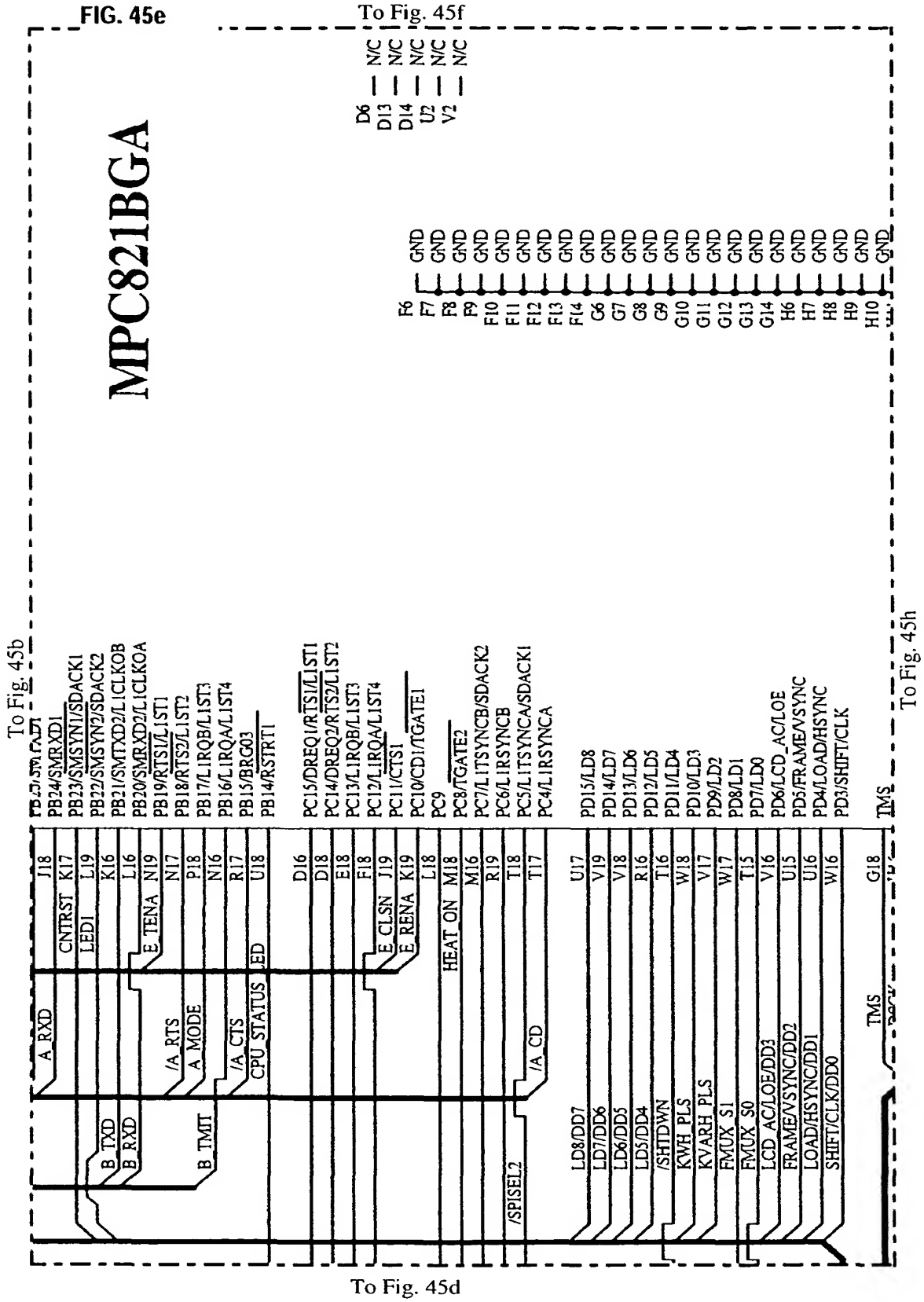

To Fig. 45f
MPC821BGA
To Fig. 45b
To Fig. 45h
To Fig. 45d
A_RXD
CNTRST
LED1
B_TXD
B_RXD
B_TMIT
/A_RTS
A_MODE
/A_CTS
CPU_STATUS
LED
E_TENA
E_CLSN
E_RENA
HEAT_ON
/A_CD
/SPISEL2
TMS
N/C
GND

FIG. 45f

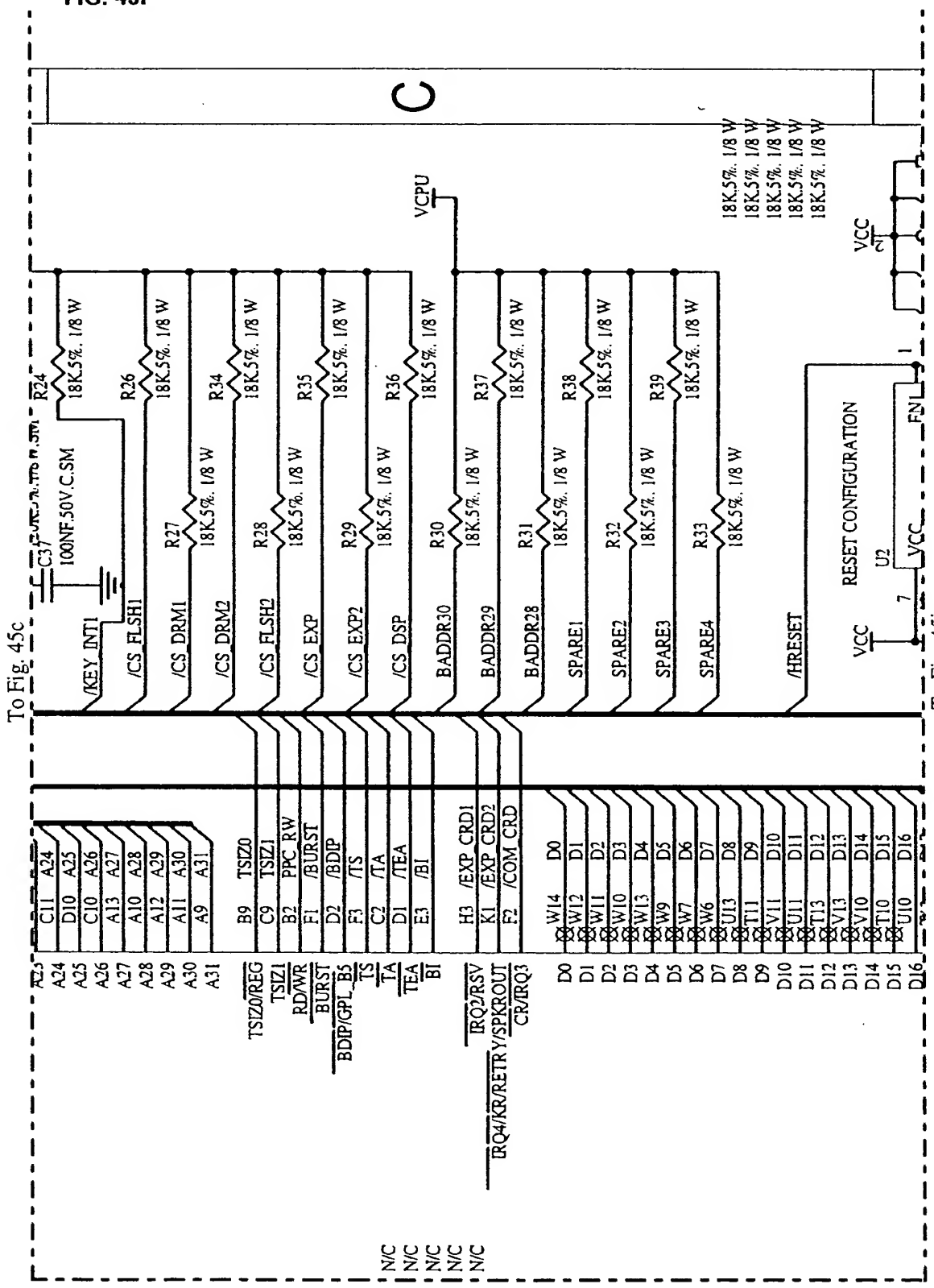

C
VCPU
VCC
18K.5%. 1/8 W
R24
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
C37
100NF.50V.C.SM
/KEY_INT1
/CS_FLSH1
/CS_DRM1
/CS_DRM2
/CS_FLSH2
/CS_EXP
/CS_EXP2
/CS_DSP
BADDR30
BADDR29
BADDR28
SPARE1
SPARE2
SPARE3
SPARE4
/HRESET
RESET CONFIGURATION
U2
FN
To Fig. 45c
To Fig. 45i
To Fig. 45e
A24
A25
A26
A27
A28
A29
A30
A31
TSIZ0/REG
TSIZ1
RD/WR
BURST
BDIP/GPL_B5
TS
TA
TEA
BI
IRQ2/RSV
IRQ4/KR/RETRY/SPKROUT
CR/IRQ3
/EXP CRD1
/EXP CRD2
/COM_CRD
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
N/C

FIG. 45g

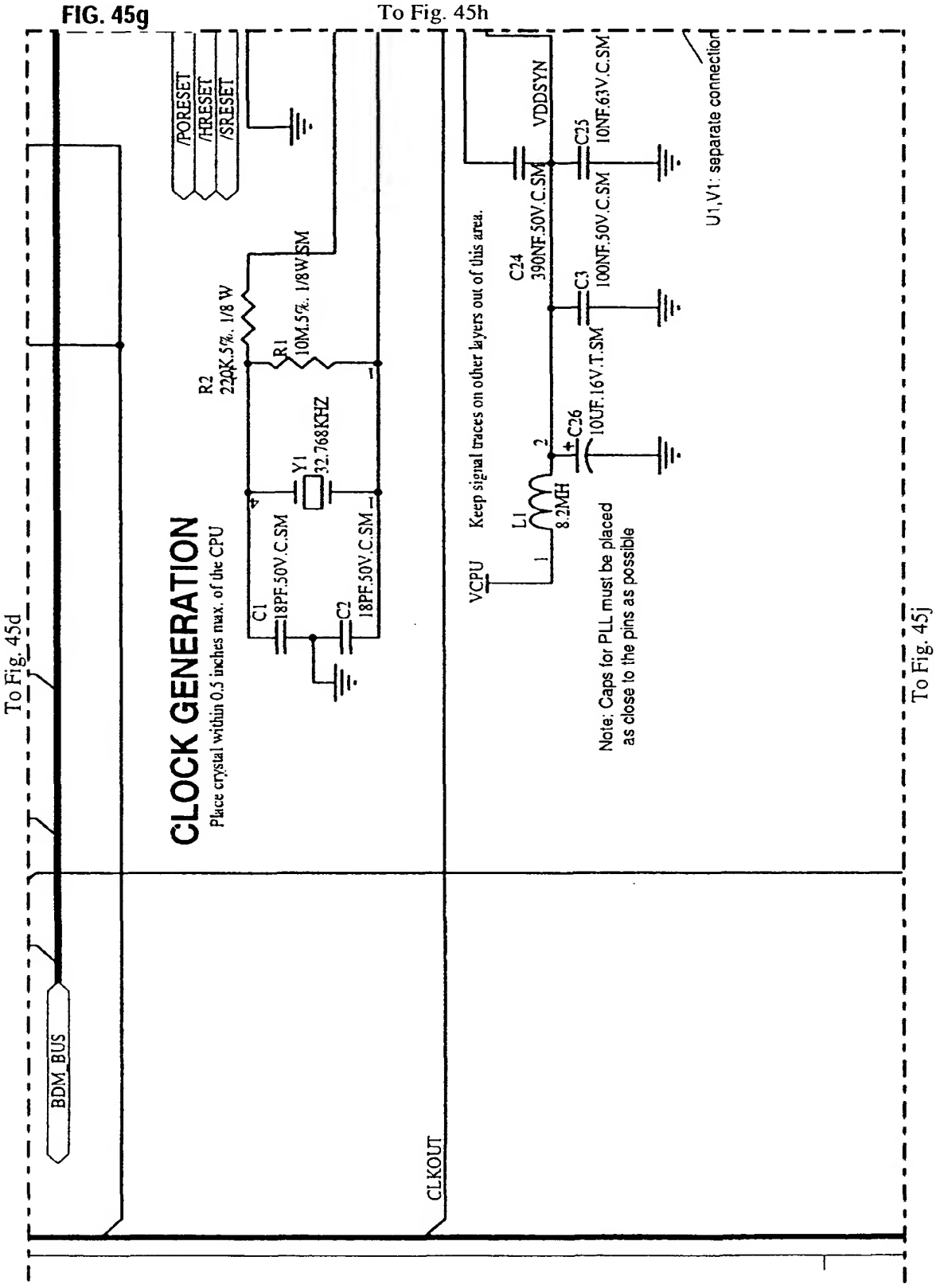
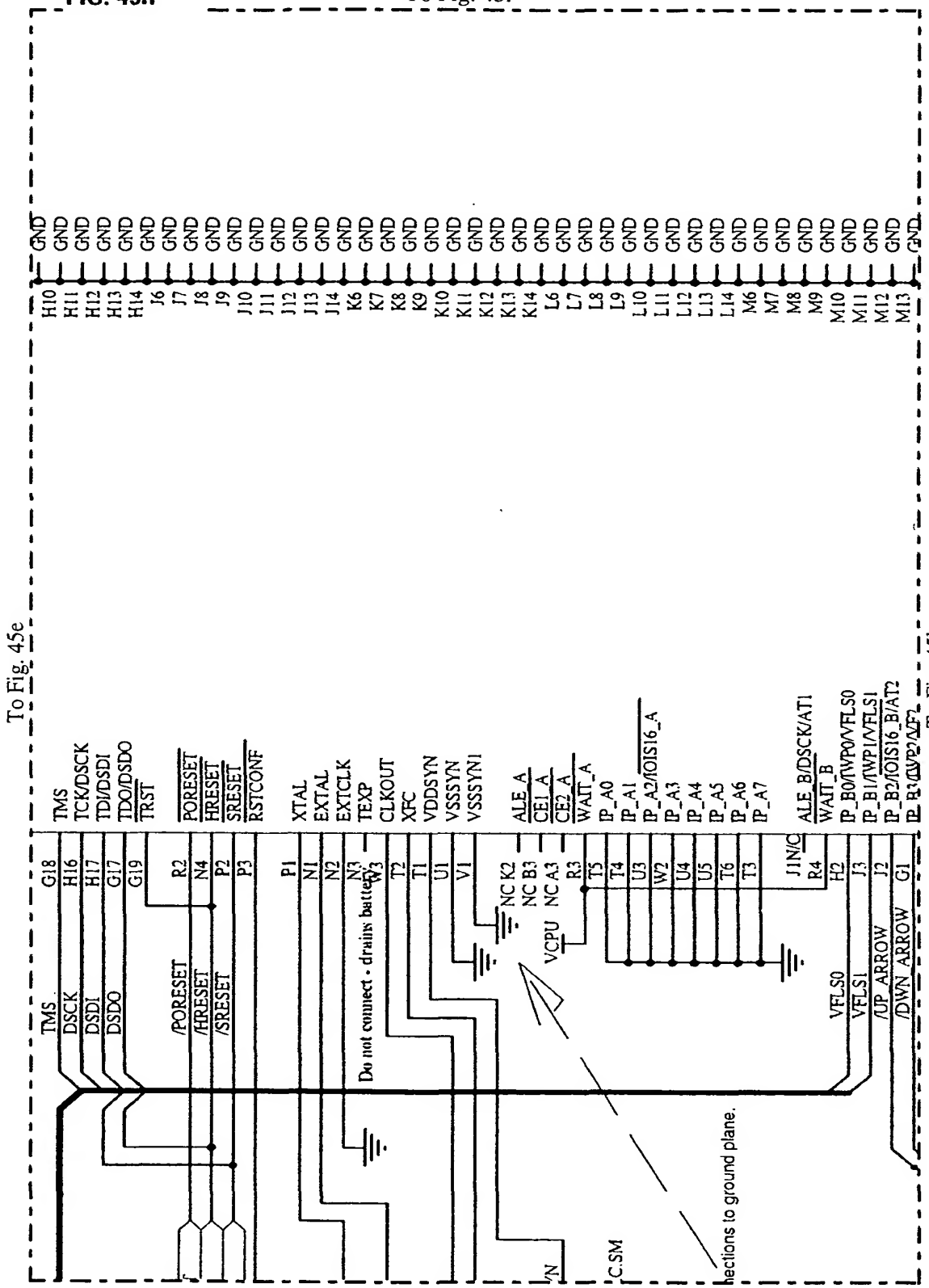

To Fig. 45h
To Fig. 45d
To Fig. 45j
CLOCK GENERATION
Place crystal within 0.5 inches max. of the CPU
/PORESET
/HRESET
/SRESET
BDM_BUS
CLKOUT
R2
220K.5%. 1/8 W
R1
10M.5%. 1/8W.SM
Y1
32.768KHZ
C1
18PF.50V.C.SM
C2
18PF.50V.C.SM
VCPU
Keep signal traces on other layers out of this area.
L1
8.2MH
C24
390NF.50V.C.SM
VDDSYN
C25
10NF.63V.C.SM
C3
100NF.50V.C.SM
C26
10UF.16V.T.SM
Note: Caps for PLL must be placed as close to the pins as possible
U1,V1: separate connection

FIG. 45h

To Fig. 45i



To Fig. 45e

To Fig. 45k

To Fig. 45g

FIG. 45i

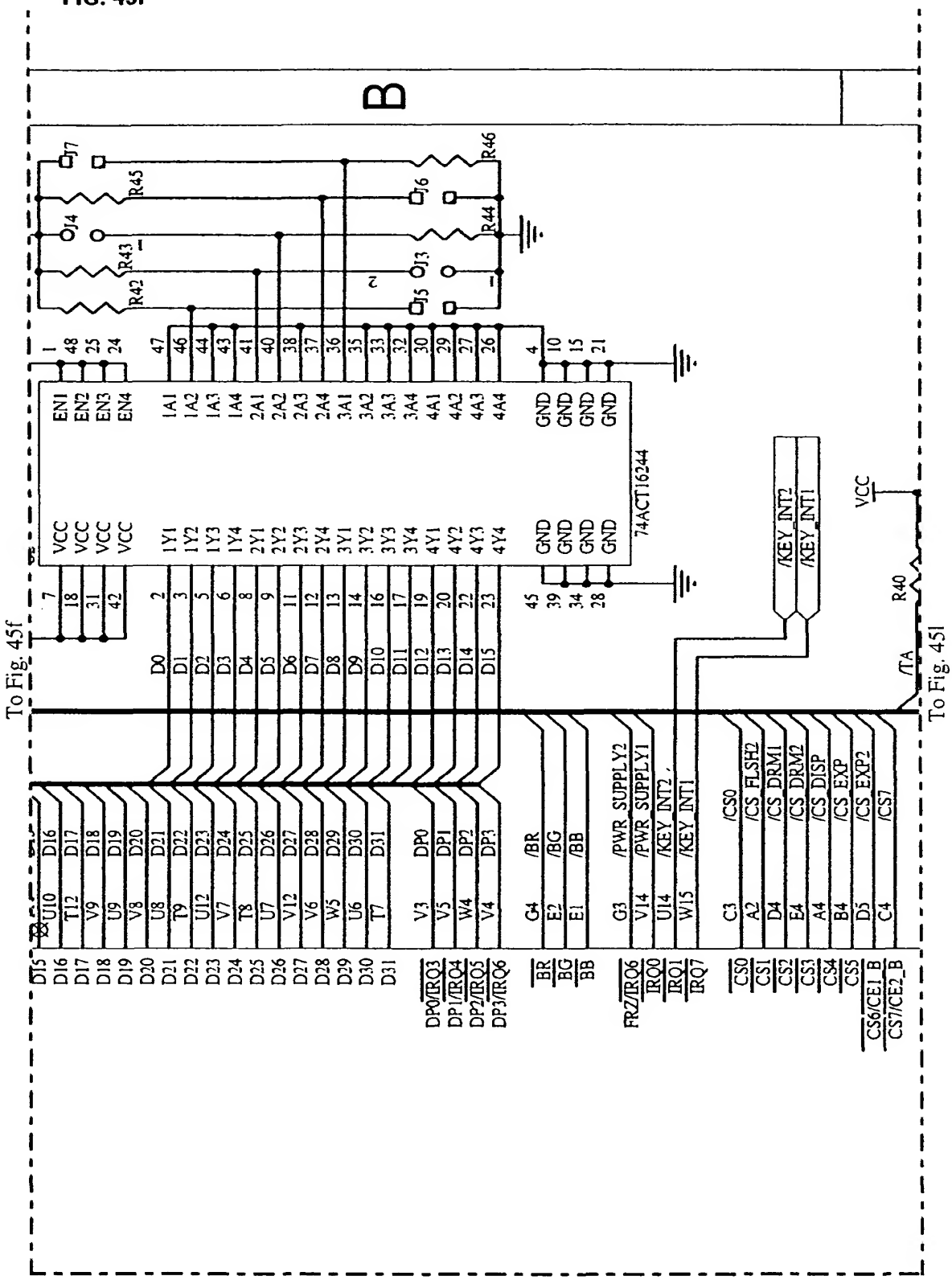

B
74ACT16244
VCC
R40
/KEY_INT2
/KEY_INT1
/TA
To Fig. 45f
To Fig. 45l
To Fig. 45h

FIG. 45j

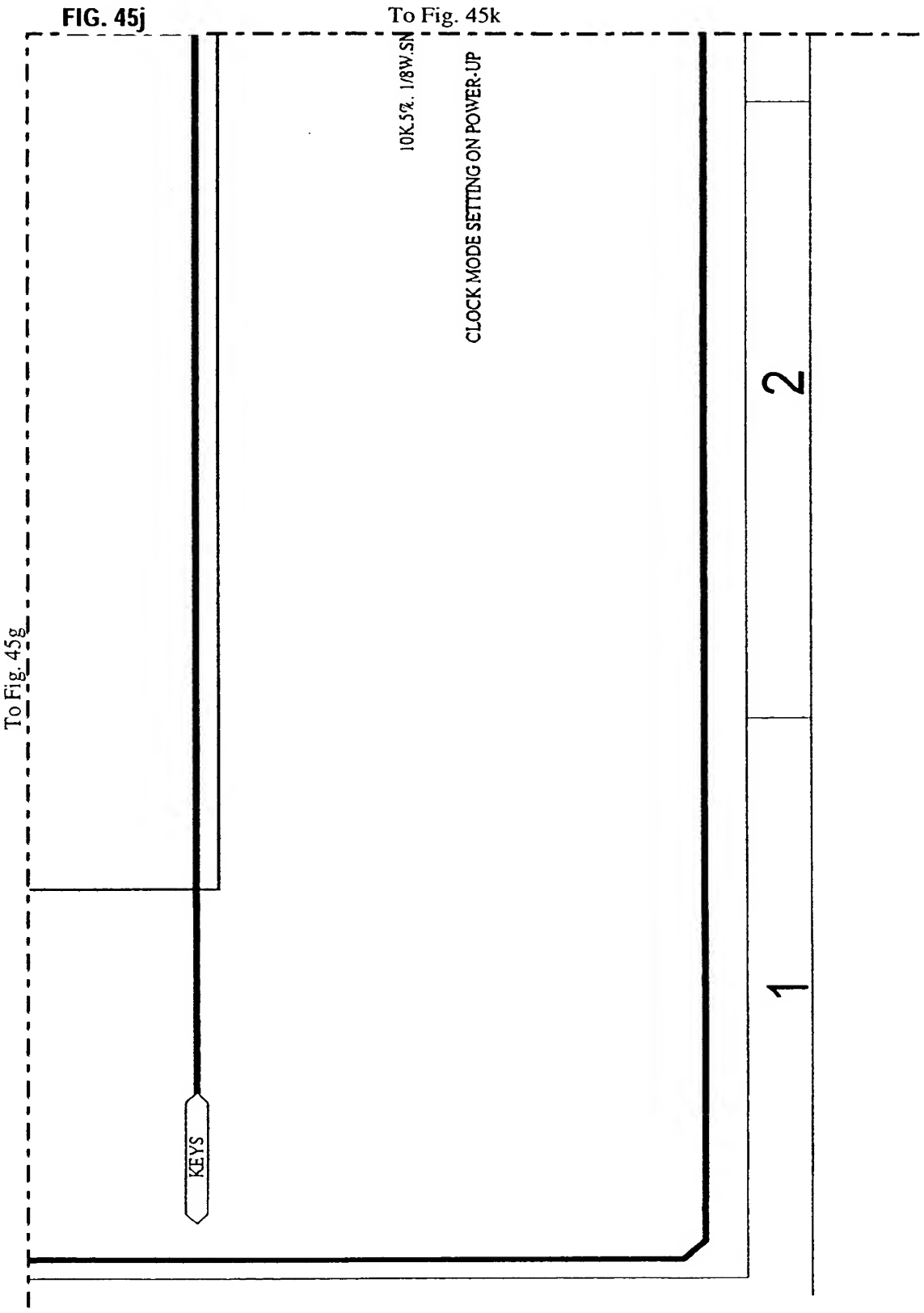
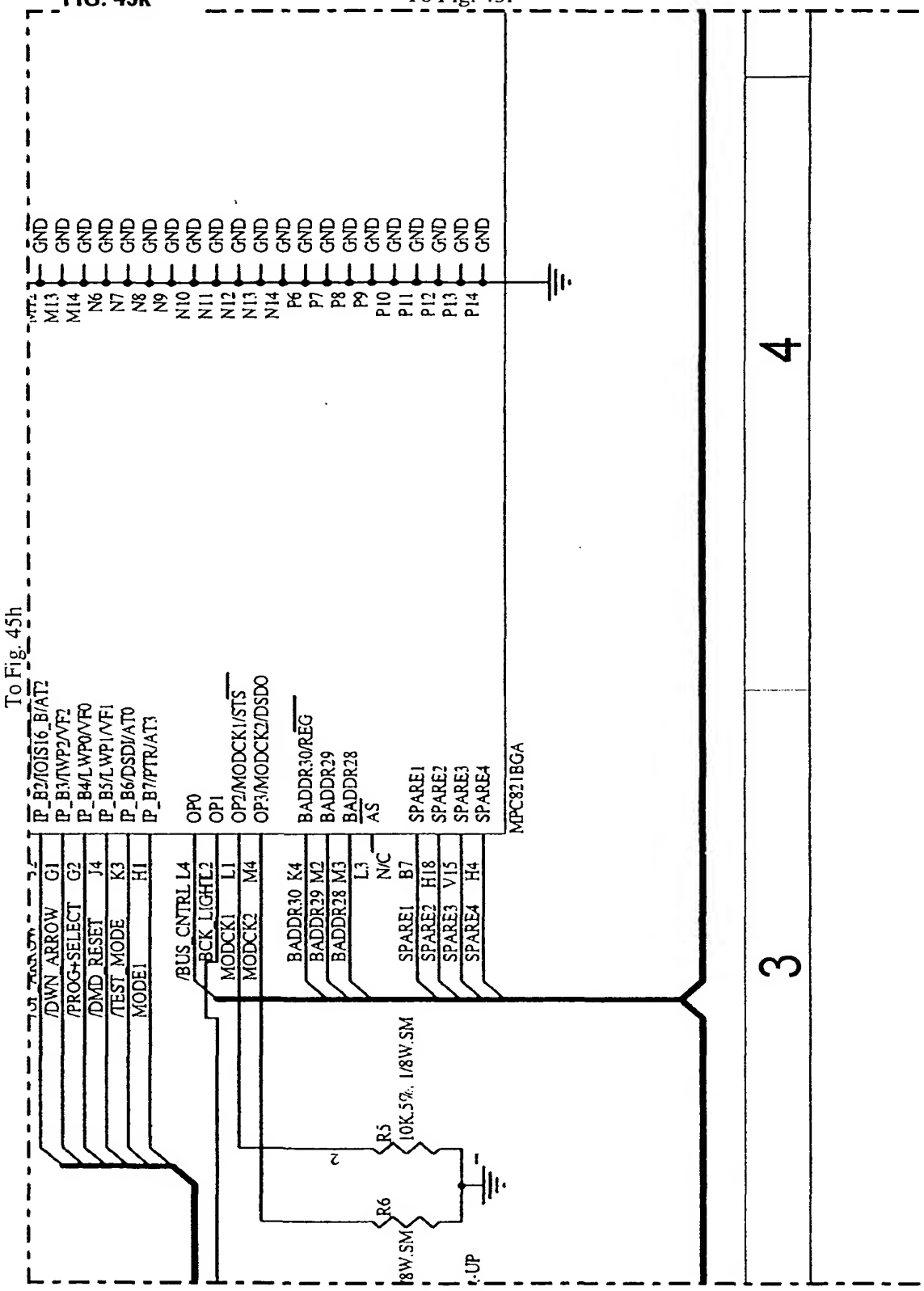

To Fig. 45k
To Fig. 45g
10K.5%. 1/8W.SN
CLOCK MODE SETTING ON POWER-UP
KEYS
2
1

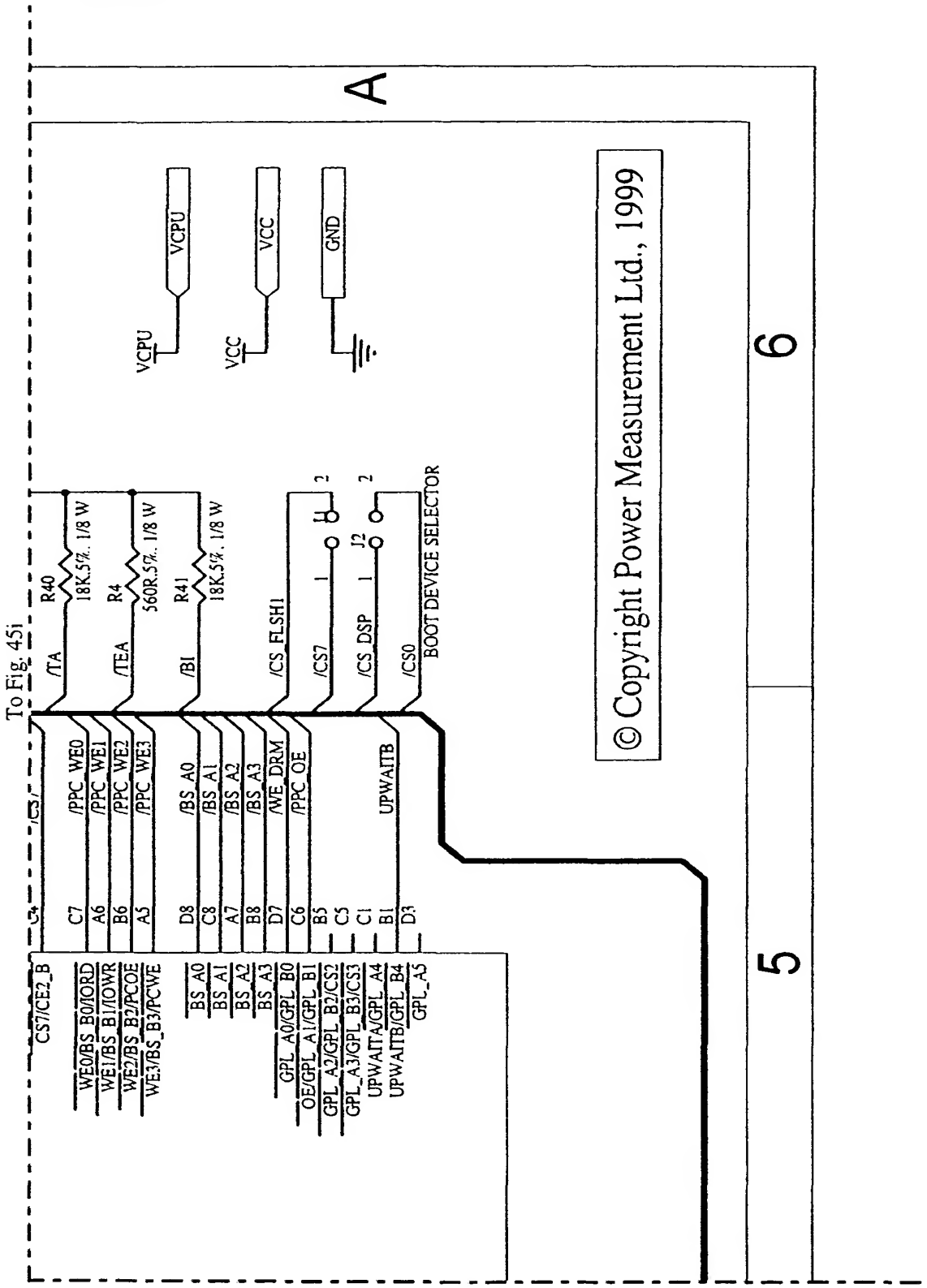
FIG. 45k

To Fig. 45l



To Fig. 45j

FIG. 45l



To Fig. 45k

FIG. 46a

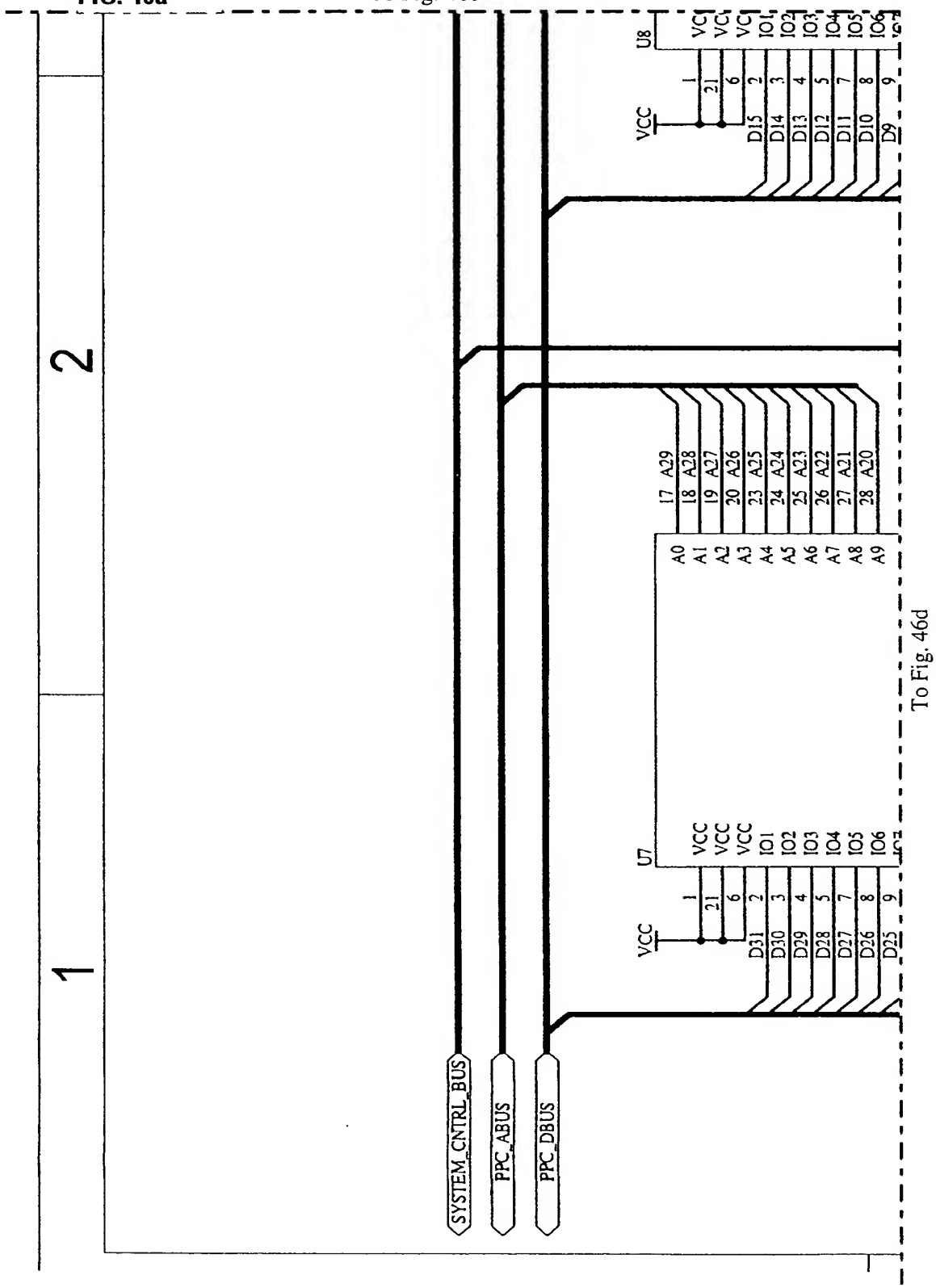

To Fig. 46b
To Fig. 46d
2
1
U8
U7
VCC
SYSTEM_CNTRL_BUS
PPC_ABUS
PPC_DBUS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A20
A21
A22
A23
A24
A25
A26
A27
A28
A29
D9
D10
D11
D12
D13
D14
D15
D25
D26
D27
D28
D29
D30
D31

FIG. 46b

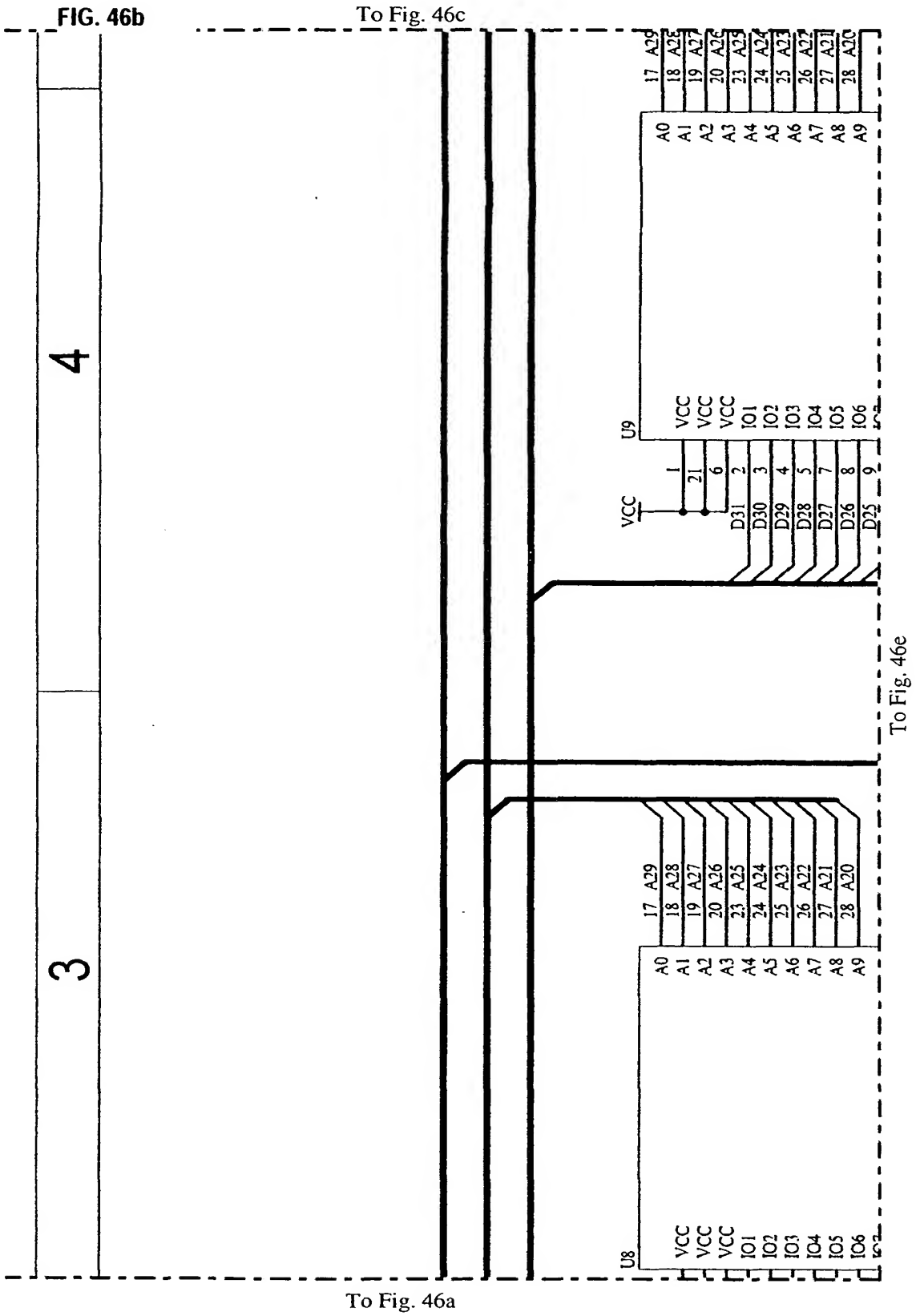

To Fig. 46c
4
3
U9
U8
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A20
A21
A22
A23
A24
A25
A26
A27
A28
A29
IO1
IO2
IO3
IO4
IO5
IO6
D25
D26
D27
D28
D29
D30
D31
To Fig. 46e
To Fig. 46a

FIG. 46c

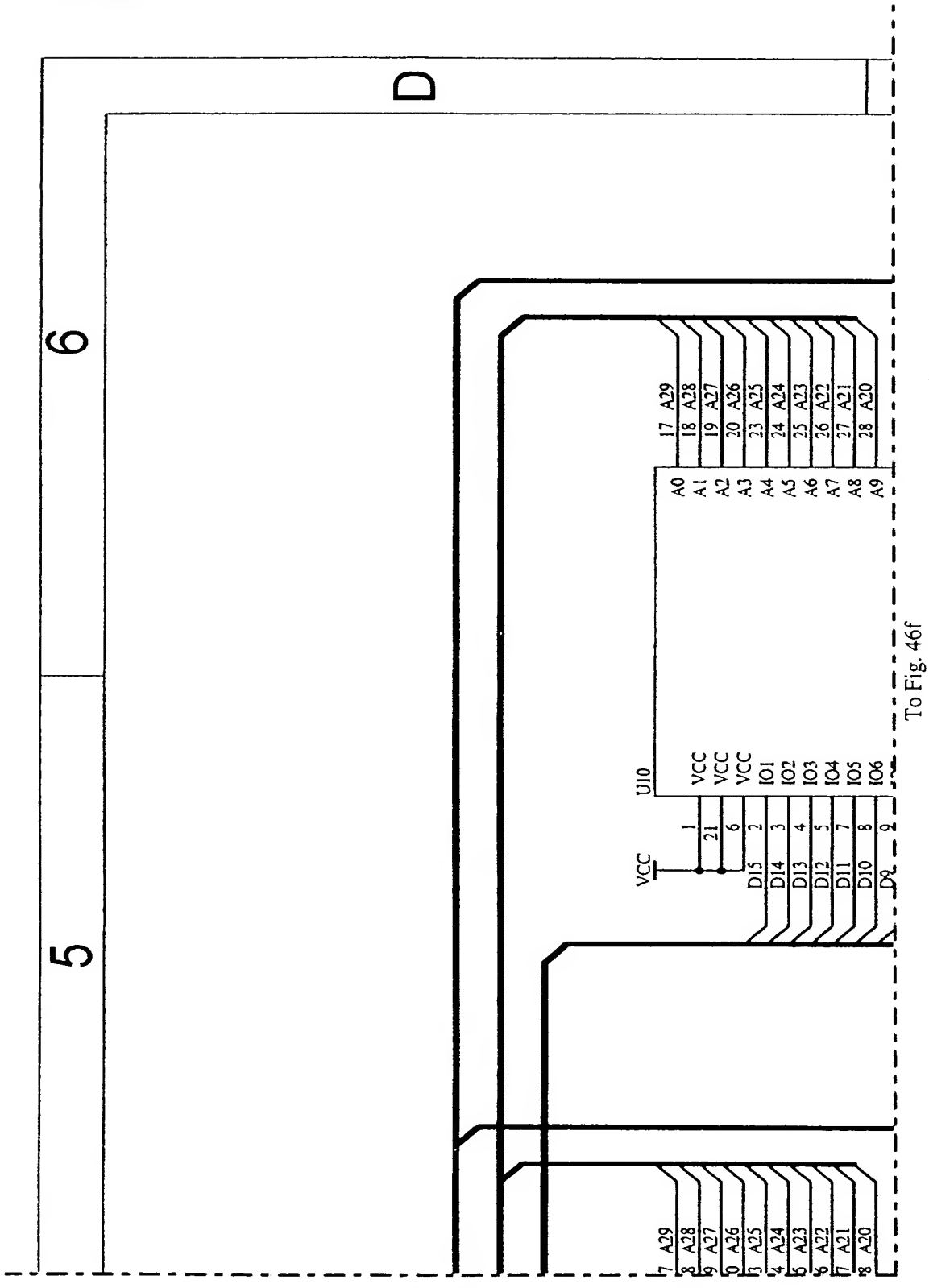

D
6
5
U10
VCC
VCC
VCC
IO1
IO2
IO3
IO4
IO5
IO6
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A29
A28
A27
A26
A25
A24
A23
A22
A21
A20
D15
D14
D13
D12
D11
D10
To Fig. 46f
To Fig. 46b

FIG. 46d

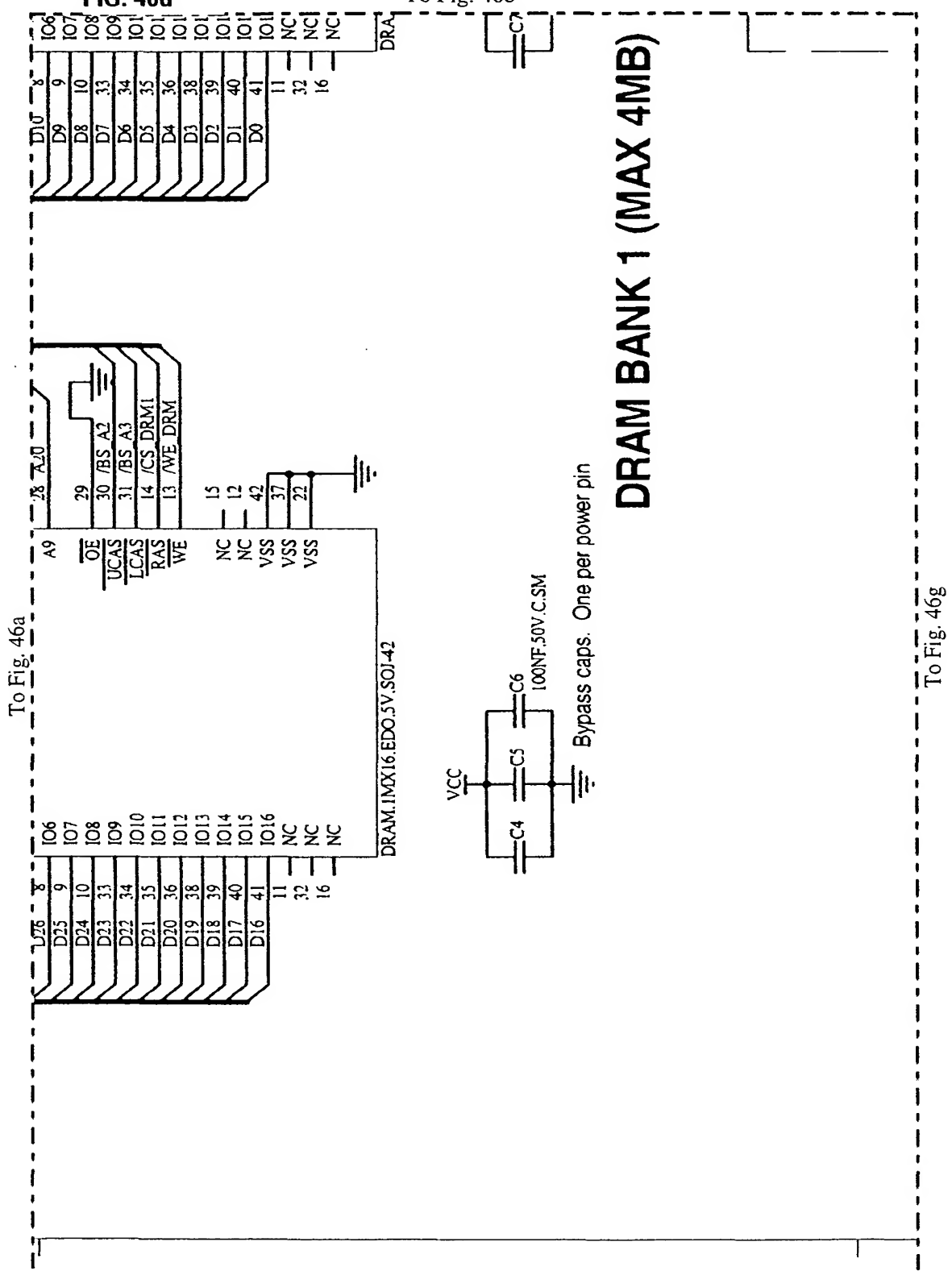

To Fig. 46e
DRAM BANK 1 (MAX 4MB)
To Fig. 46a
To Fig. 46g
DRAM.IMX16.EDO.5V.SOJ-42
Bypass caps. One per power pin
100NF.50V.C.SM
C4
C5
C6
C7
VCC
A9
OE
UCAS
LCAS
RAS
WE
NC
VSS
/BS A2
/BS A3
/CS DRM1
/WE DRM
DRA
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
IO16
D26
D25
D24
D23
D22
D21
D20
D19
D18
D17
D16
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0

FIG. 46e

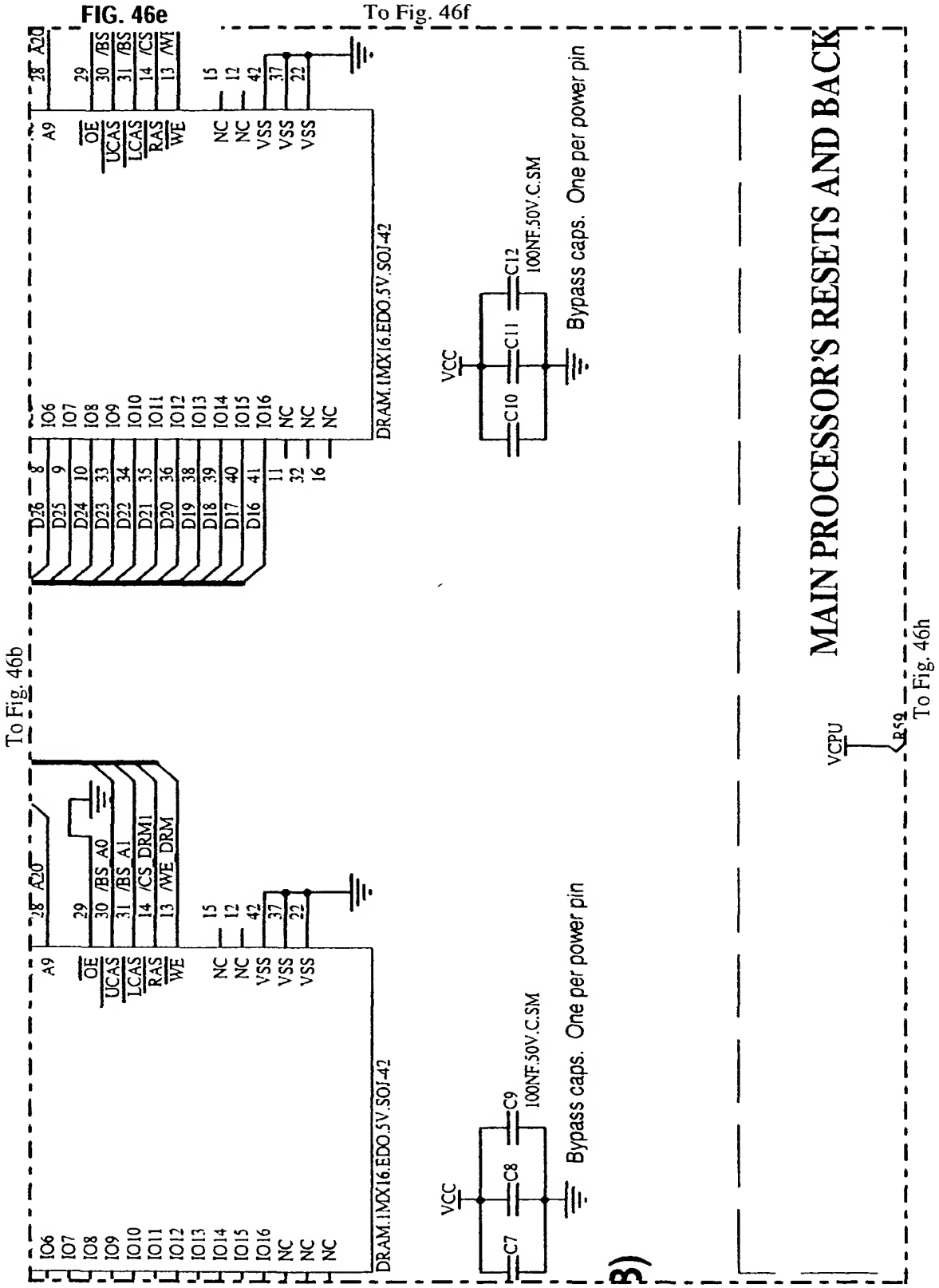

To Fig. 46f
To Fig. 46b
To Fig. 46d
To Fig. 46h
DRAM.1MX16.EDO.5V.SOJ-42
Bypass caps. One per power pin
100NF.50V.C.SM
VCC
VCPU
MAIN PROCESSOR'S RESETS AND BACK
A20
A9
OE
UCAS
LCAS
RAS
WE
NC
VSS
/BS
/CS
/WE
A0
A1
DRM1
DRM
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
IO16
D26
D25
D24
D23
D22
D21
D20
D19
D18
D17
D16
C7
C8
C9
C10
C11
C12

FIG. 46f

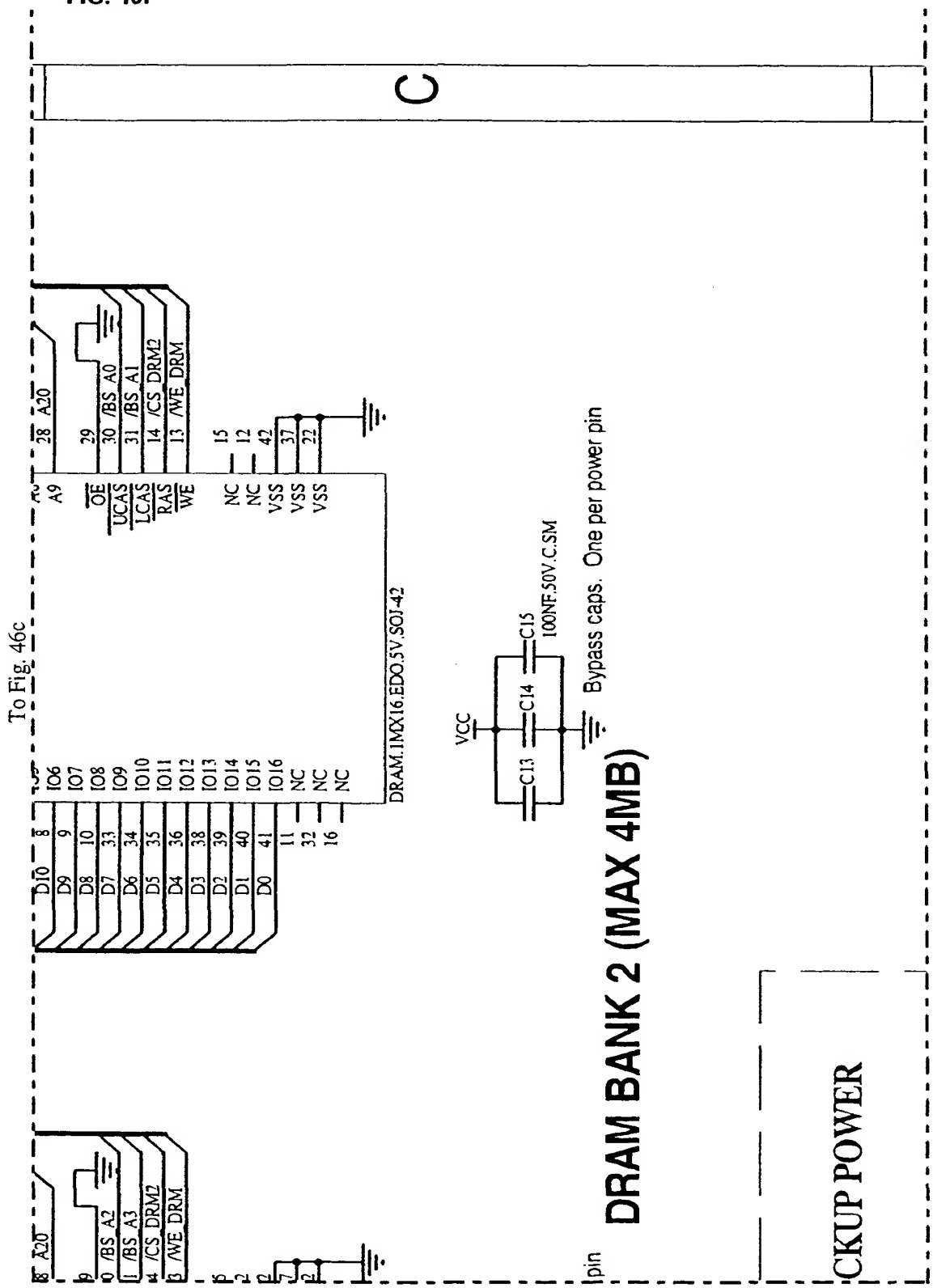
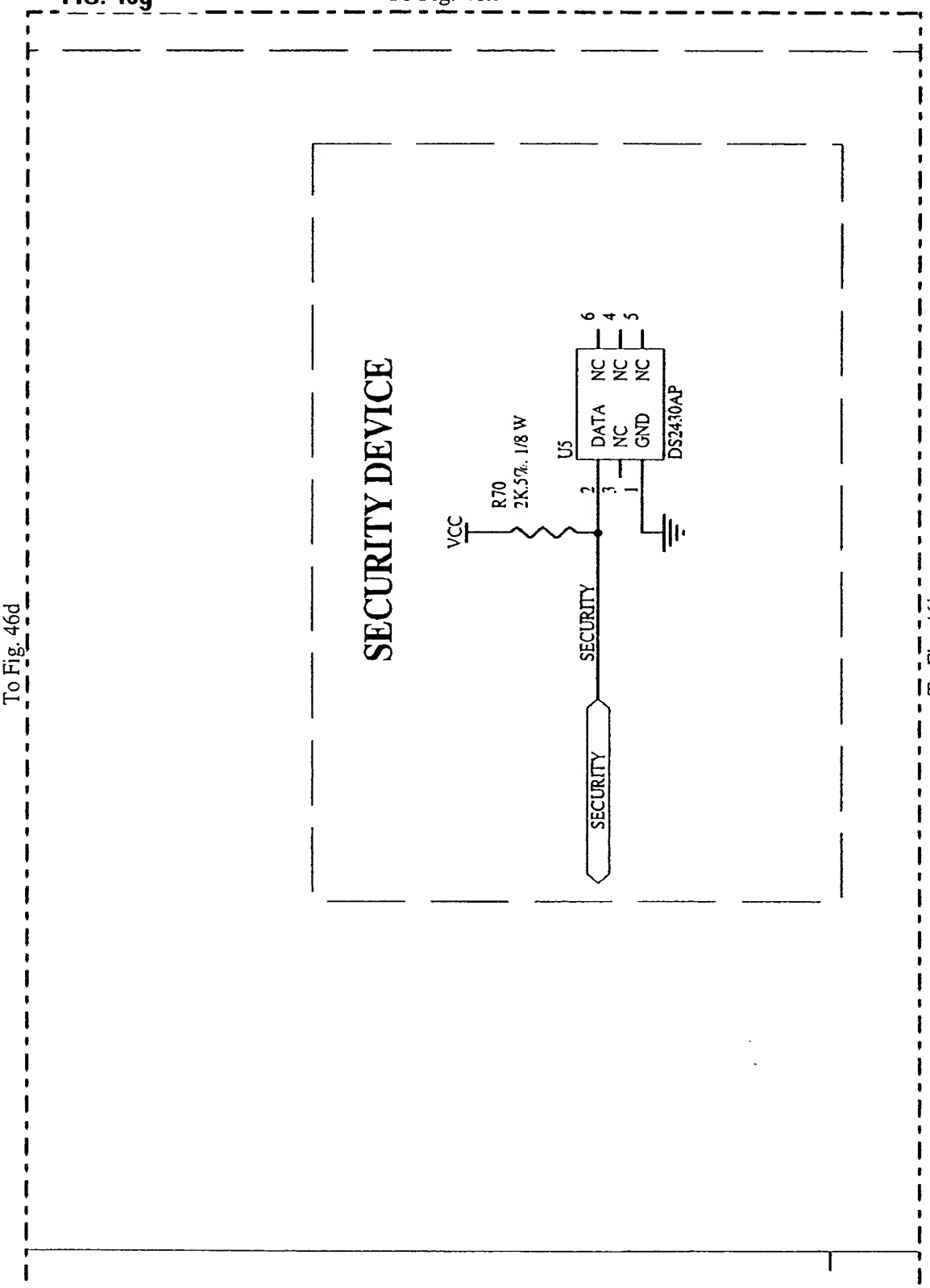

C
To Fig. 46c
To Fig. 46i
To Fig. 46e
DRAM BANK 2 (MAX 4MB)
CKUP POWER
Bypass caps. One per power pin
C15
100NF.50V.C.SM
C14
C13
VCC
DRAM.1MX16.EDO.5V.SOJ-42
A20
/BS_A2
/BS_A3
/CS_DRM2
/WE_DRM
/BS_A0
/BS_A1
/CS_DRM2
/WE_DRM
OE
UCAS
LCAS
RAS
WE
NC
NC
VSS
VSS
VSS
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
IO16
NC
NC
NC

FIG. 46g

To Fig. 46h



To Fig. 46d

To Fig. 46j

FIG. 46h

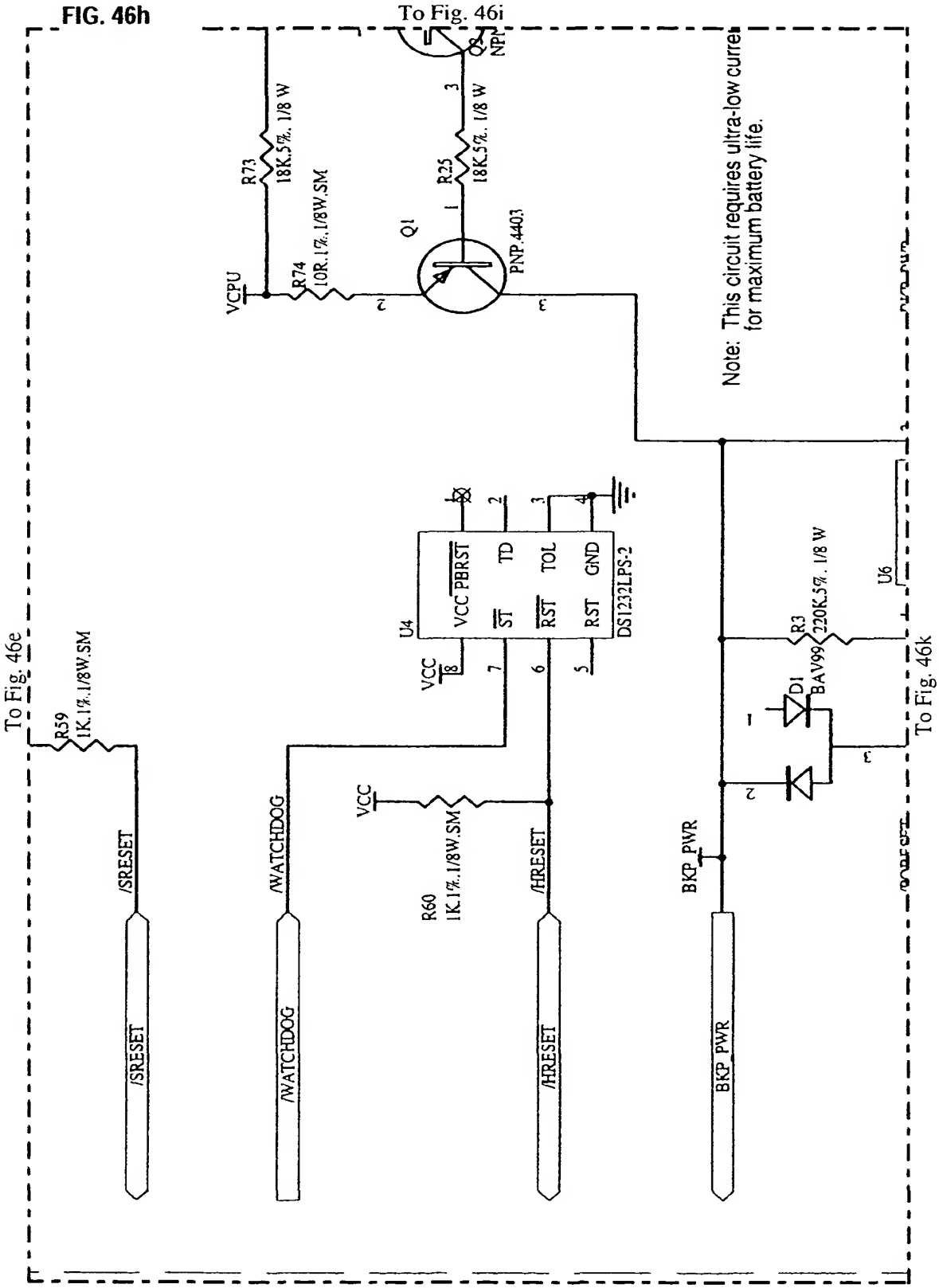
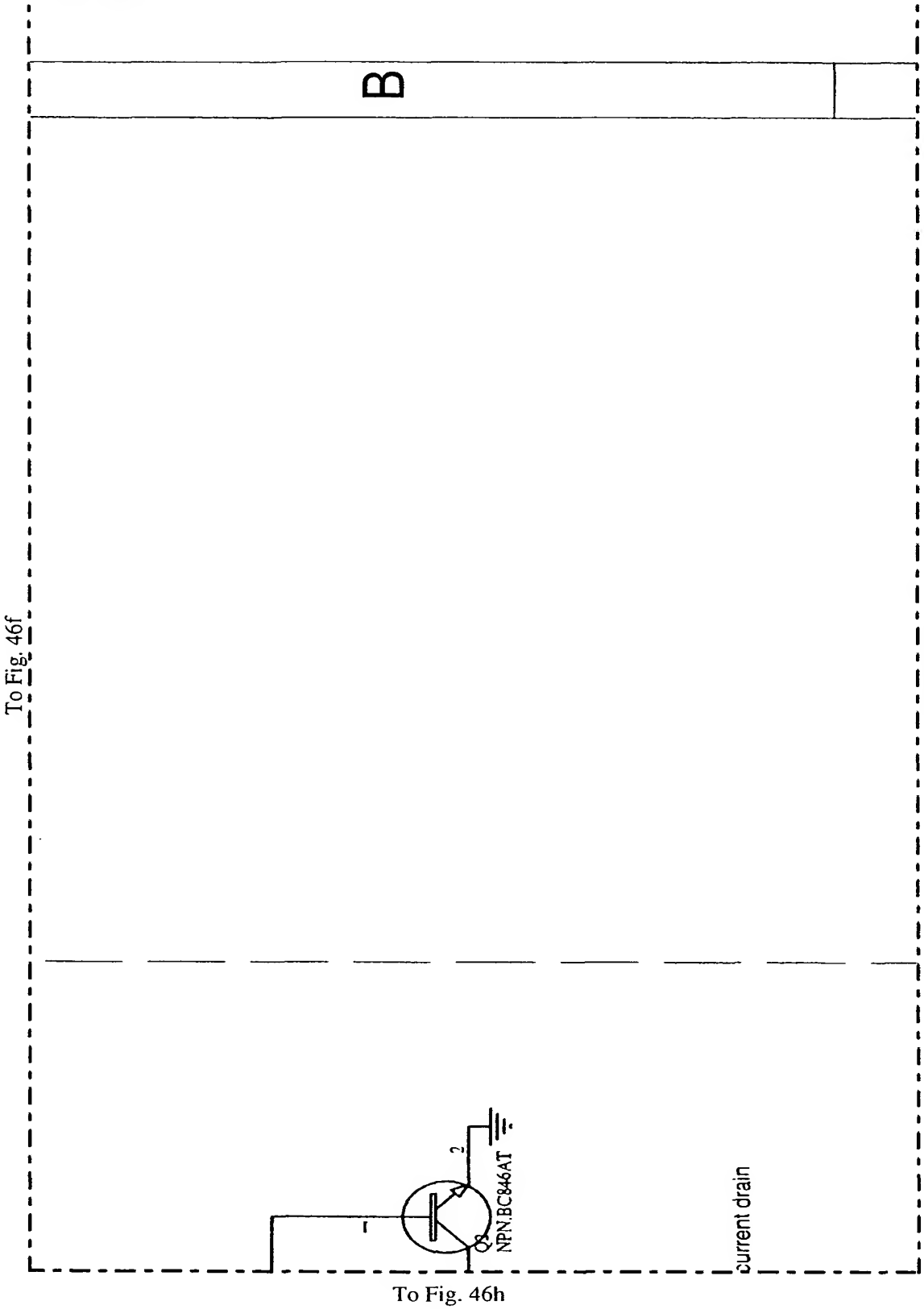

To Fig. 46i
To Fig. 46e
To Fig. 46k
To Fig. 46g
R73
18K.5%. 1/8 W
R74
10R.1%.1/8W.SM
VCPU
Q1
PNP.4403
R25
18K.5%. 1/8 W
NPN
Note: This circuit requires ultra-low current for maximum battery life.
U4
DS1232LPS:2
VCC PBRST
TD
TOL
GND
ST
RST
RST
VCC
R59
1K.1%.1/8W.SM
/SRESET
/WATCHDOG
R60
1K.1%.1/8W.SM
/HRESET
BKP PWR
U6
R3
220K.5%. 1/8 W
D1
BAV99

FIG. 46i



To Fig. 46h

FIG. 46j

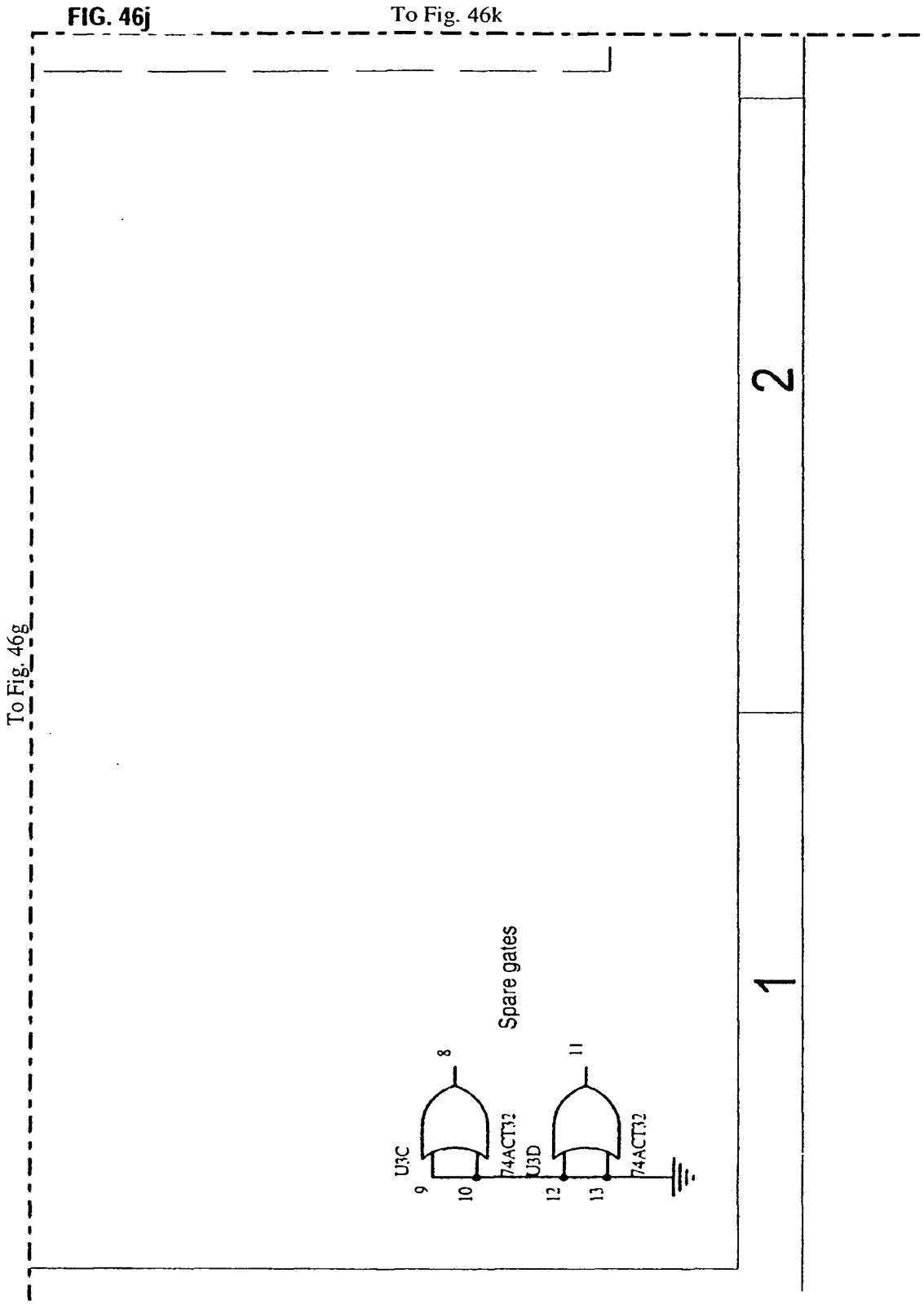
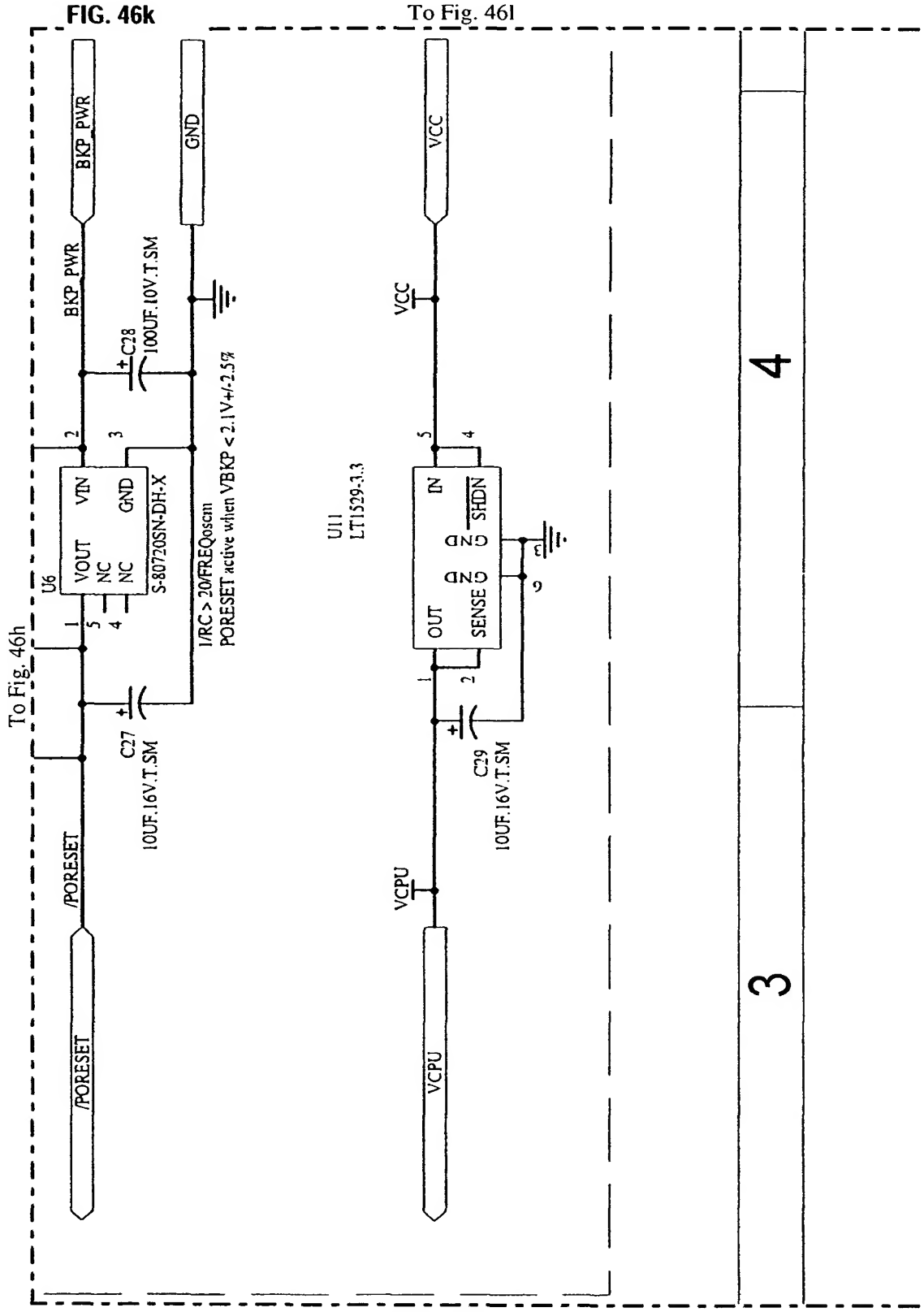

To Fig. 46k
To Fig. 46g
2
1
Spare gates
U3C
74ACT32
U3D
74ACT32
8
9
10
11
12
13

FIG. 46k



To Fig. 46j

FIG. 46l

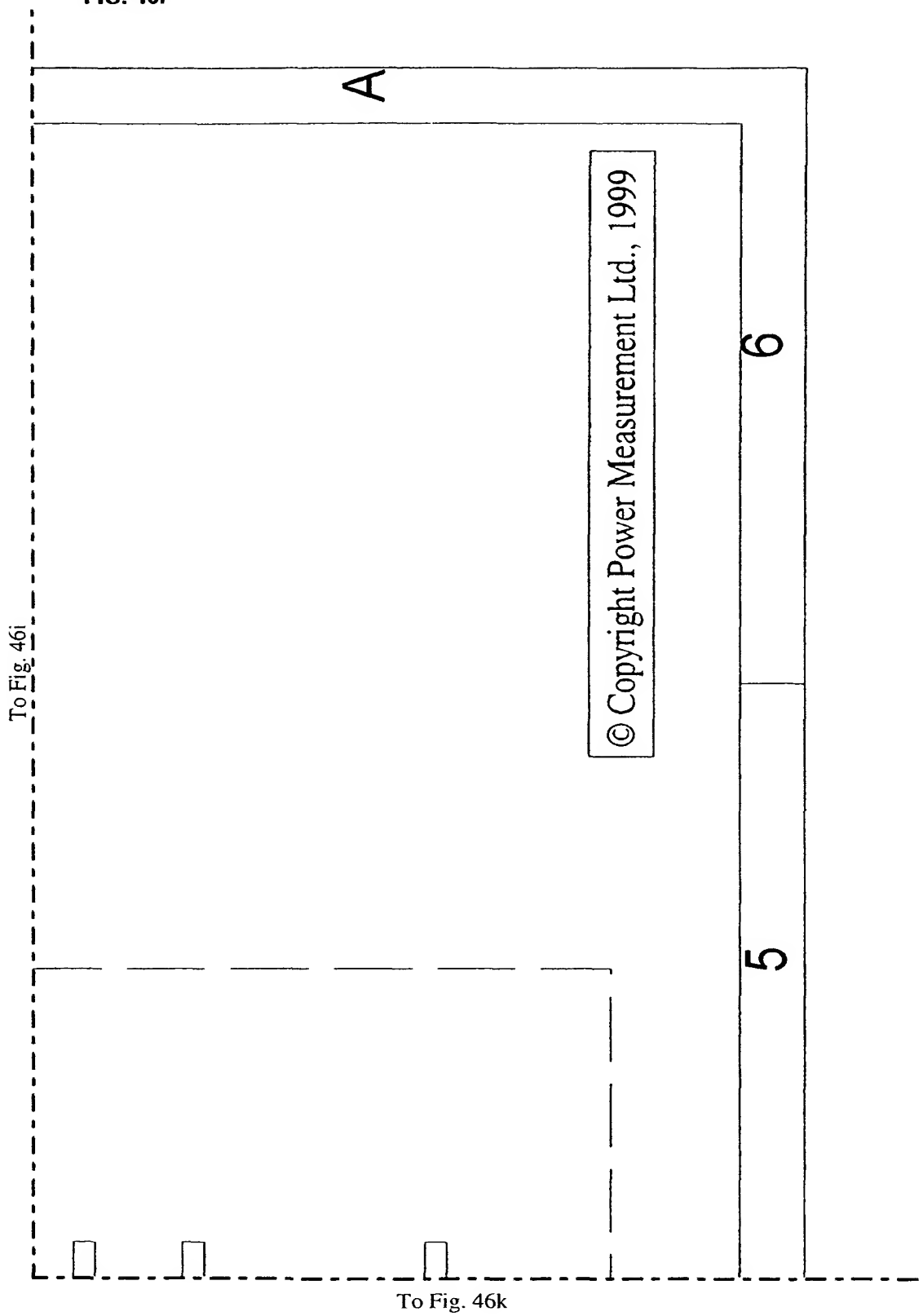

A
6
5
© Copyright Power Measurement Ltd., 1999
To Fig. 46i
To Fig. 46k

FIG. 47a

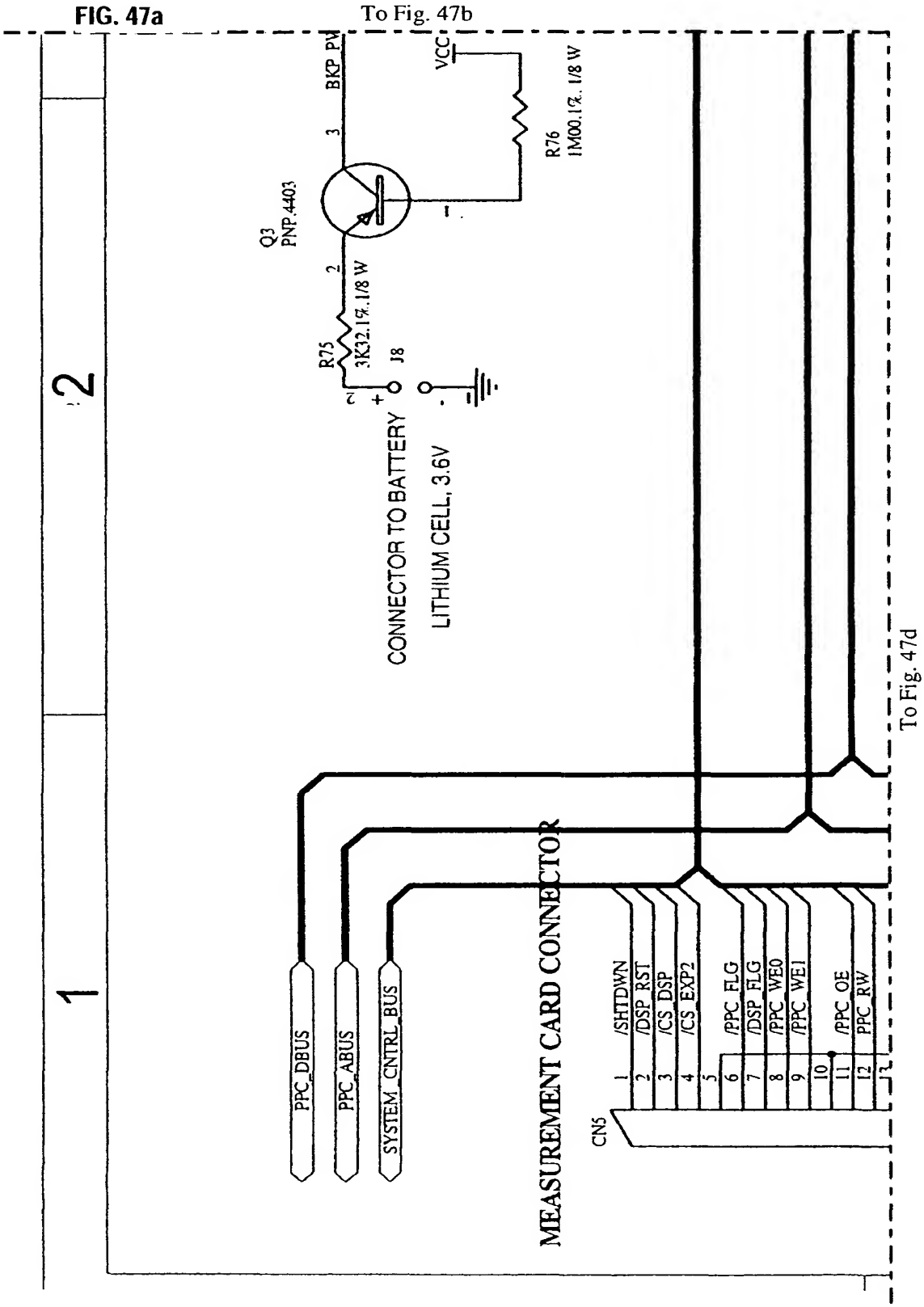

To Fig. 47b
BKP PW
VCC
R76
1M00.1%. 1/8 W
Q3
PNP.4403
R75
3K32.1%.1/8 W
J8
CONNECTOR TO BATTERY
LITHIUM CELL, 3.6V
PPC_DBUS
PPC_ABUS
SYSTEM_CNTRL_BUS
MEASUREMENT CARD CONNECTOR
CN5
/SHTDWN
/DSP_RST
/CS_DSP
/CS_EXP2
/PPC_FLG
/DSP_FLG
/PPC_WE0
/PPC_WE1
/PPC_OE
PPC_RW
To Fig. 47d

FIG. 47b

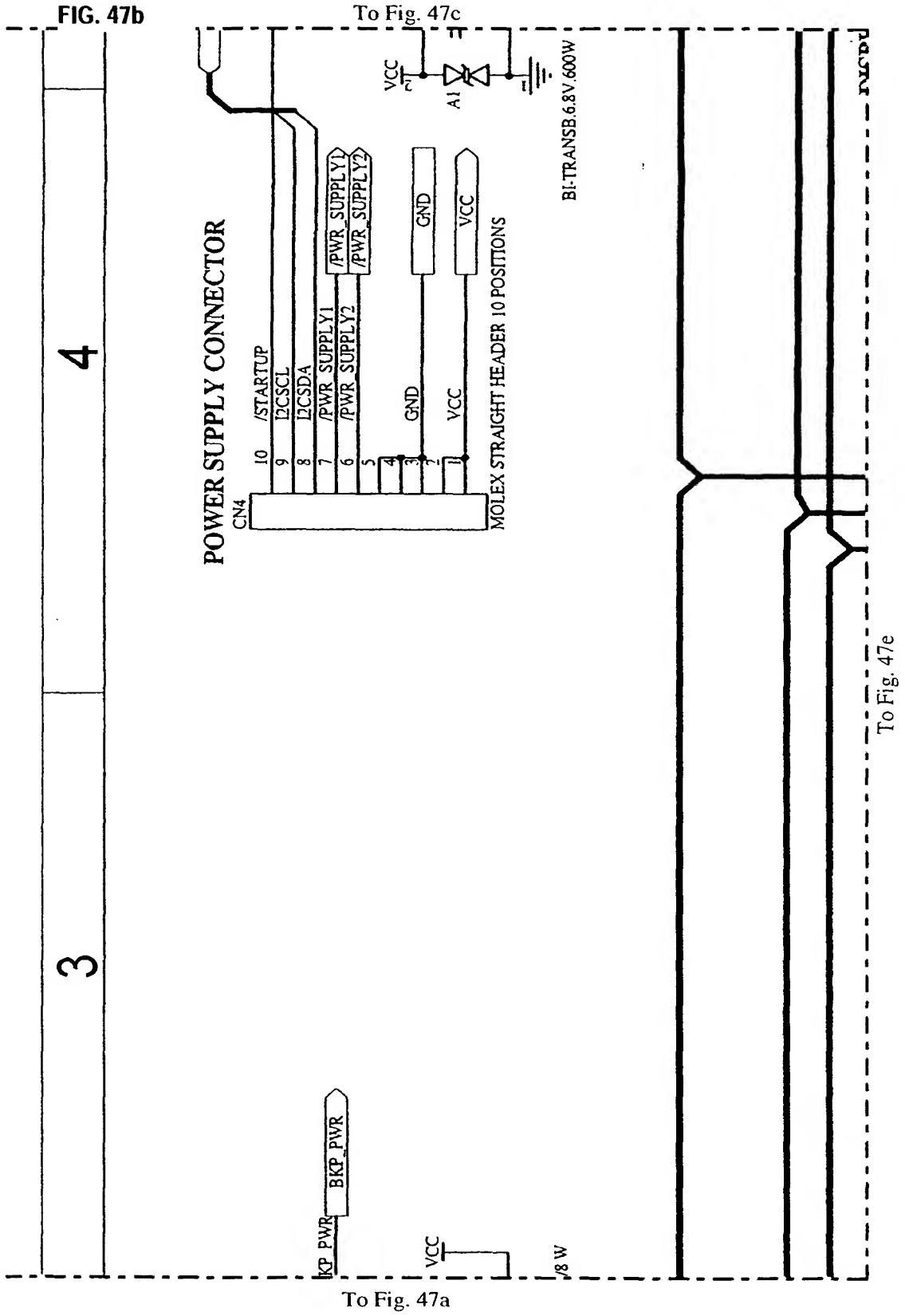

To Fig. 47c
4
3
POWER SUPPLY CONNECTOR
CN4
10 /STARTUP
9 I2CSCL
8 I2CSDA
7 /PWR_SUPPLY1
6 /PWR_SUPPLY2
5
4
3
2
1
GND
VCC
MOLEX STRAIGHT HEADER 10 POSITIONS
/PWR_SUPPLY1
/PWR_SUPPLY2
GND
VCC
VCC
A1
BI-TRANSB 6.8V, 600W
BKP_PWR
BKP PWR
VCC
/8 W
To Fig. 47e
To Fig. 47a

FIG. 47c

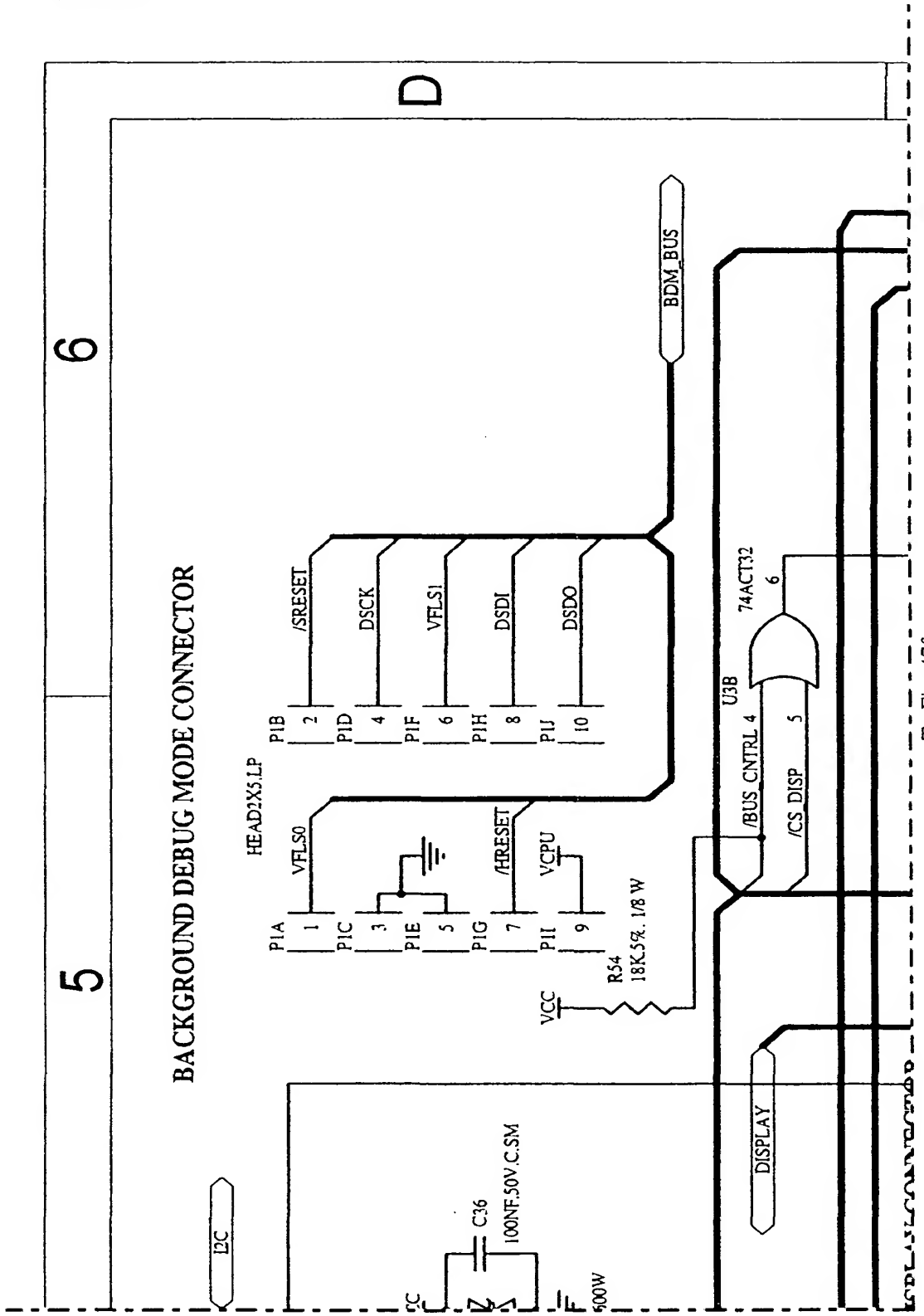

D
6
5
BACKGROUND DEBUG MODE CONNECTOR
BDM_BUS
/SRESET
DSCK
VFLS1
DSDI
DSDO
P1B 2
P1D 4
P1F 6
P1H 8
P1J 10
HEAD2X5.LP
VFLS0
/HRESET
VCPU
P1A 1
P1C 3
P1E 5
P1G 7
P1I 9
R54
18K.5%. 1/8 W
VCC
74ACT32
U3B
6
/BUS_CNTRL 4
/CS_DISP 5
DISPLAY
I2C
C36
100NF.50V.C.SM
To Fig. 47f
To Fig. 47b

FIG. 47d

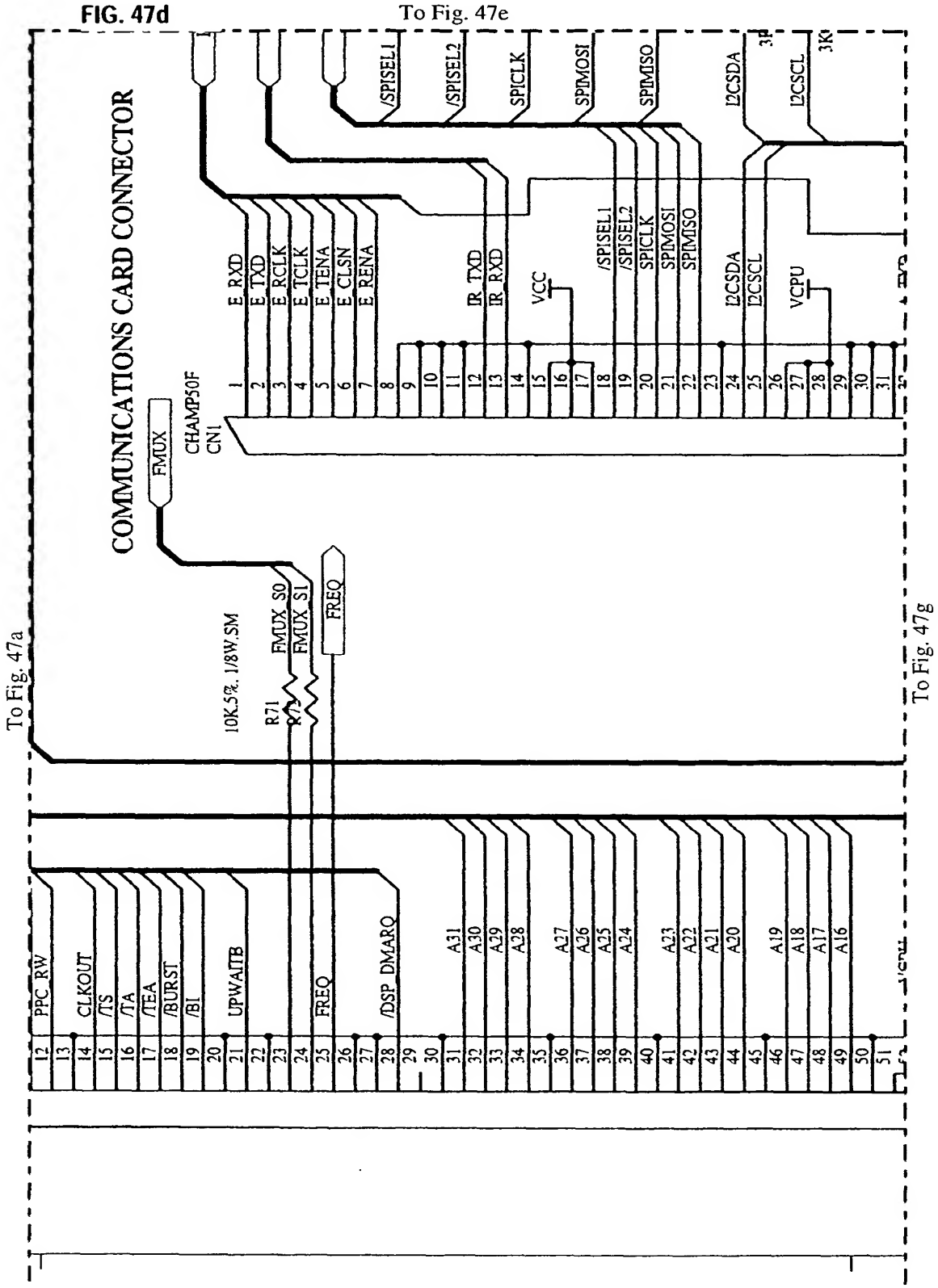

To Fig. 47e
COMMUNICATIONS CARD CONNECTOR
CHAMP50F
CN1
FMUX
E_RXD
E_TXD
E_RCLK
E_TCLK
E_TENA
E_CLSN
E_RENA
IR_TXD
IR_RXD
VCC
/SPISEL1
/SPISEL2
SPICLK
SPIMOSI
SPIMISO
I2CSDA
I2CSCL
VCPU
10K,5%, 1/8W,SM
R71
R72
FMUX_S0
FMUX_S1
FREQ
PPC_RW
CLKOUT
/TS
/TA
/TEA
/BURST
/BI
UPWAITB
/DSP_DMARQ
A31
A30
A29
A28
A27
A26
A25
A24
A23
A22
A21
A20
A19
A18
A17
A16
To Fig. 47a
To Fig. 47g

FIG. 47e

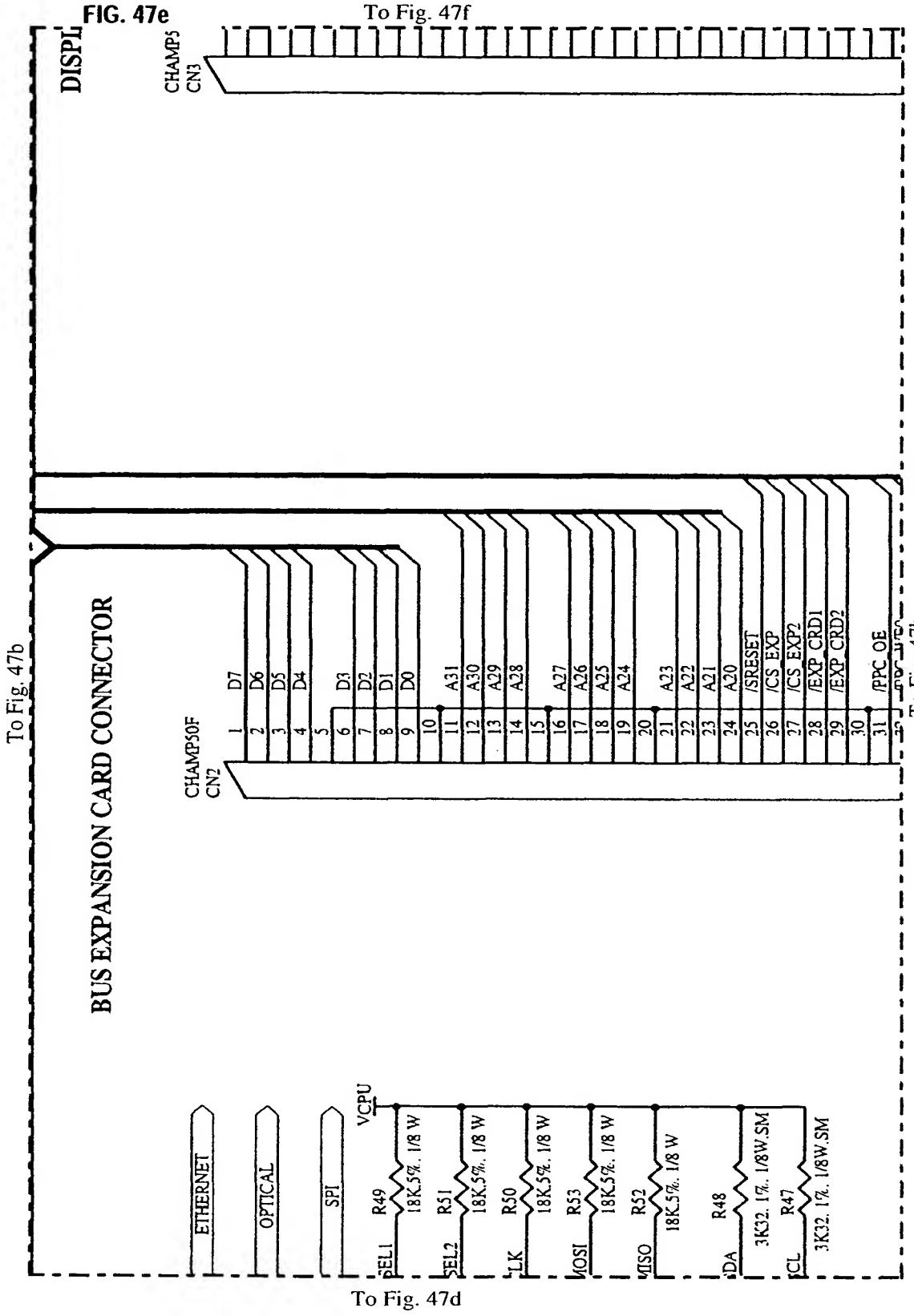

To Fig. 47f
DISPL
CHAMP5
CN3
To Fig. 47b
BUS EXPANSION CARD CONNECTOR
CHAMP50F
CN2
D7
D6
D5
D4
D3
D2
D1
D0
A31
A30
A29
A28
A27
A26
A25
A24
A23
A22
A21
A20
/SRESET
/CS_EXP
/CS_EXP2
/EXP_CRD1
/EXP_CRD2
/PPC_OE
To Fig. 47h
ETHERNET
OPTICAL
SPI
VCPU
R49
18K.5%. 1/8 W
R51
18K.5%. 1/8 W
R50
18K.5%. 1/8 W
R53
18K.5%. 1/8 W
R52
18K.5%. 1/8 W
R48
3K32. 1%. 1/8W.SM
R47
3K32. 1%. 1/8W.SM
To Fig. 47d

FIG. 47f

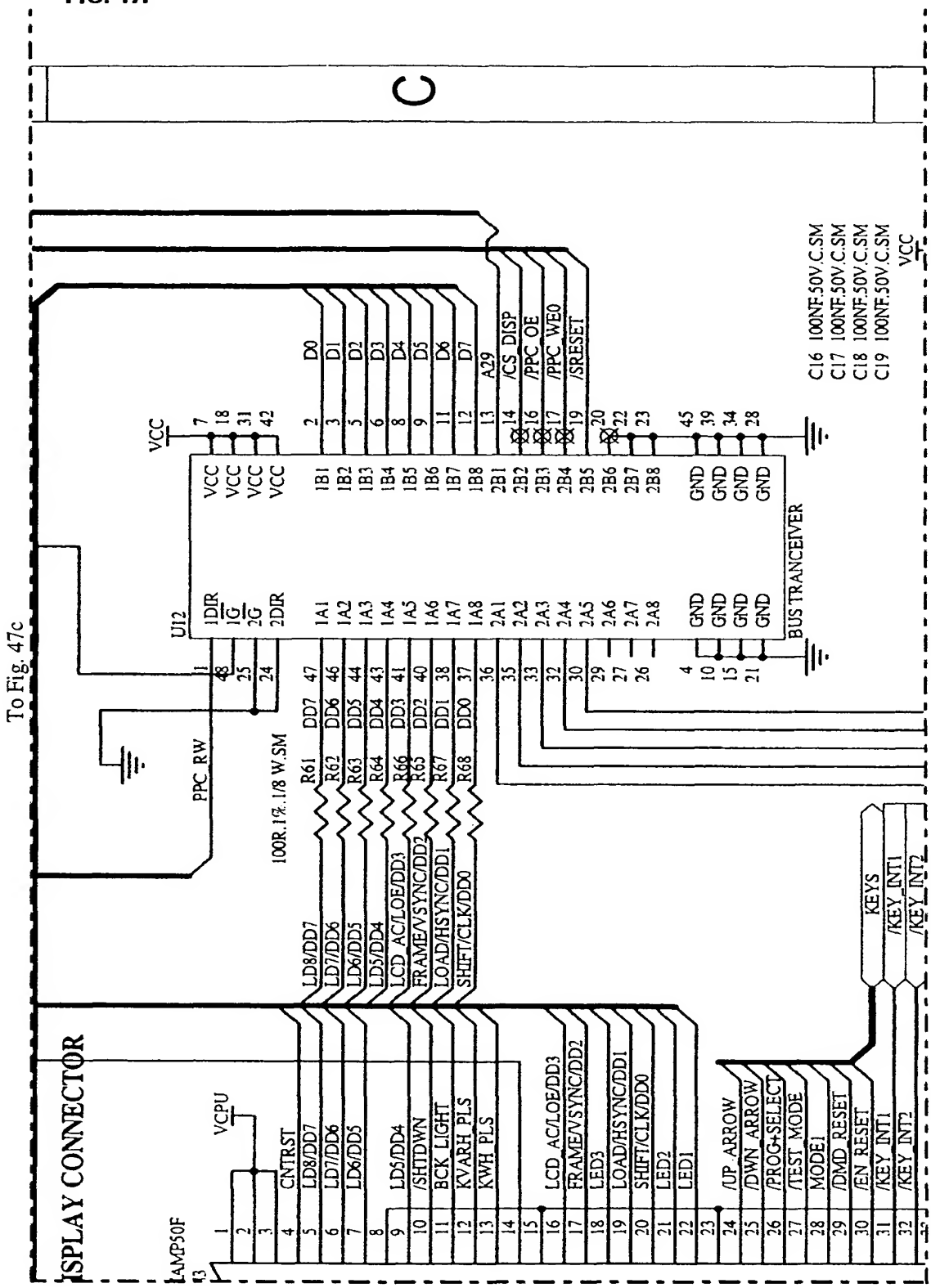

To Fig. 47c
To Fig. 47i
To Fig. 47e
U12
BUS TRANCEIVER
VCC
GND
100R.1%.1/8 W.SM
PPC_RW
/CS_DISP
/PPC_OE
/PPC_WE0
/SRESET
C16 100NF.50V.C.SM
C17 100NF.50V.C.SM
C18 100NF.50V.C.SM
C19 100NF.50V.C.SM
KEYS
/KEY_INT1
/KEY_INT2
SPLAY CONNECTOR
VCPU
CNTRST
LD8/DD7
LD7/DD6
LD6/DD5
LD5/DD4
/SHTDWN
BCK_LIGHT
KVARH_PLS
KWH_PLS
LCD_AC/LOE/DD3
FRAME/VSYNC/DD2
LOAD/HSYNC/DD1
SHIFT/CLK/DD0
LED3
LED2
LED1
/UP_ARROW
/DWN_ARROW
/PROG+SELECT
/TEST_MODE
MODE1
/DMD_RESET
/EN_RESET
/KEY_INT1
/KEY_INT2

FIG. 47g

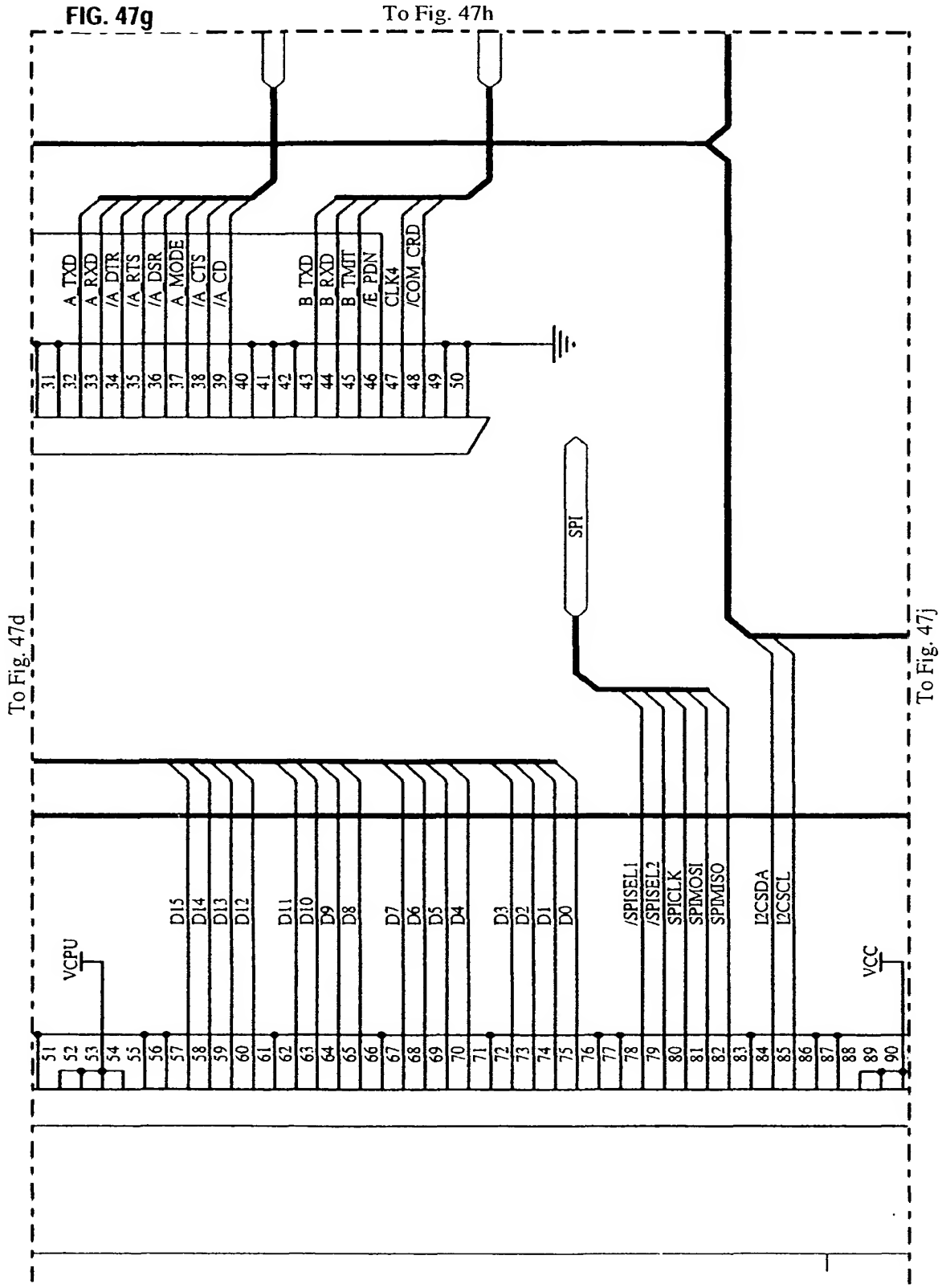

To Fig. 47h
To Fig. 47d
To Fig. 47j
A_TXD
A_RXD
/A_DTR
/A_RTS
/A_DSR
A_MODE
/A_CTS
/A_CD
B_TXD
B_RXD
B_TMIT
/E_PDN
CLK4
/COM_CRD
SPI
VCPU
VCC
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
/SPISEL1
/SPISEL2
SPICLK
SPIMOSI
SPIMISO
I2CSDA
I2CSCL

FIG. 47h

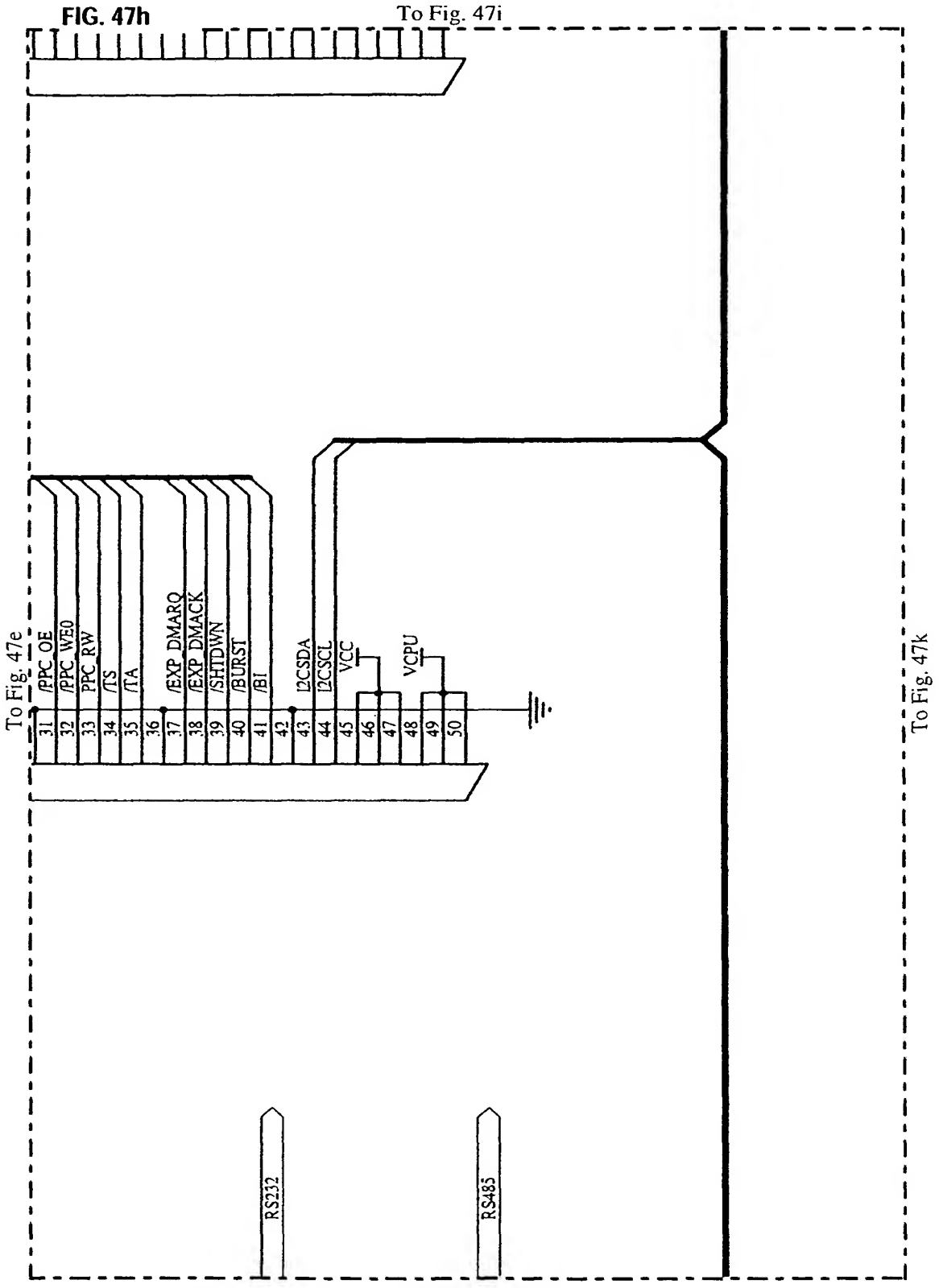
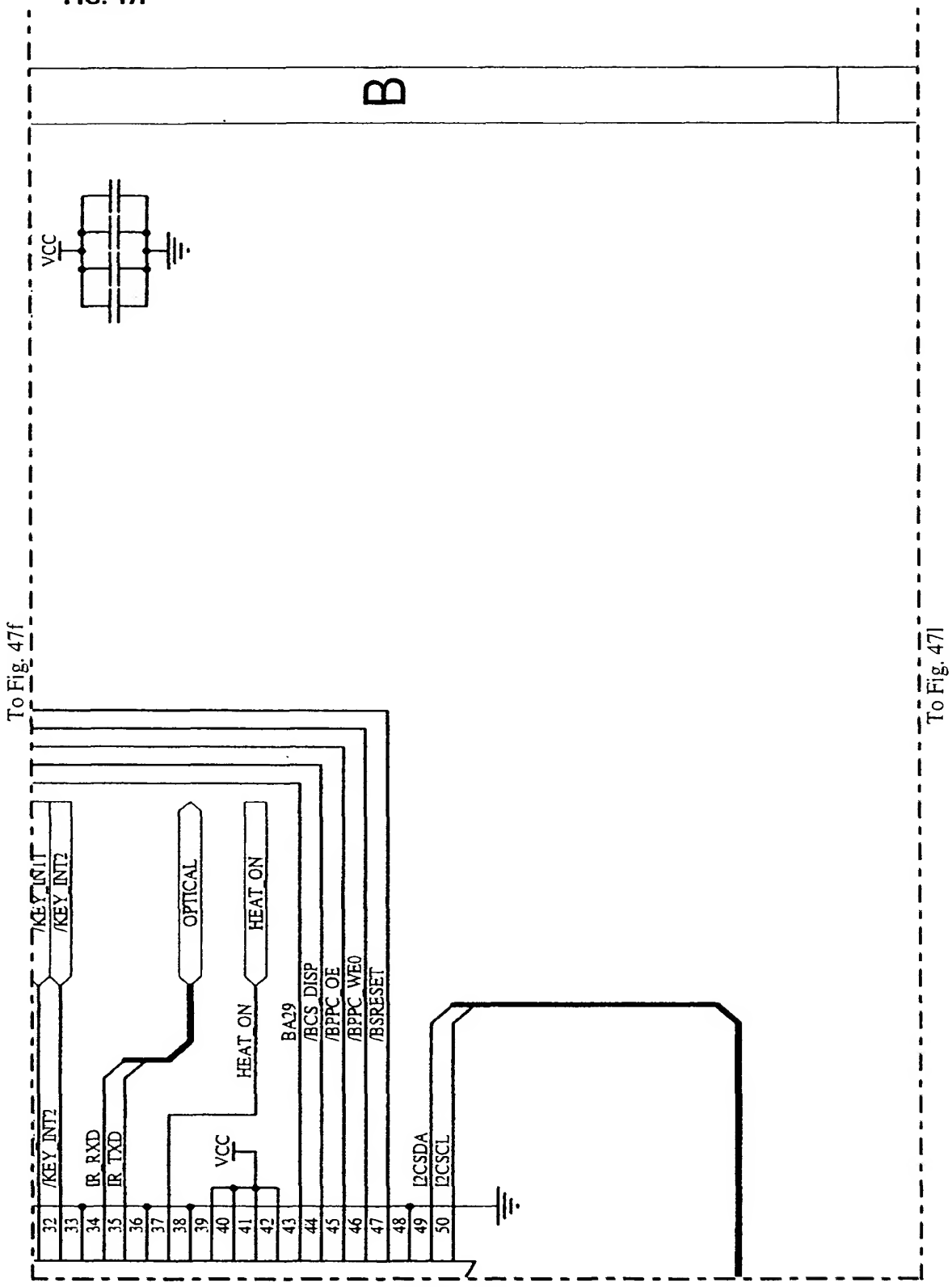

To Fig. 47i
To Fig. 47e
/PPC_OE
/PPC_WE0
PPC_RW
/TS
/TA
/EXP_DMARQ
/EXP_DMACK
/SHTDWN
/BURST
/BI
I2CSDA
I2CSCL
VCC
VCPU
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
RS232
RS485
To Fig. 47k
To Fig. 47g

FIG. 47i



To Fig. 47h

FIG. 47j

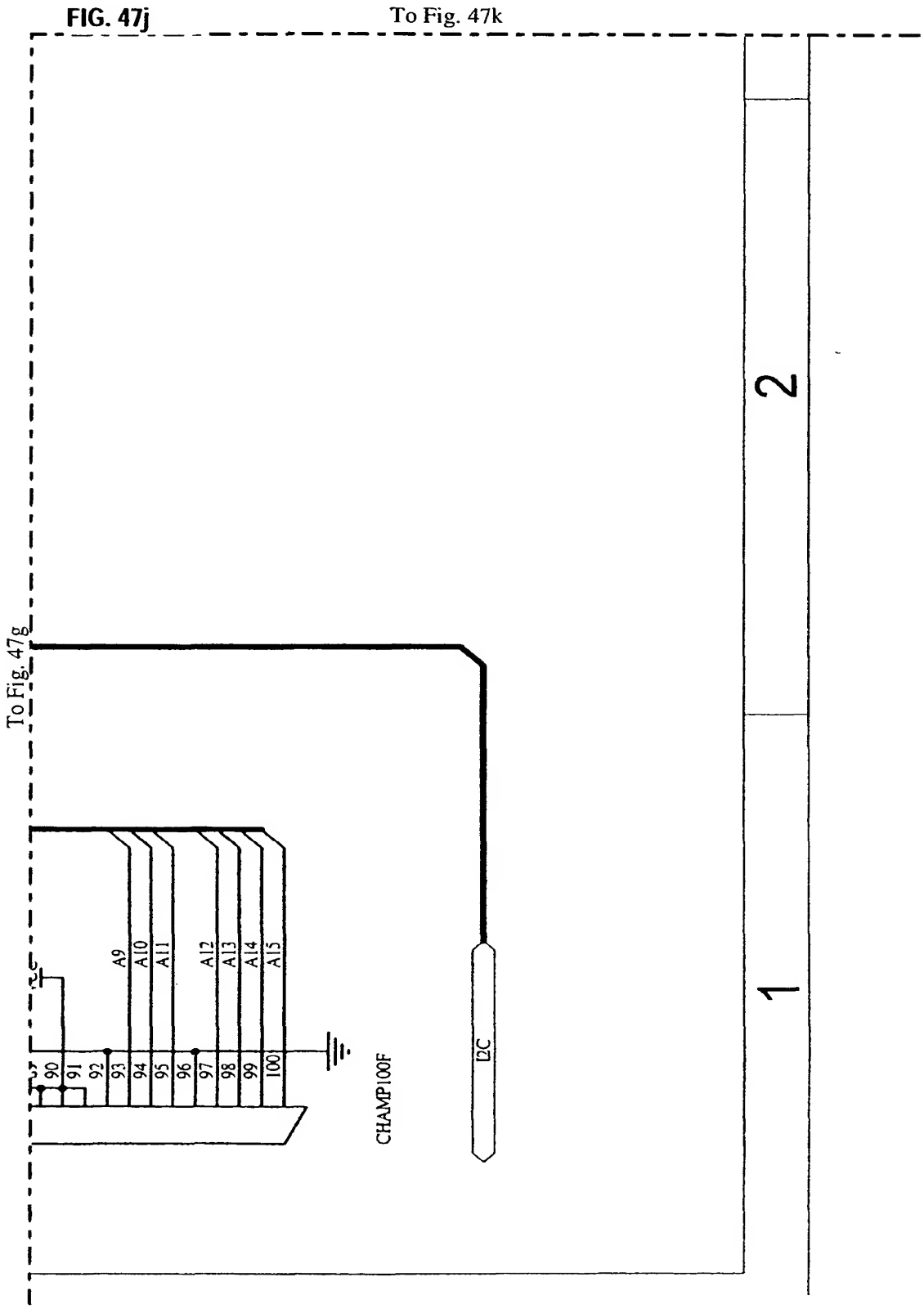

To Fig. 47k
To Fig. 47g
2
1
A9
A10
A11
A12
A13
A14
A15
90
91
92
93
94
95
96
97
98
99
100
CHAMP100F
I2C

FIG. 47k

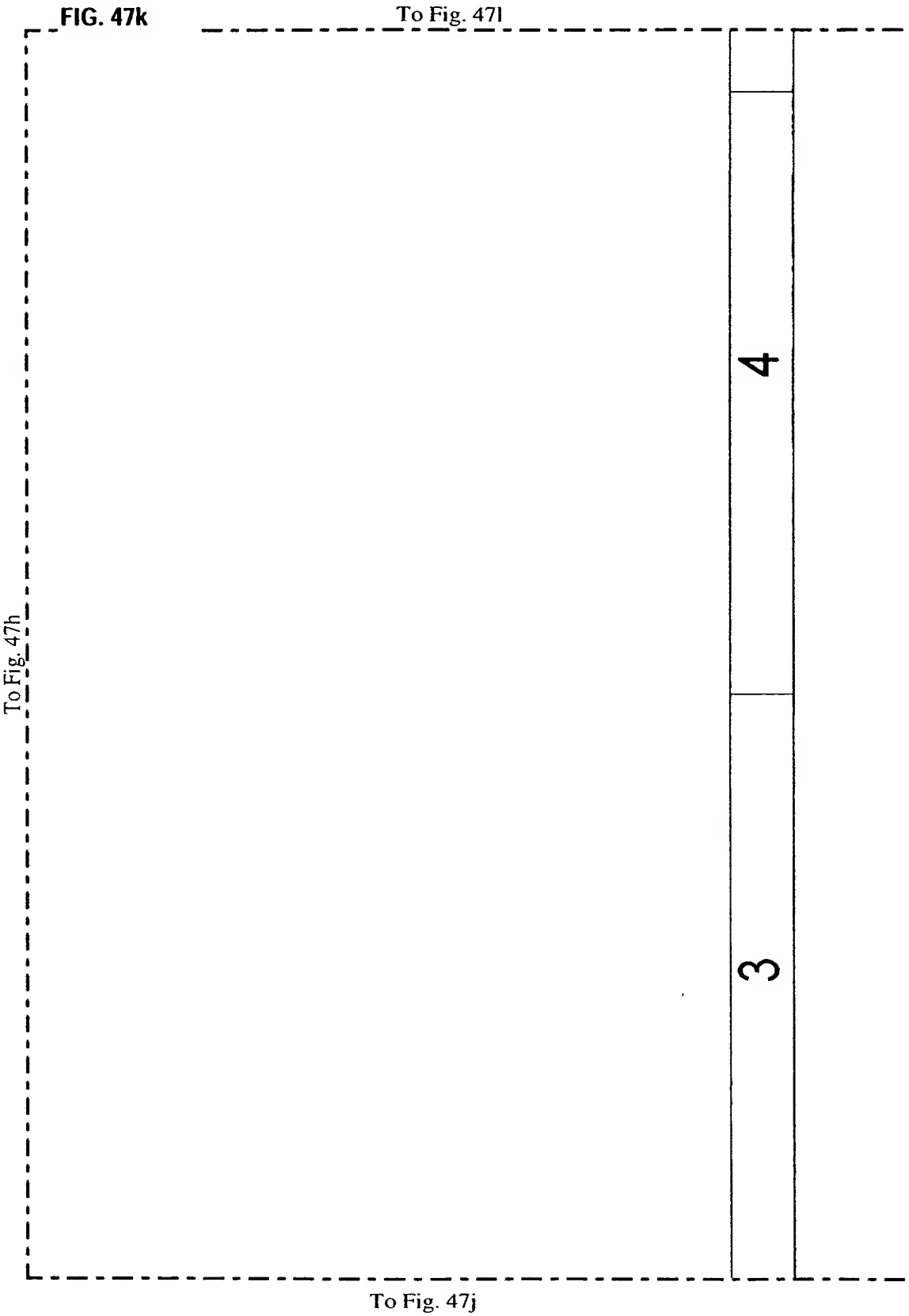


FIG. 47l

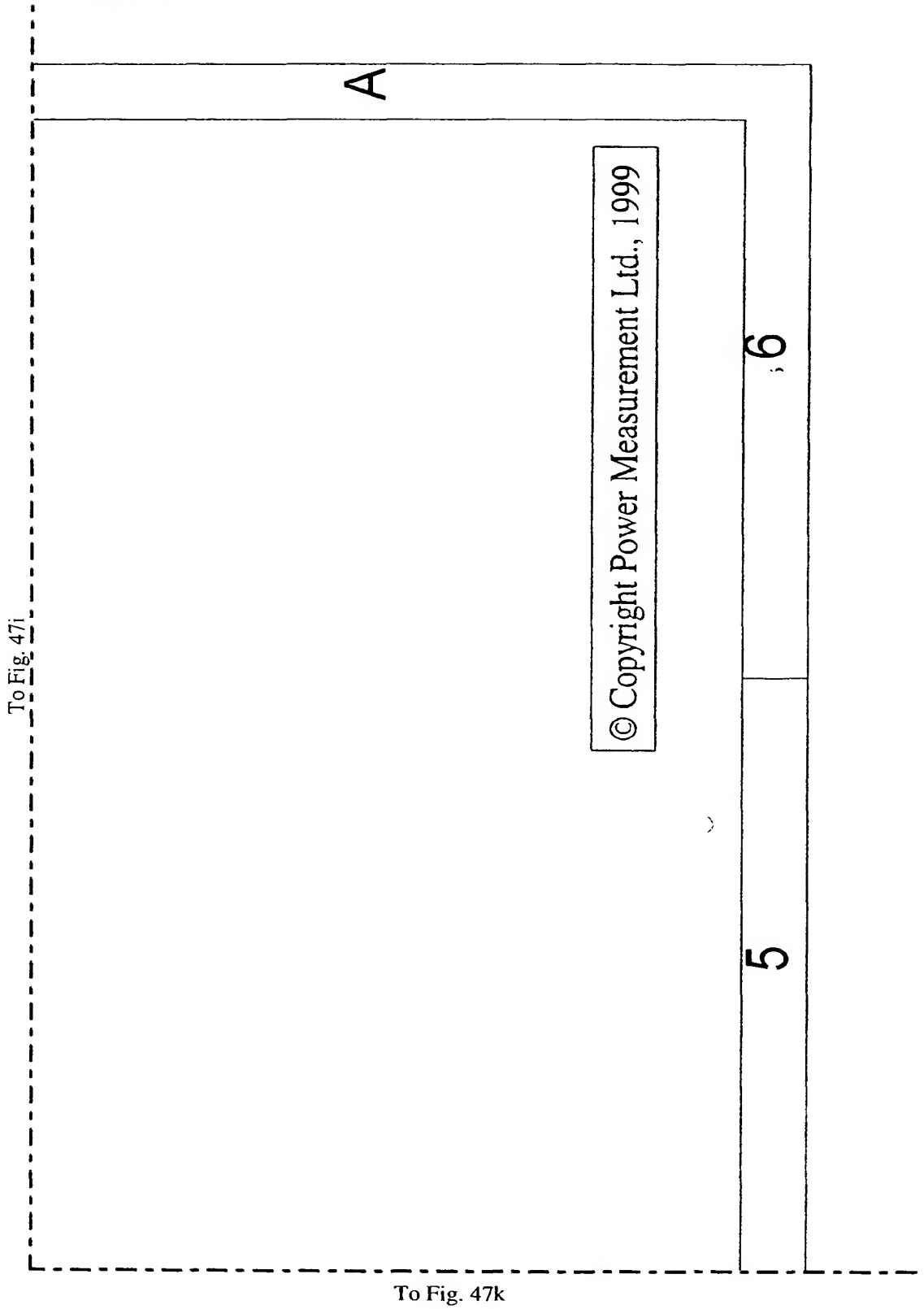

A
6
5
© Copyright Power Measurement Ltd., 1999
To Fig. 47i
To Fig. 47k

FIG. 48a

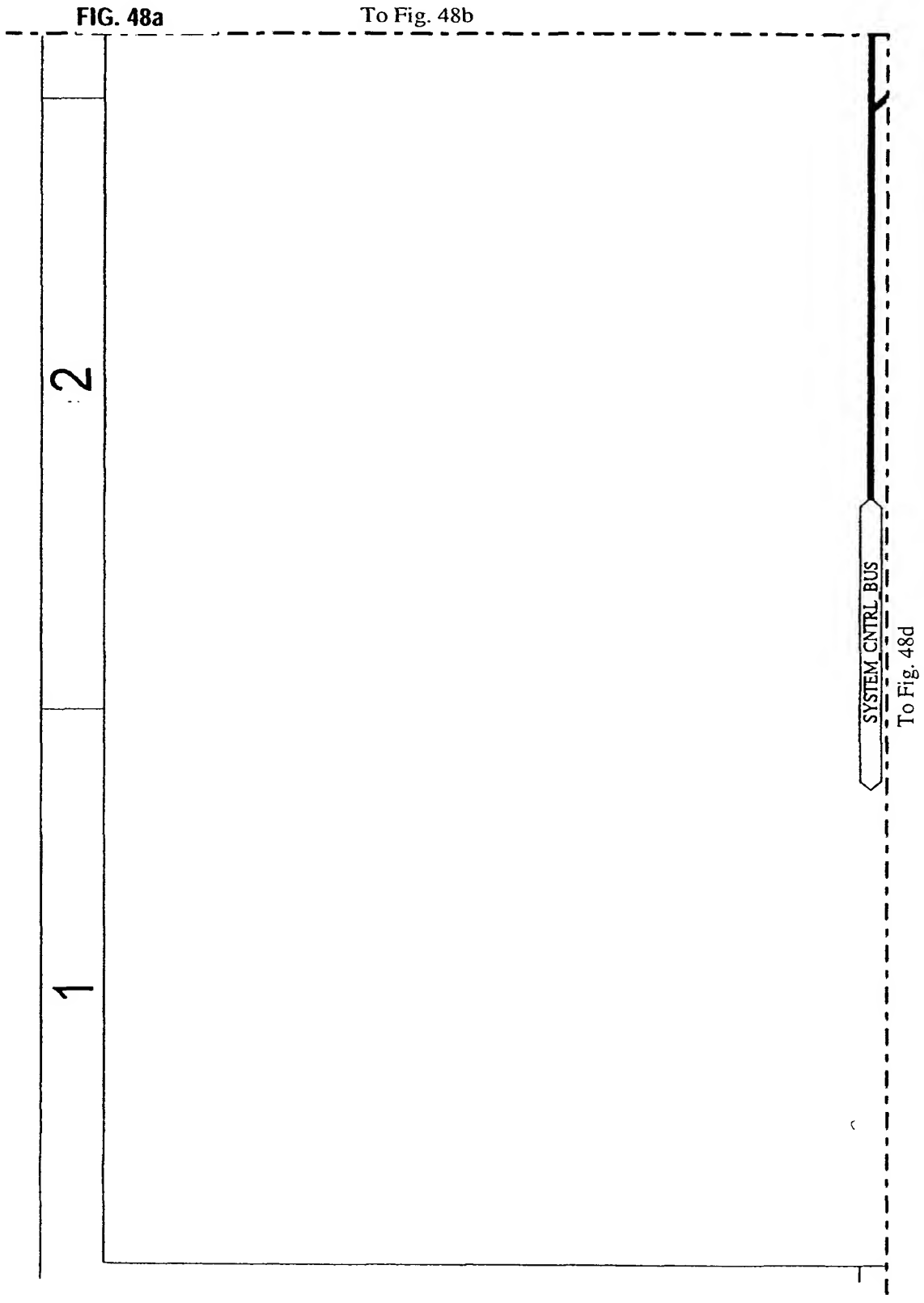


FIG. 48b

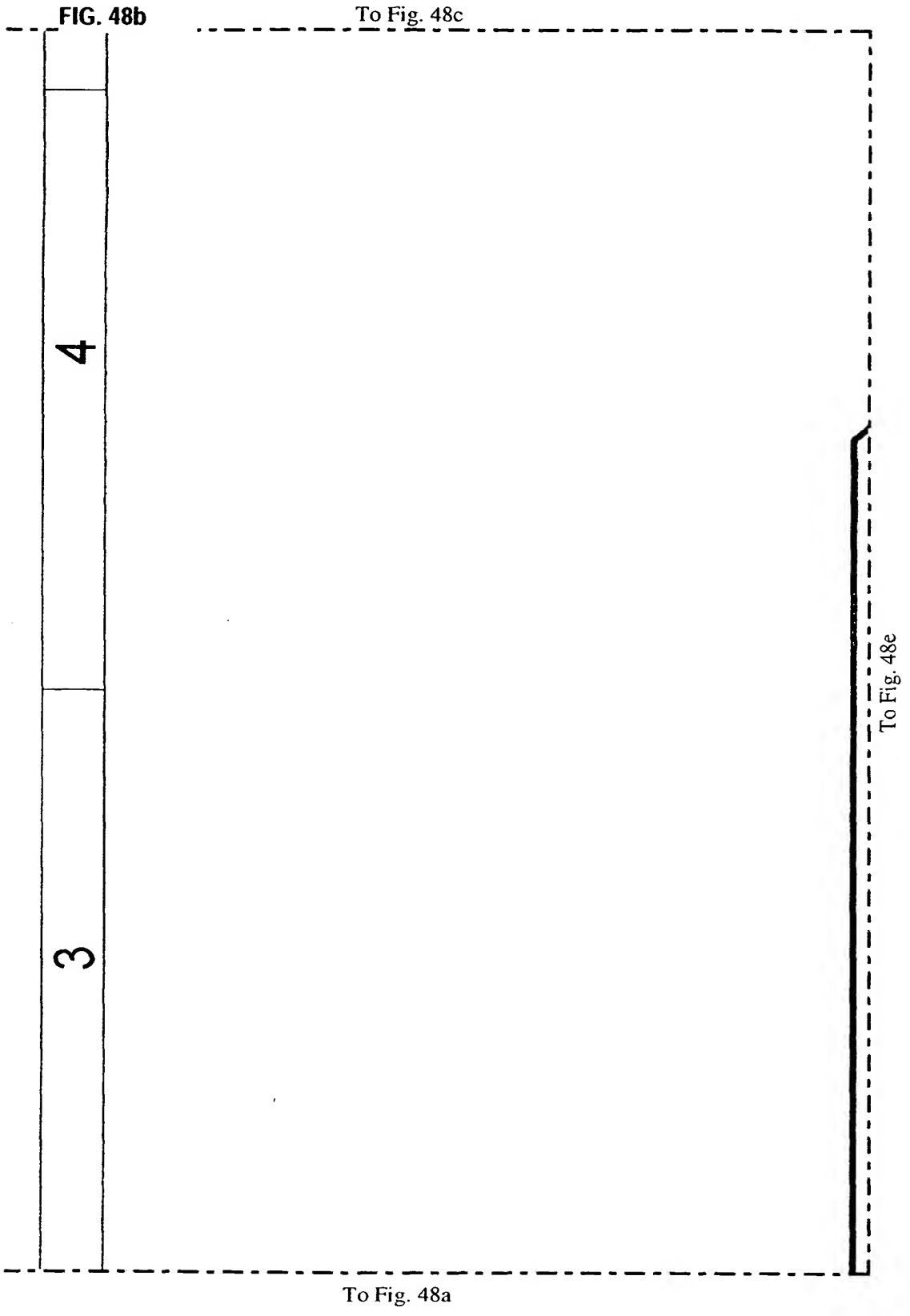


FIG. 48c

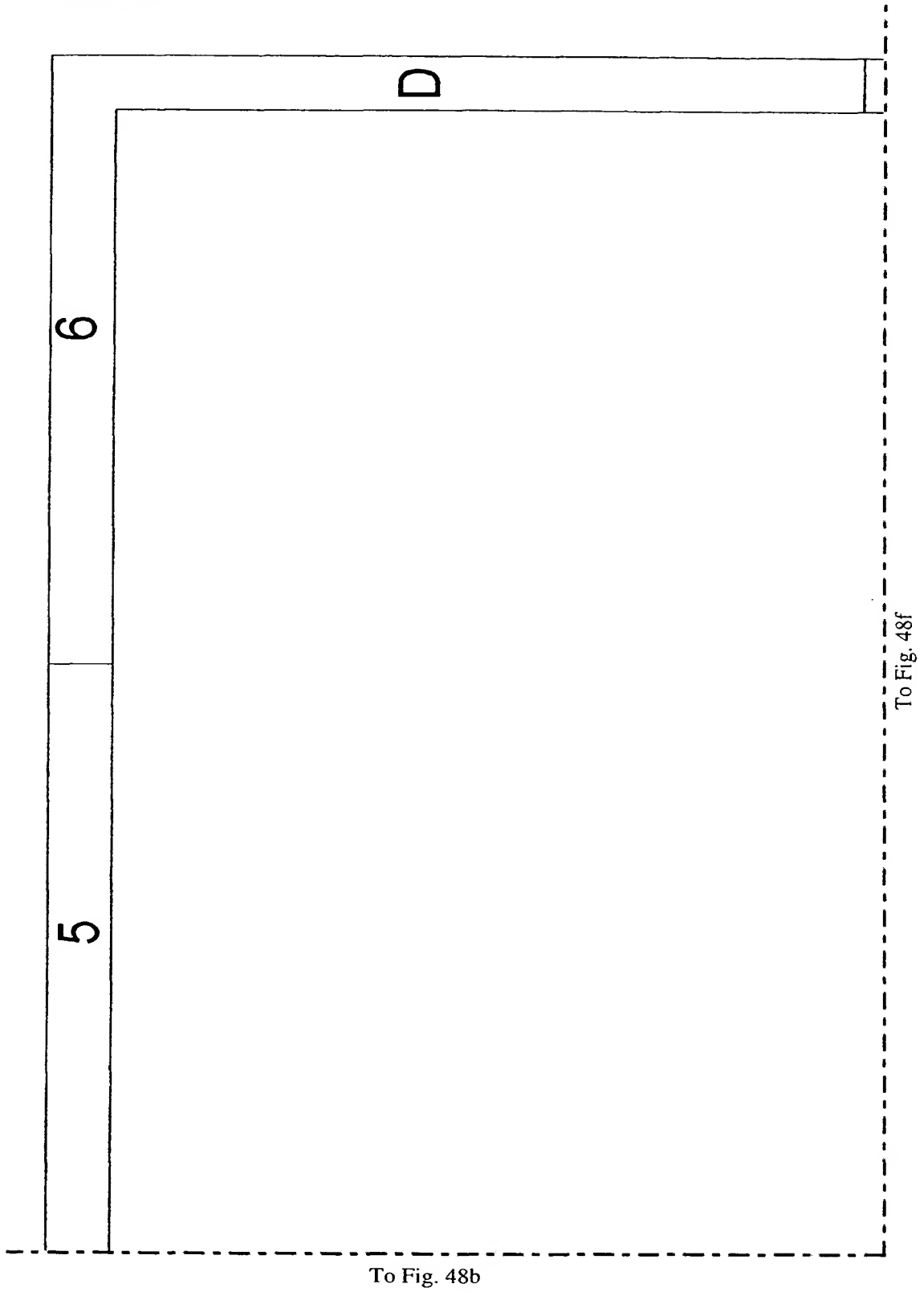


FIG. 48d

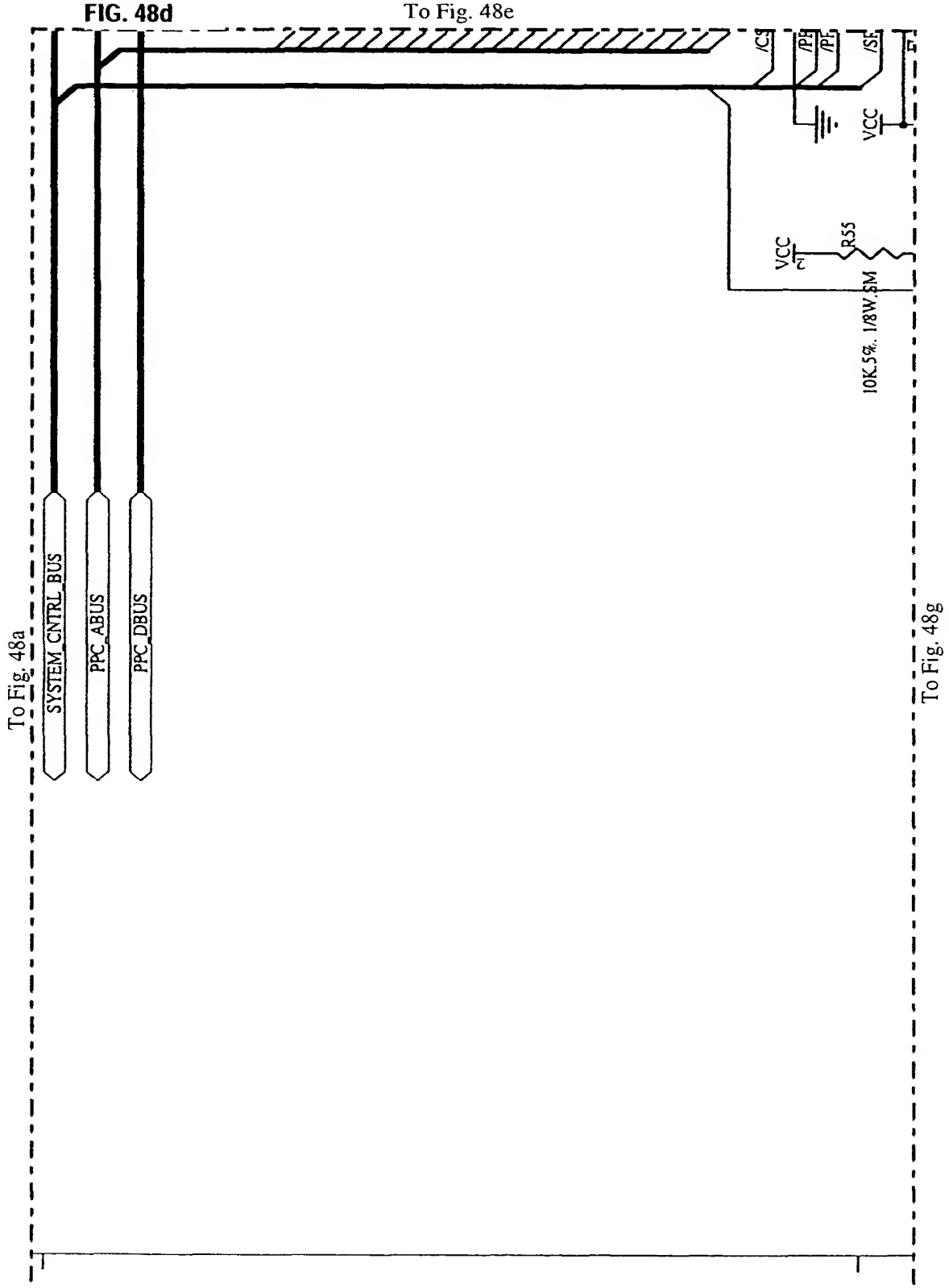

To Fig. 48e
/CS
/PE
/PE
/SE
VCC
VCC
R55
10K,5%, 1/8W, SM
SYSTEM_CNTRL_BUS
PPC_ABUS
PPC_DBUS
To Fig. 48a
To Fig. 48g

FIG. 48e

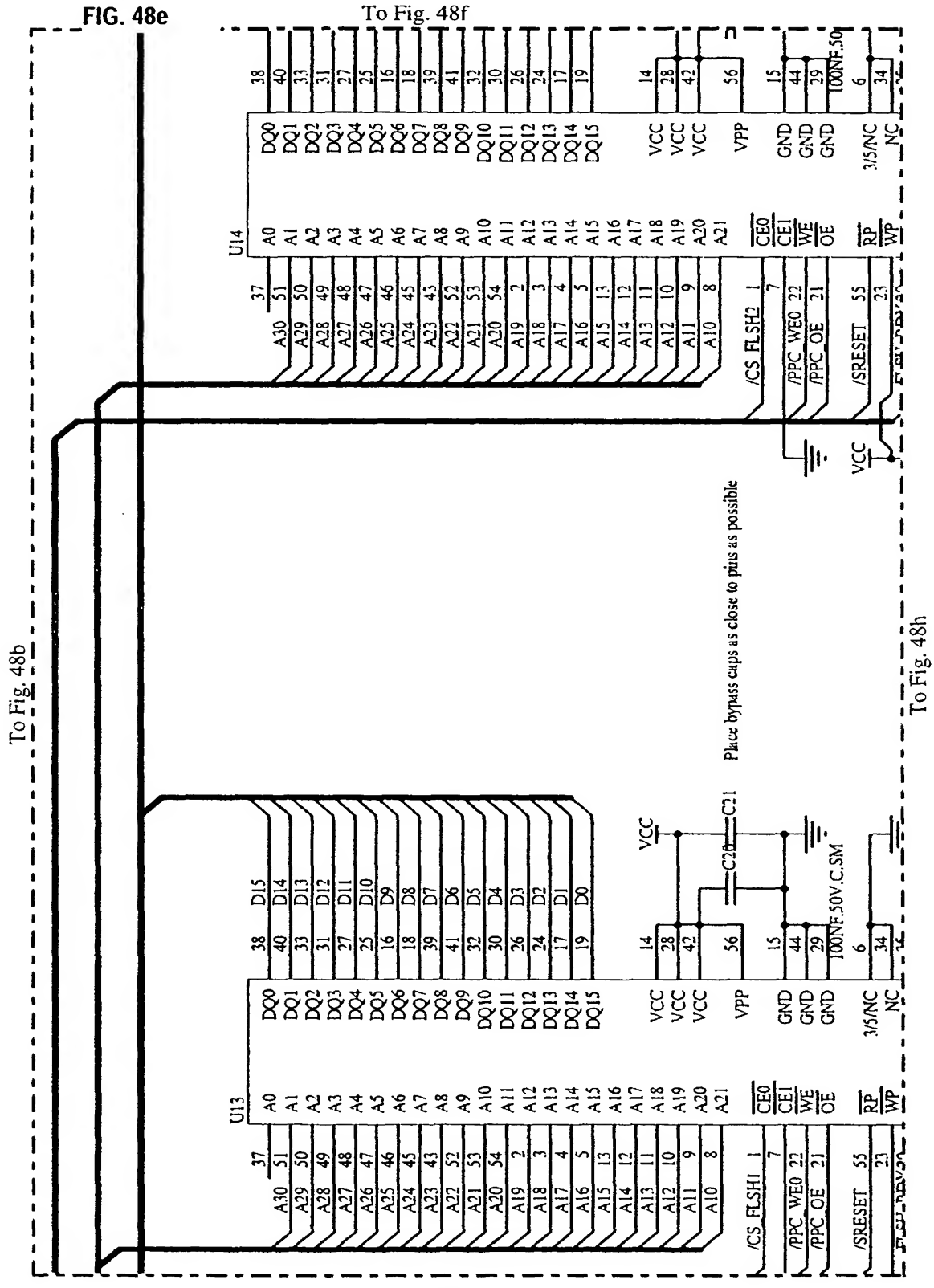
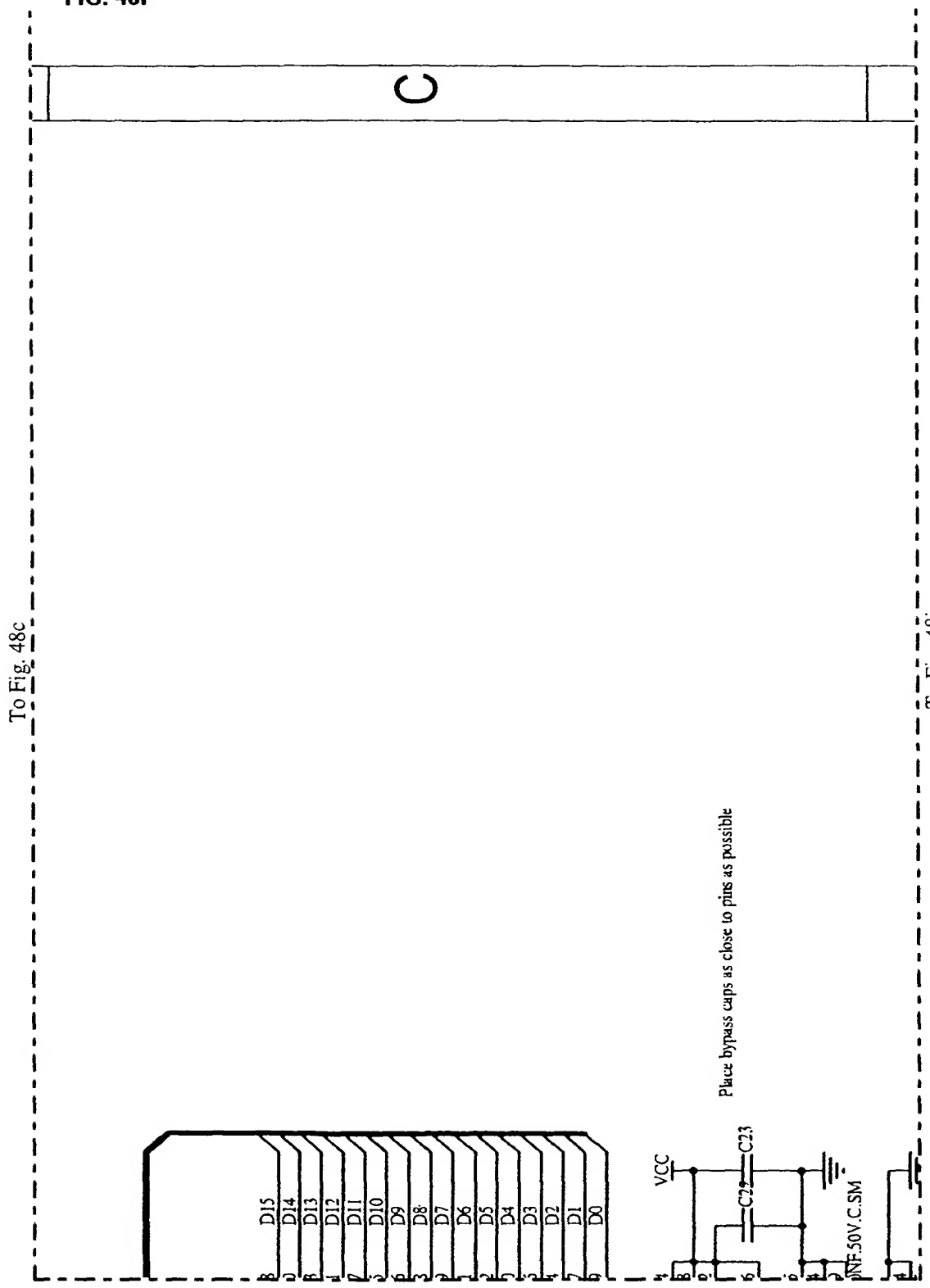

To Fig. 48f
To Fig. 48b
To Fig. 48h
To Fig. 48d
U14
U13
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
VCC VCC VCC VPP GND GND GND 3/5/NC NC
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21
A30 A29 A28 A27 A26 A25 A24 A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10
CE0 CE1 WE OE RP WP
/CS_FLSH2 /CS_FLSH1 /PPC_WE0 /PPC_OE /SRESET
Place bypass caps as close to pins as possible
C21
100NF.50V.C.SM

FIG. 48f



To Fig. 48e

FIG. 48g

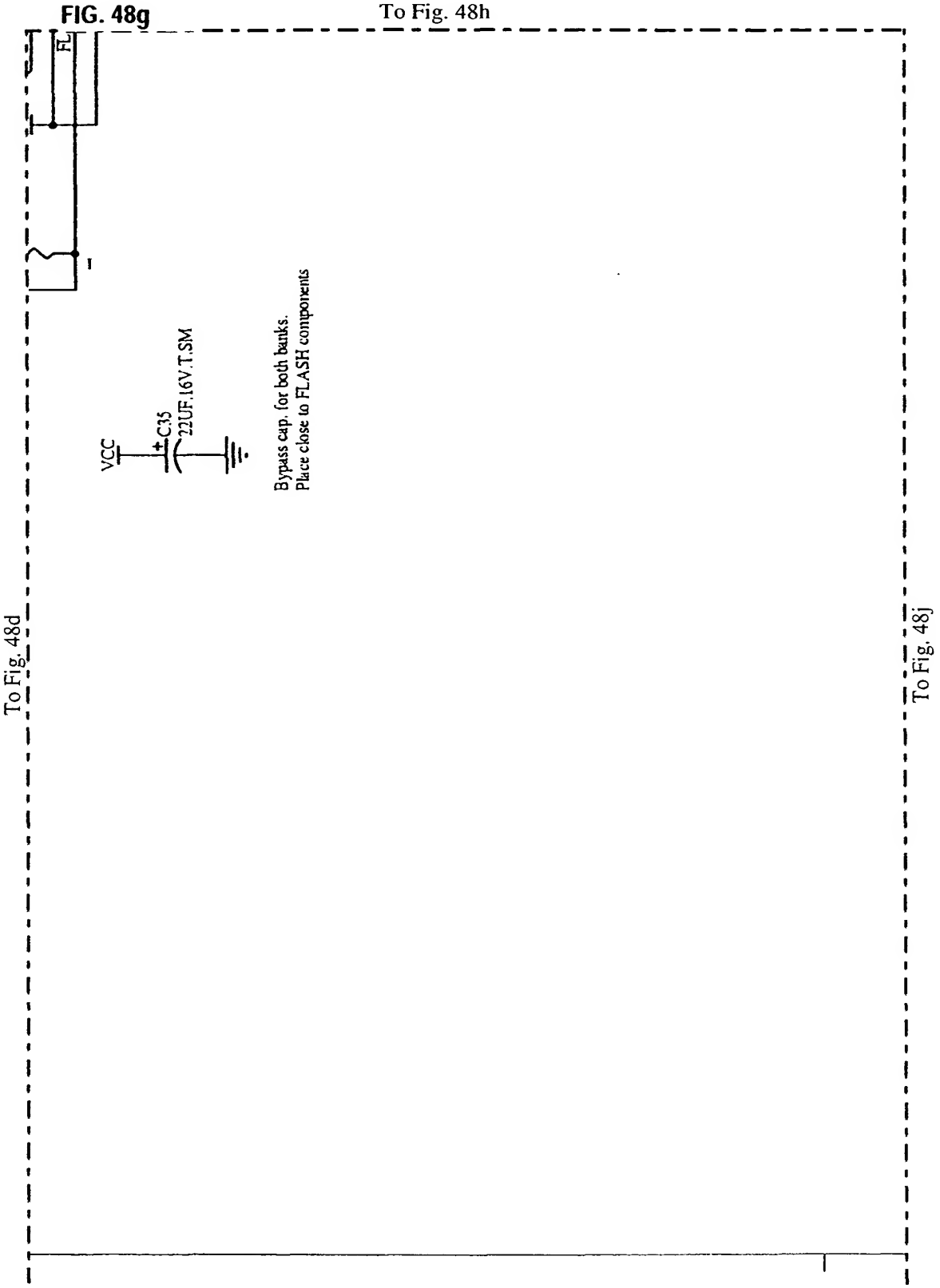

To Fig. 48h
FL
1
VCC
C35
22UF.16V.T.SM
Bypass cap. for both banks.
Place close to FLASH components
To Fig. 48d
To Fig. 48j

FIG. 48h

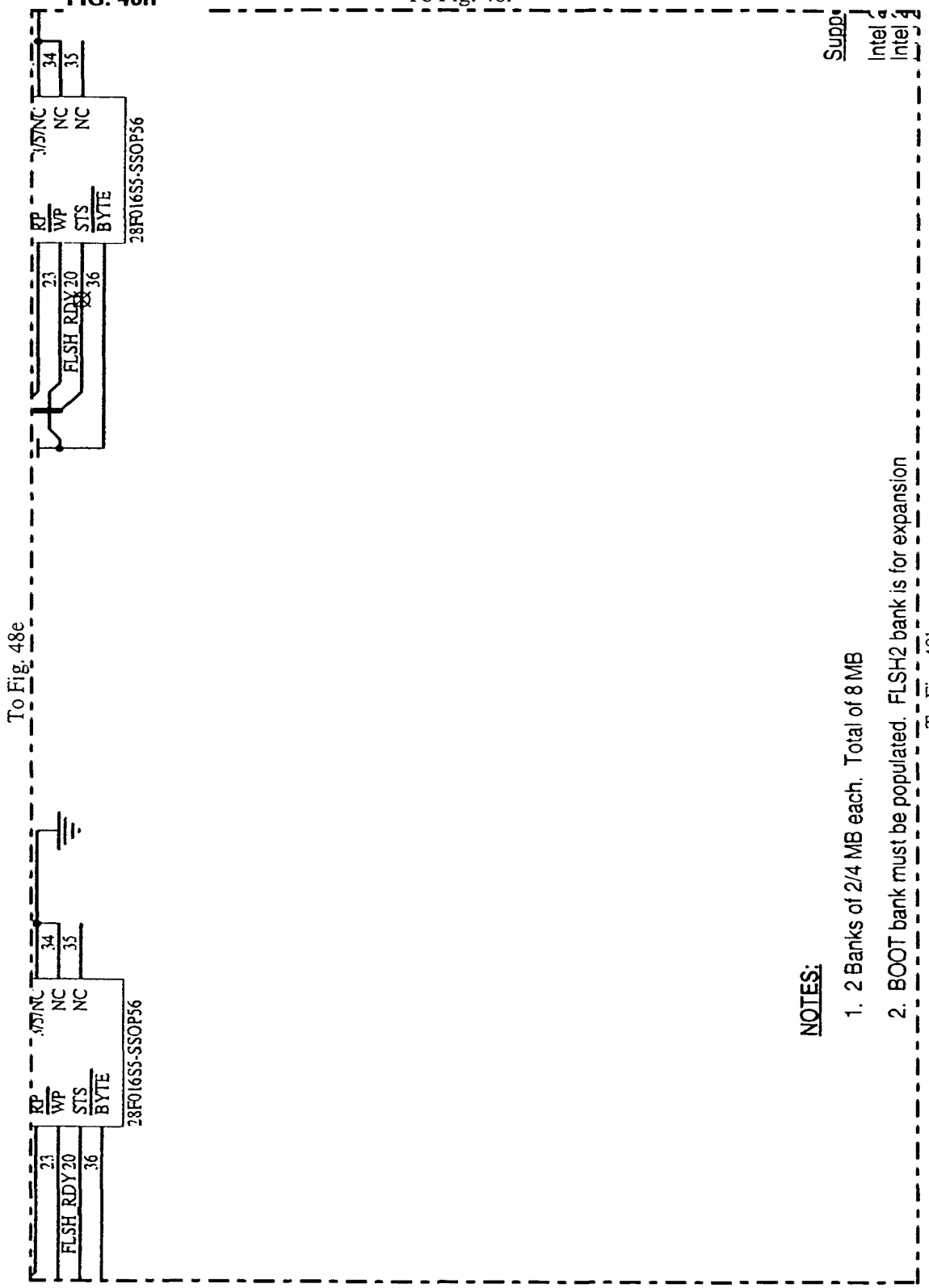
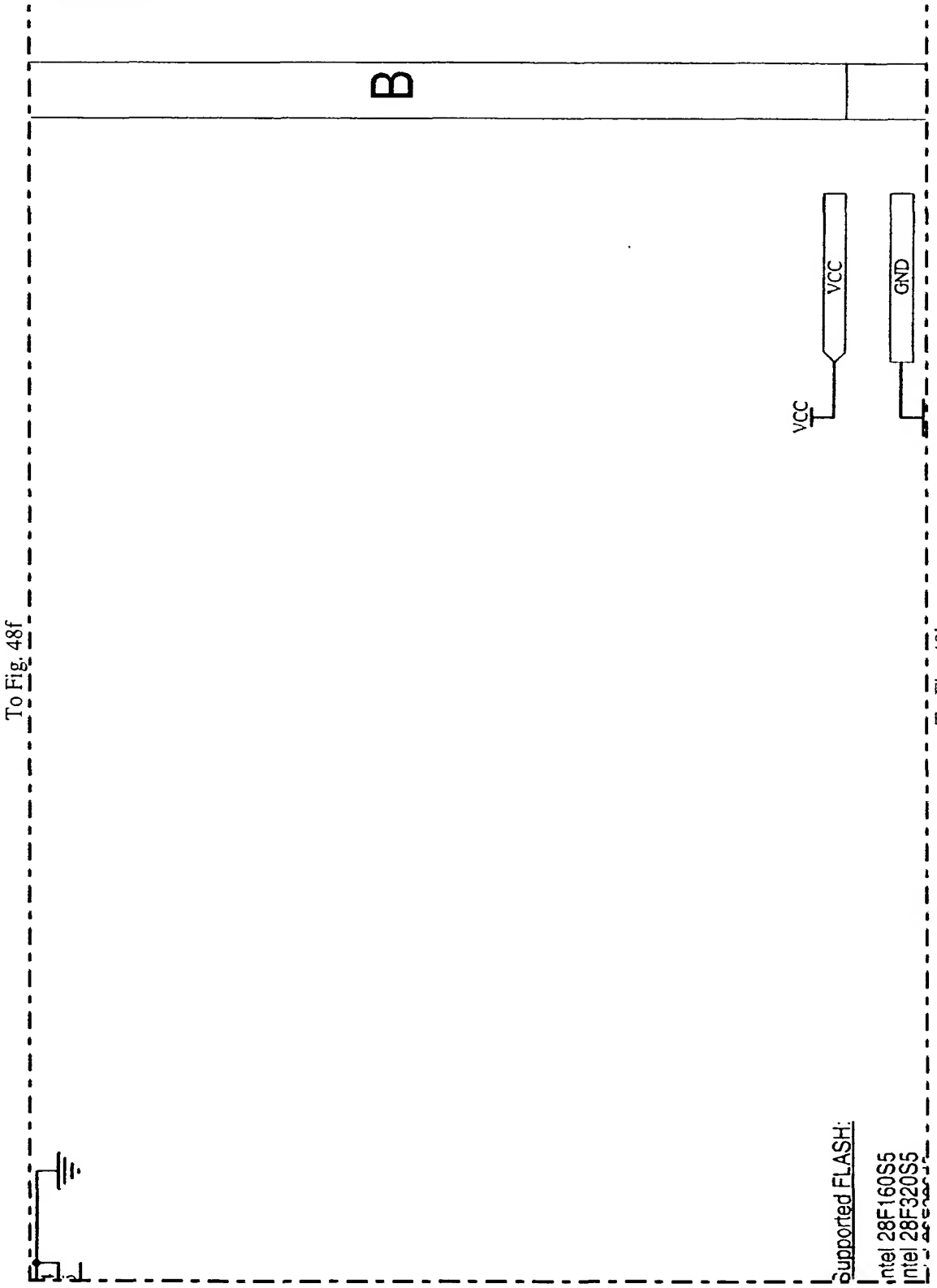

To Fig. 48i
To Fig. 48e
To Fig. 48k
To Fig. 48g
28F016S5-SSOP56
28F016S5-SSOP56
RP
WP
STS
BYTE
FLSH_RDY
NC
34
35
23
20
36
NOTES:
1. 2 Banks of 2/4 MB each. Total of 8 MB
2. BOOT bank must be populated. FLSH2 bank is for expansion

FIG. 48i



To Fig. 48h

FIG. 48j

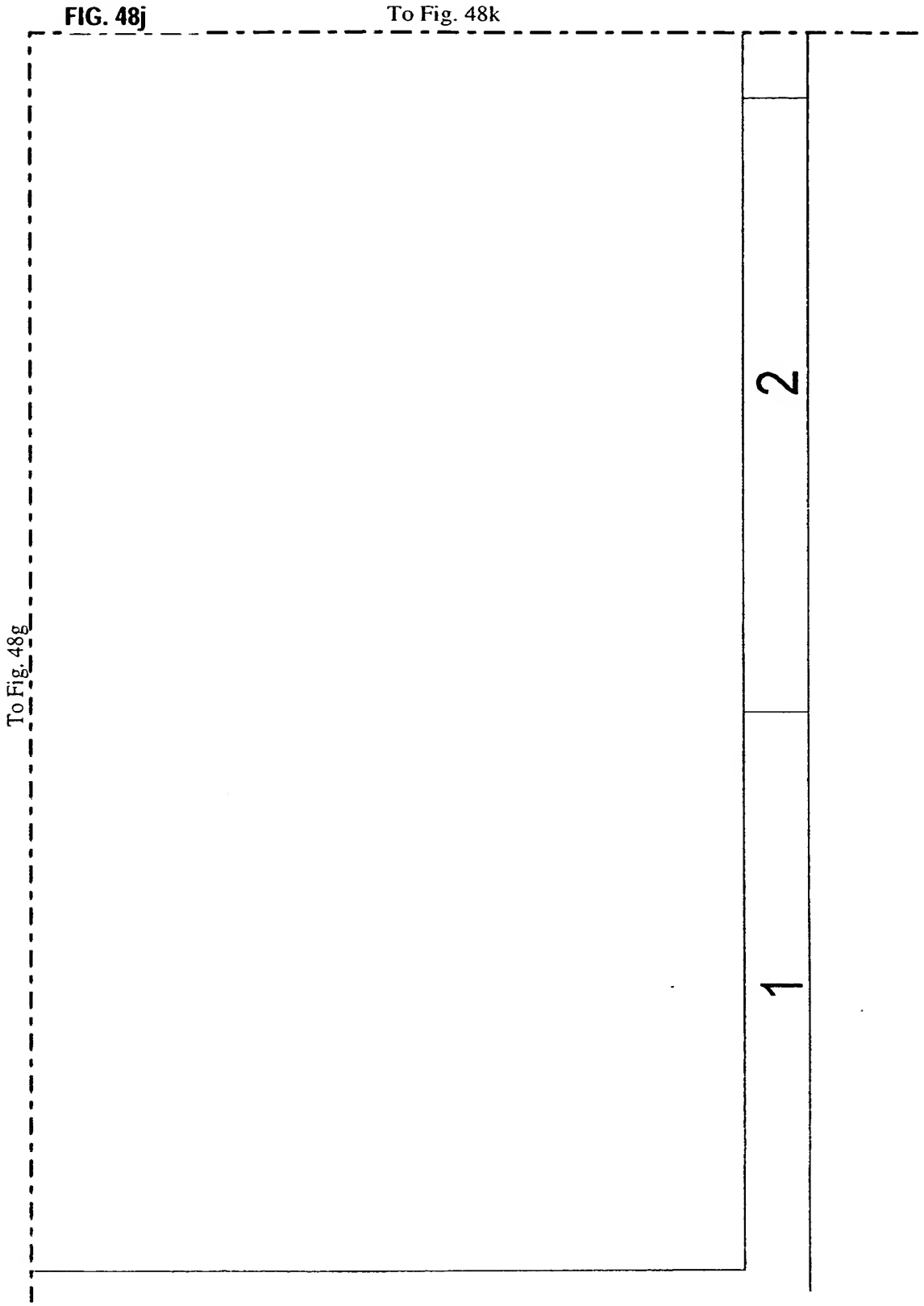
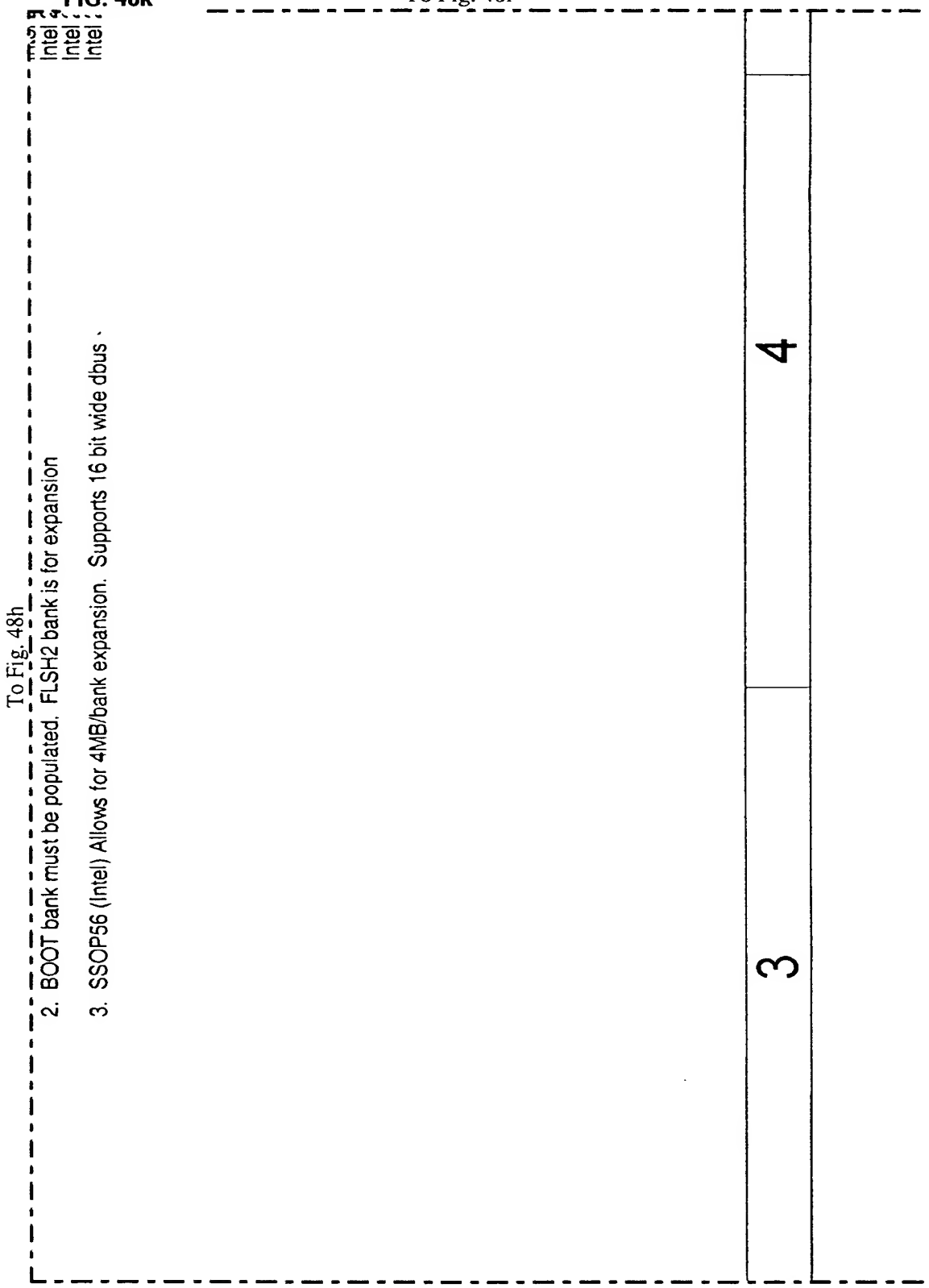


FIG. 48k

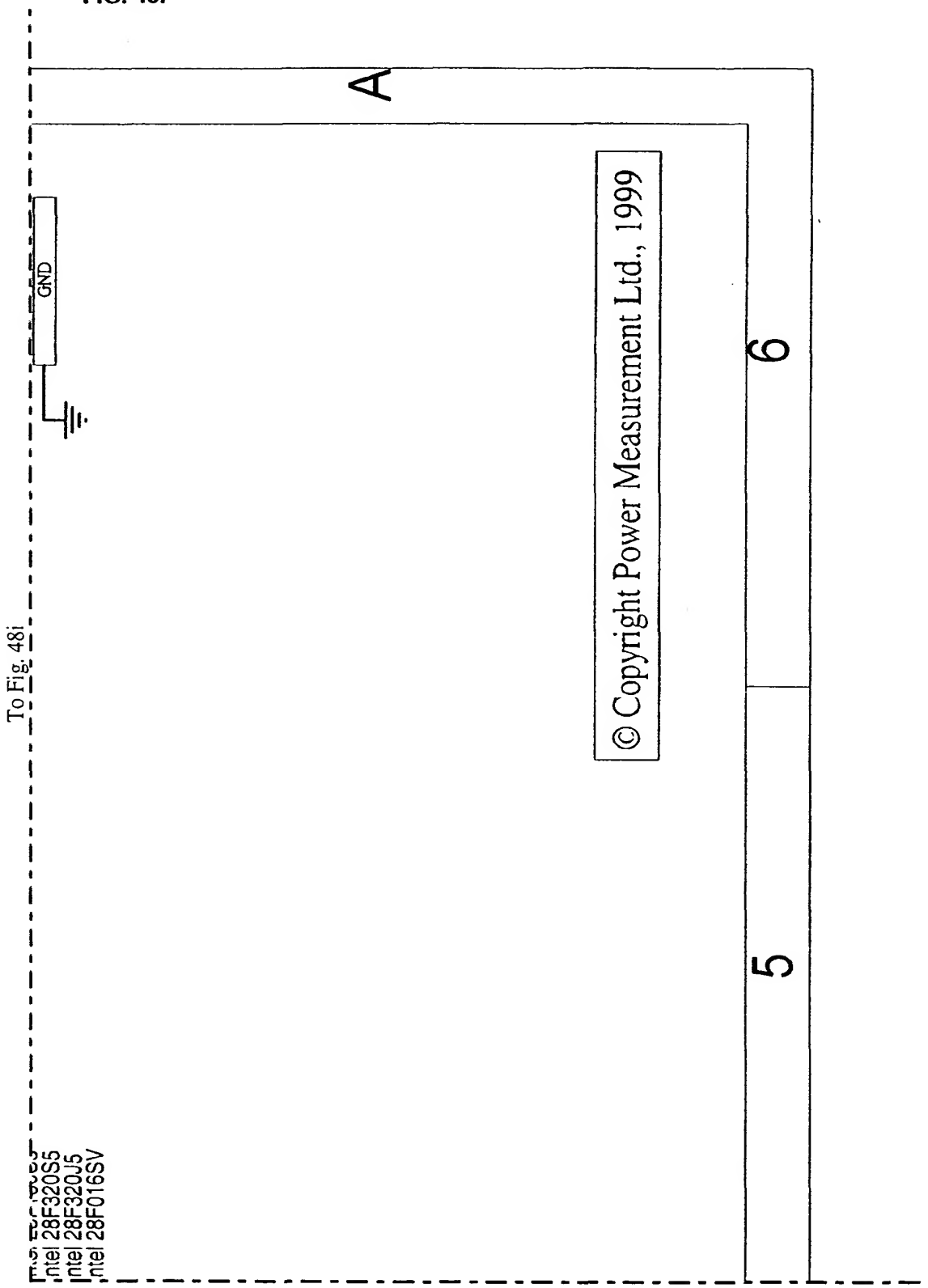
To Fig. 48l



To Fig. 48h

To Fig. 48j

FIG. 48l



To Fig. 48k

FIG. 49a

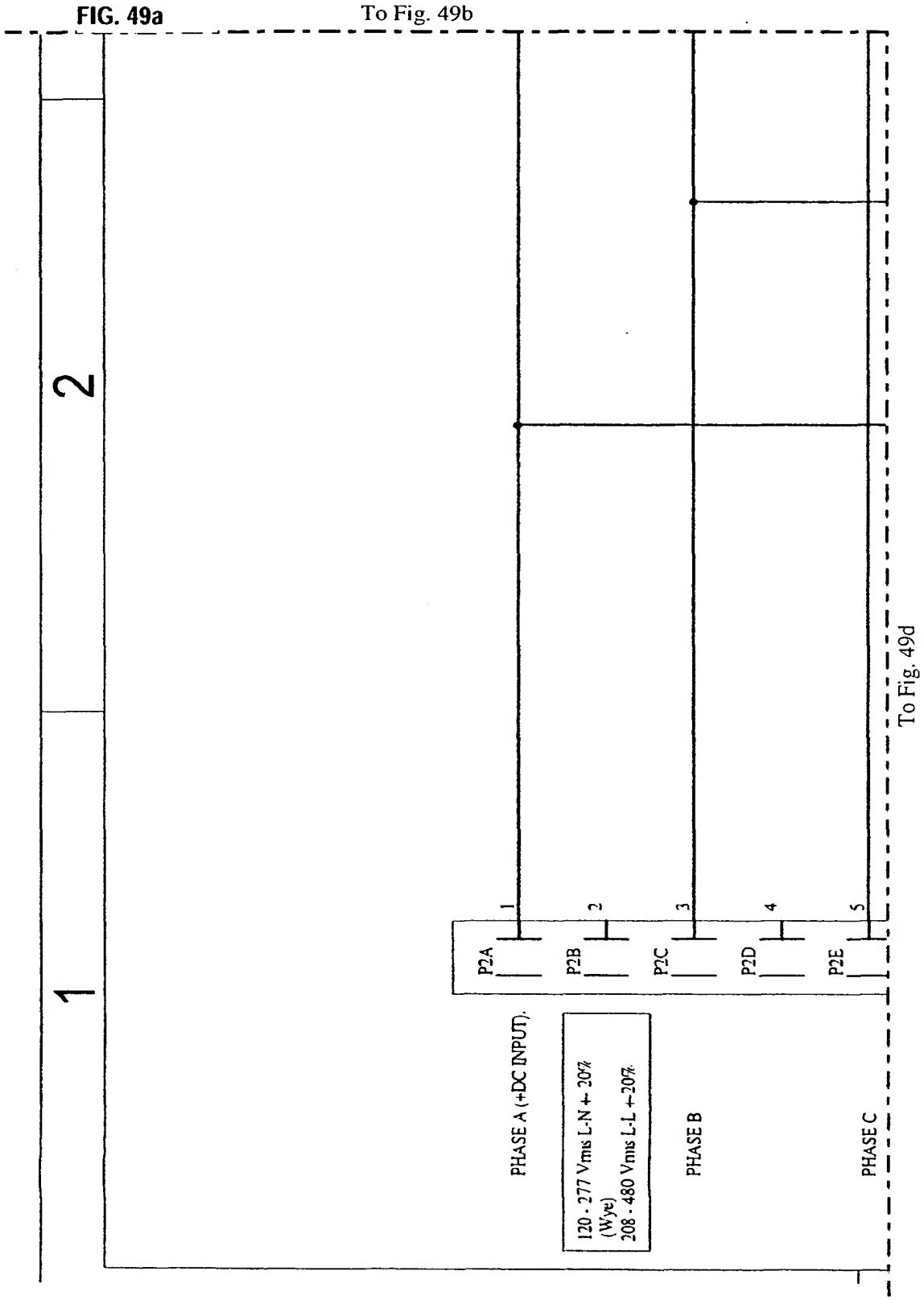

To Fig. 49b
2
1
1
2
3
4
5
P2A
P2B
P2C
P2D
P2E
PHASE A (+DC INPUT).
120 - 277 Vrms L-N +- 20%
(Wye)
208 - 480 Vrms L-L +-20%
PHASE B
PHASE C
To Fig. 49d

FIG. 49b

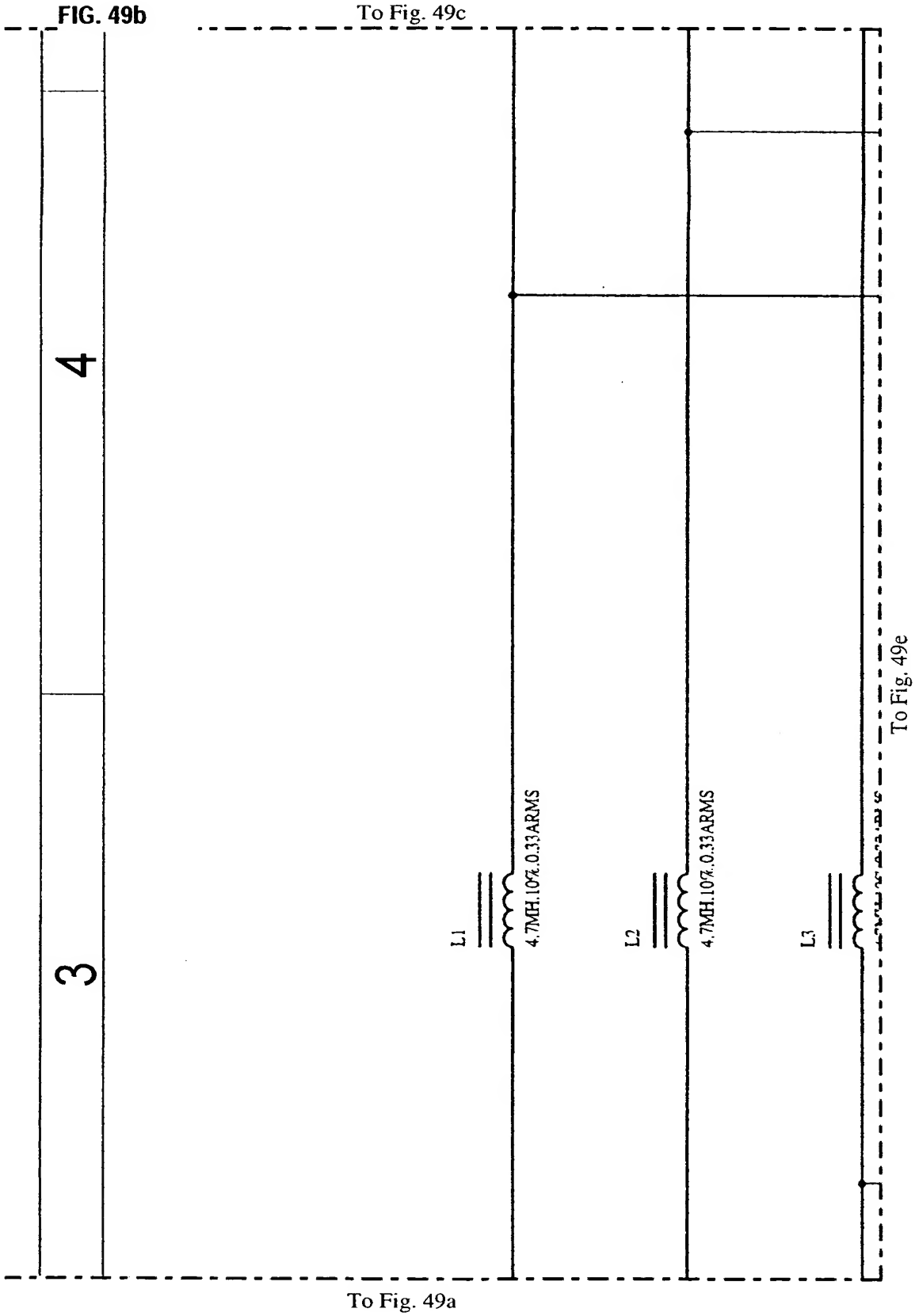

To Fig. 49c
4
3
L1
4.7MH.10%.0.33ARMS
L2
4.7MH.10%.0.33ARMS
L3
To Fig. 49e
To Fig. 49a

FIG. 49c

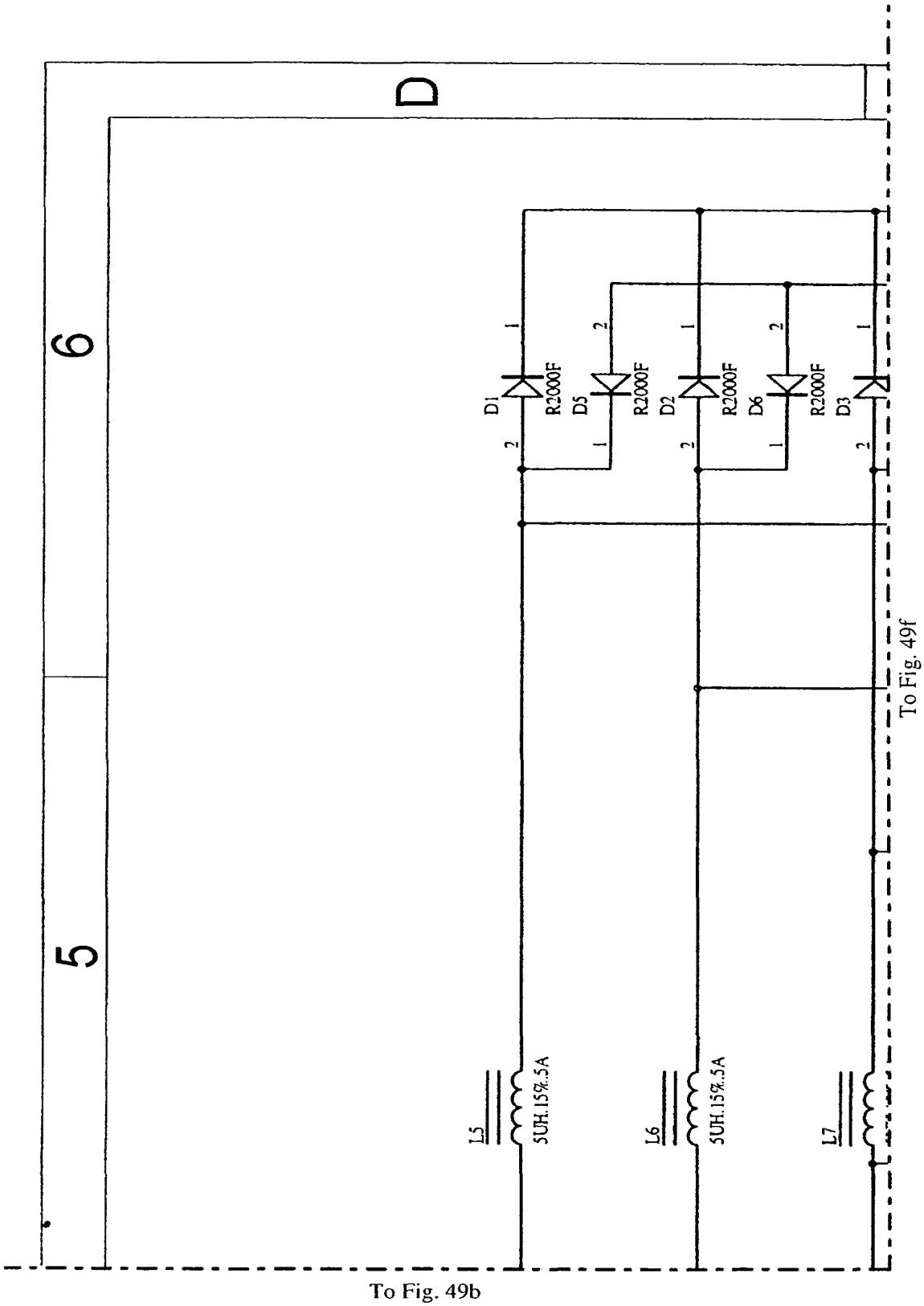

D
6
5
D1
R2000F
D5
R2000F
D2
R2000F
D6
R2000F
D3
L5
5UH.15%.5A
L6
5UH.15%.5A
L7
To Fig. 49f
To Fig. 49b

FIG. 49d

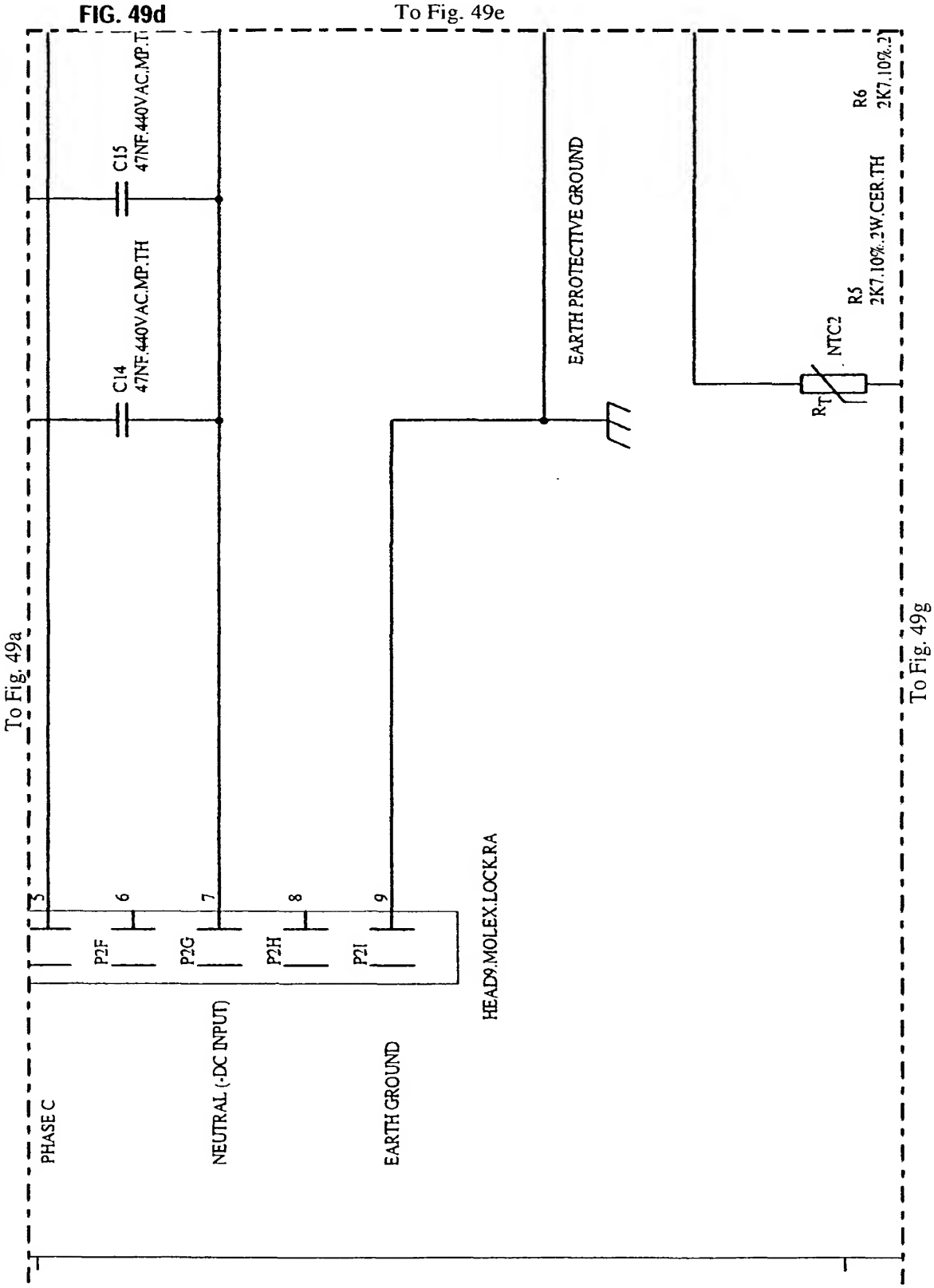

To Fig. 49e
To Fig. 49a
To Fig. 49g
C15
47NF.440VAC.MP.TH
C14
47NF.440VAC.MP.TH
EARTH PROTECTIVE GROUND
R6
2K7.10%.2W.CER.TH
R5
2K7.10%.2W.CER.TH
NTC2
R_T
5
6
7
8
9
P2F
P2G
P2H
P2I
HEAD9.MOLEX.LOCK.RA
PHASE C
NEUTRAL (-DC INPUT)
EARTH GROUND

FIG. 49e

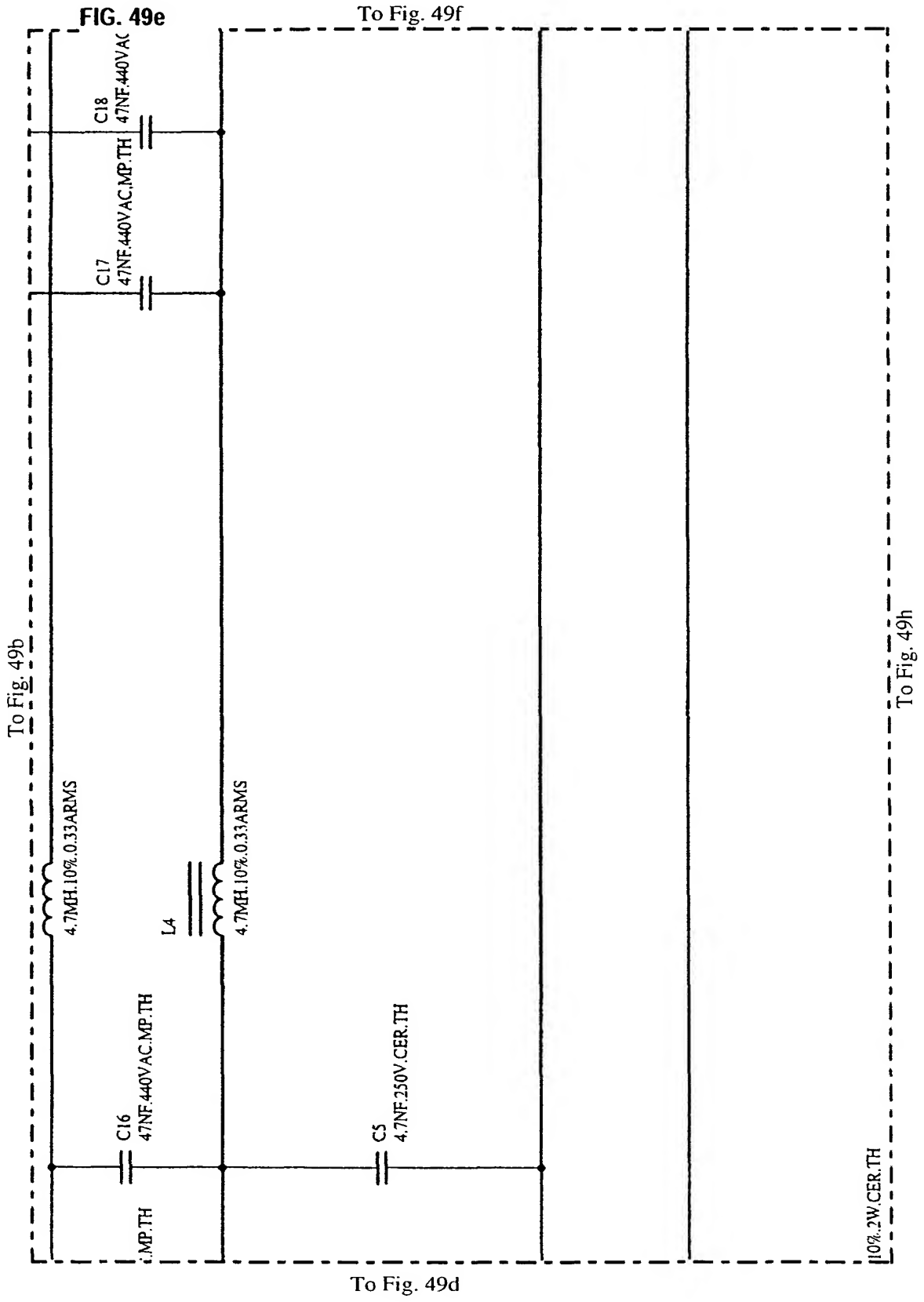

To Fig. 49f
C18
47NF.440VAC
C17
47NF.440VAC.MP.TH
To Fig. 49b
4.7MH.10%.0.33ARMS
L4
4.7MH.10%.0.33ARMS
C16
47NF.440VAC.MP.TH
C5
4.7NF.250V.CER.TH
.MP.TH
10%..2W.CER.TH
To Fig. 49h
To Fig. 49d

FIG. 49f

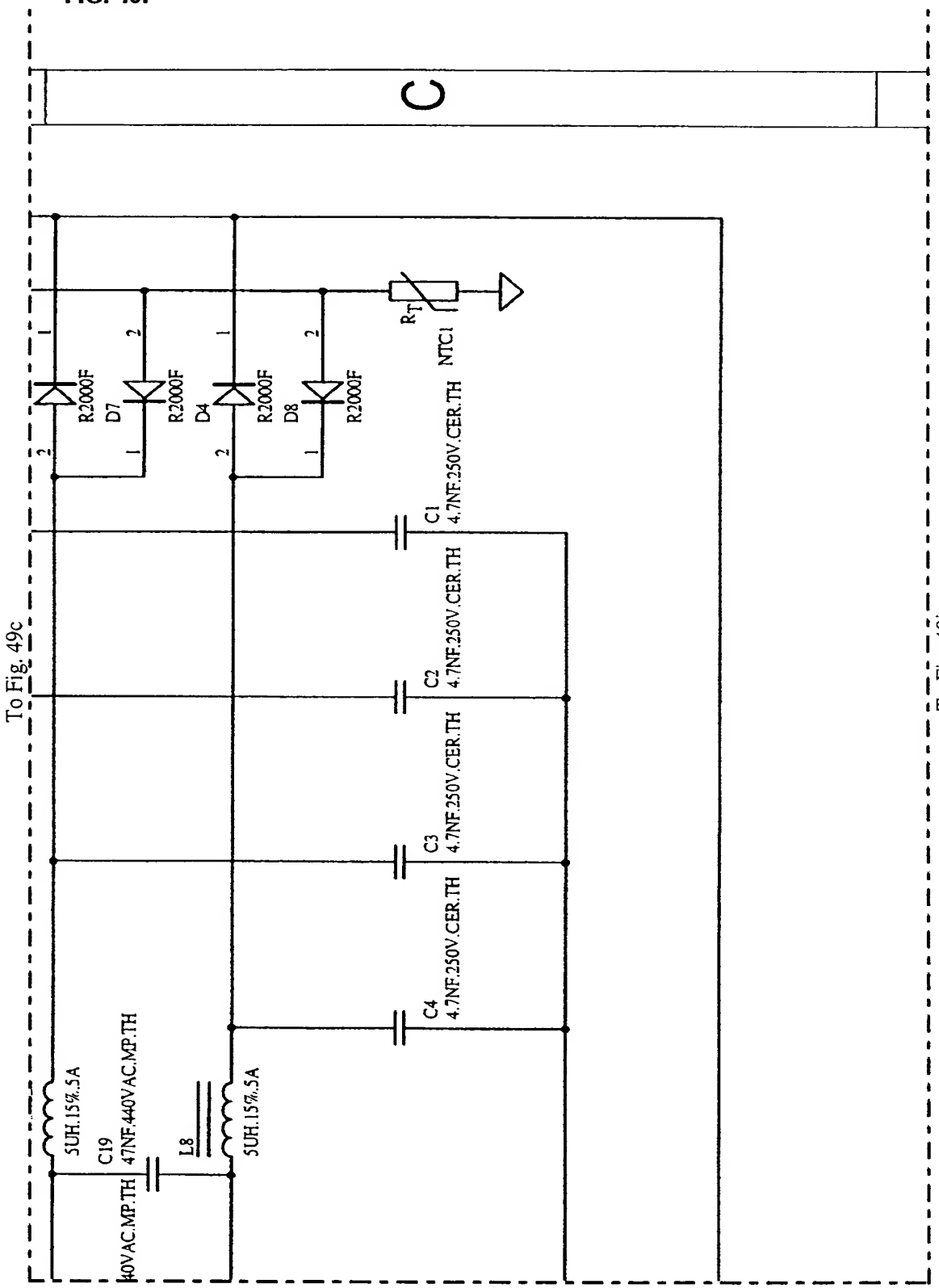

C
To Fig. 49c
To Fig. 49i
To Fig. 49e
R2000F
D7
R2000F
D4
R2000F
D8
R2000F
NTC1
C1
4.7NF.250V.CER.TH
C2
4.7NF.250V.CER.TH
C3
4.7NF.250V.CER.TH
C4
4.7NF.250V.CER.TH
5UH.15%.5A
C19
47NF.440VAC.MP.TH
L8
5UH.15%.5A

FIG. 49g

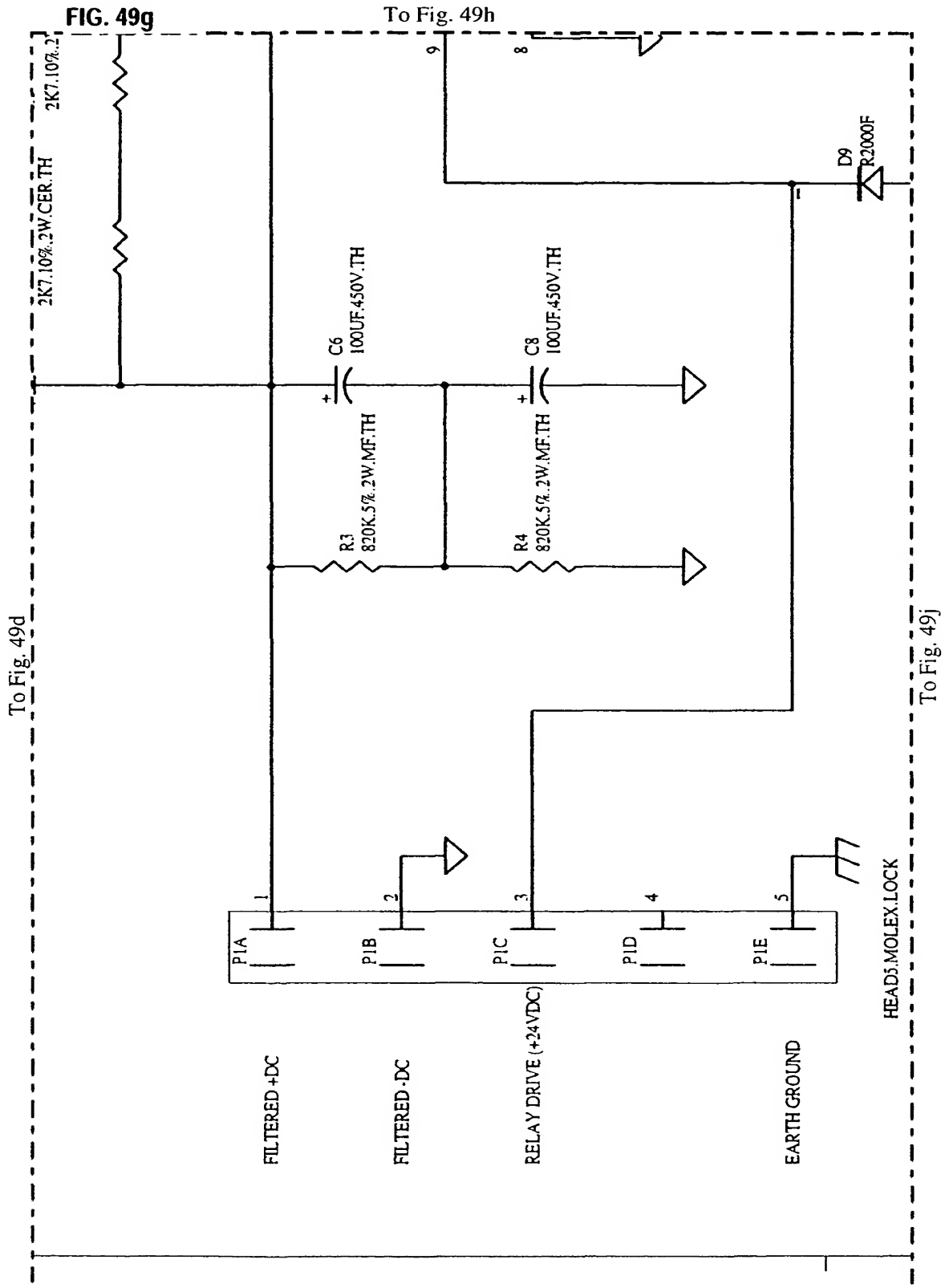
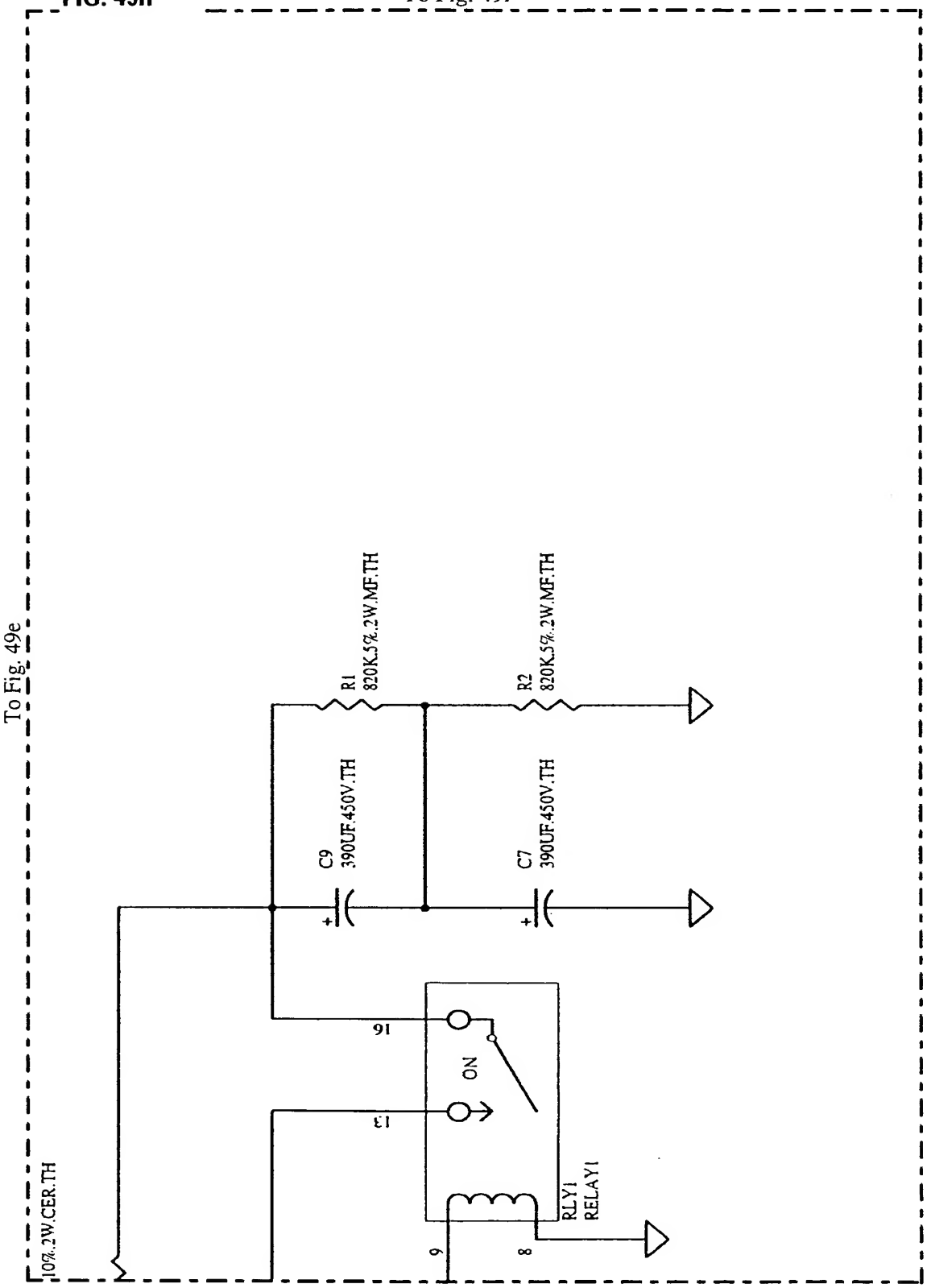

To Fig. 49h
To Fig. 49d
To Fig. 49j
2K7.10%.2W.CER.TH
2K7.10%..2
C6
100UF.450V.TH
C8
100UF.450V.TH
R3
820K.5%.2W.MF.TH
R4
820K.5%.2W.MF.TH
D9
R2000F
9
8
1
P1A
P1B
P1C
P1D
P1E
1
2
3
4
5
FILTERED +DC
FILTERED -DC
RELAY DRIVE (+24VDC)
EARTH GROUND
HEAD5.MOLEX.LOCK

FIG. 49h

To Fig. 49i



To Fig. 49g

FIG. 49i

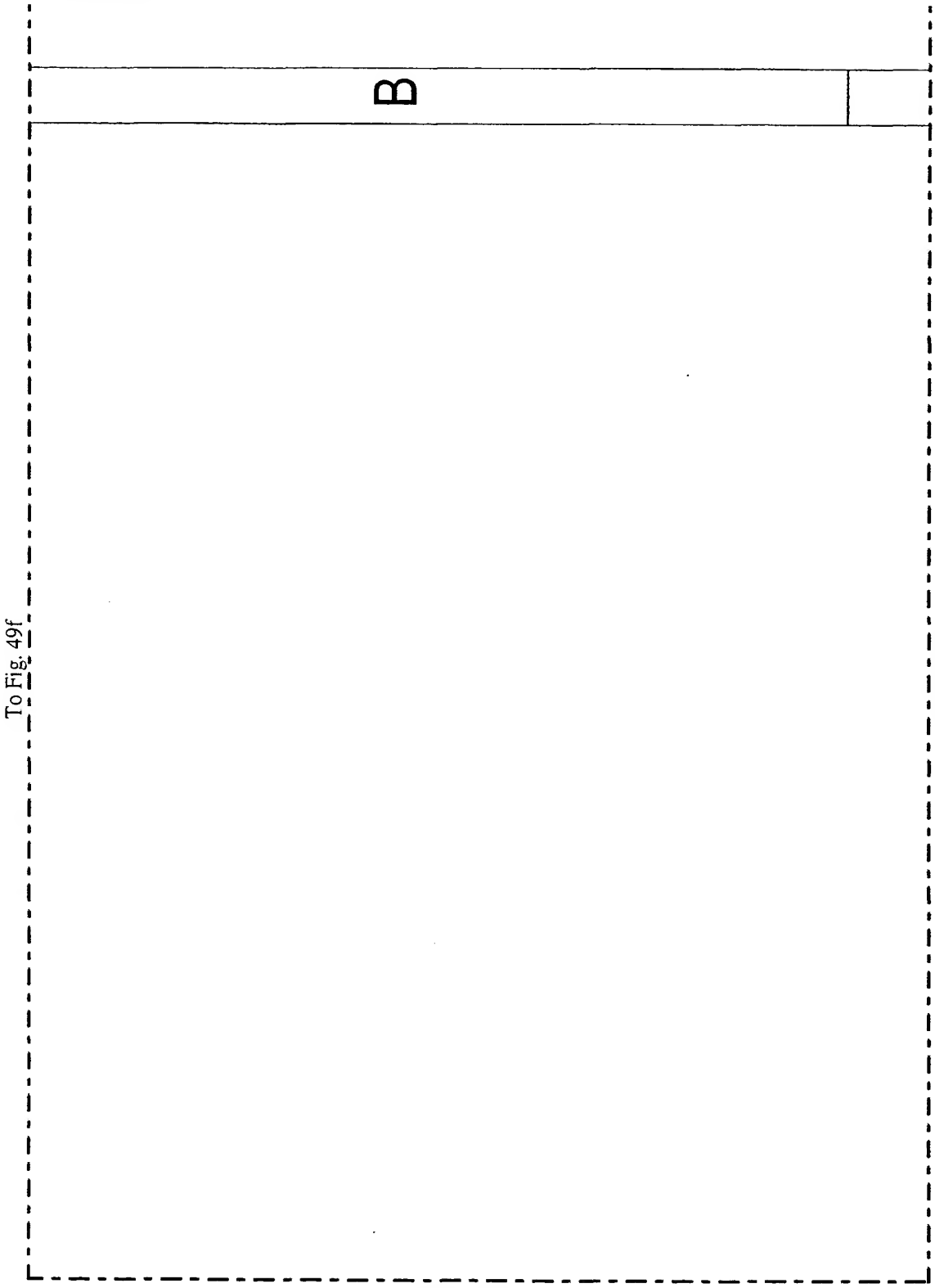


FIG. 49j

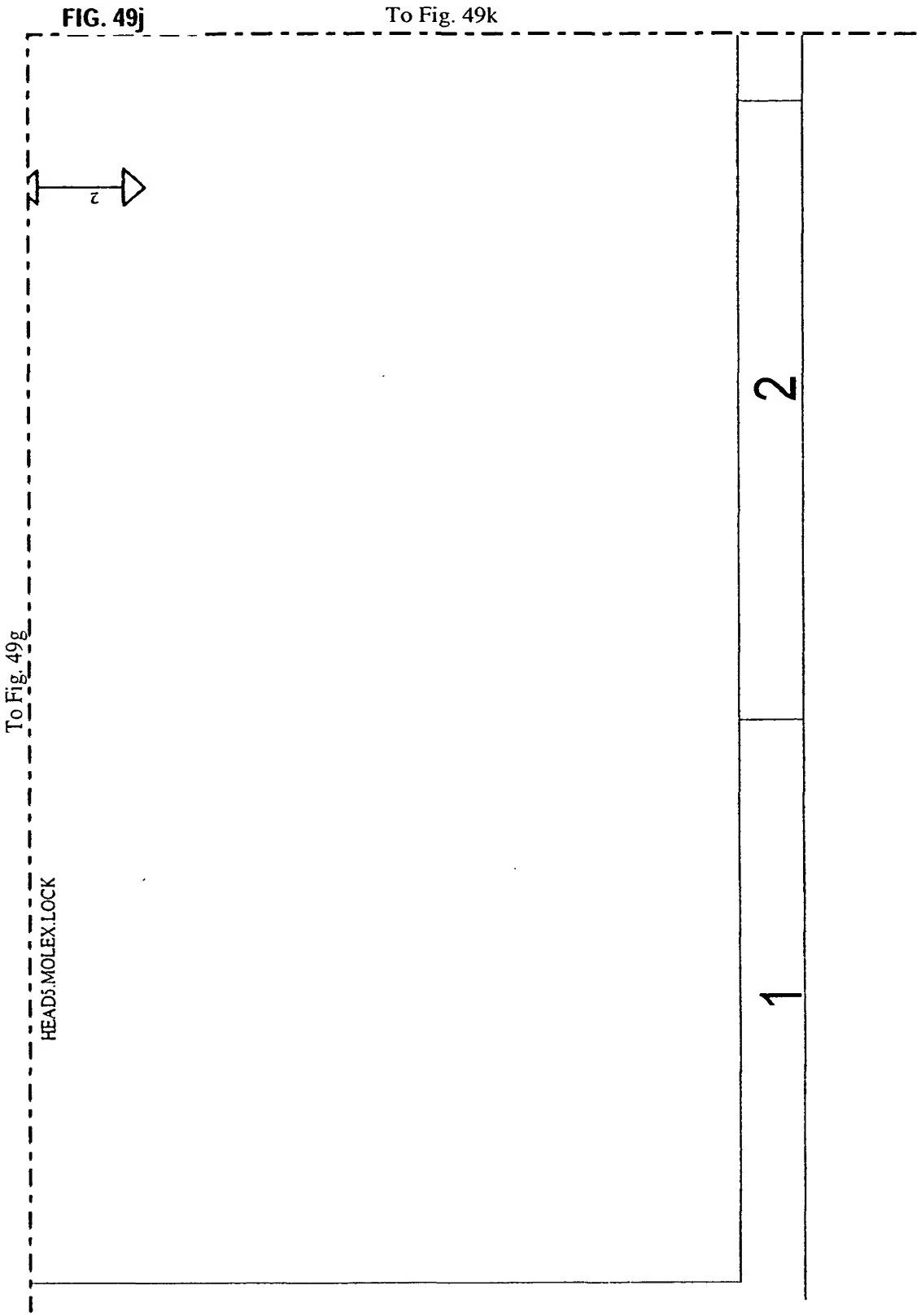
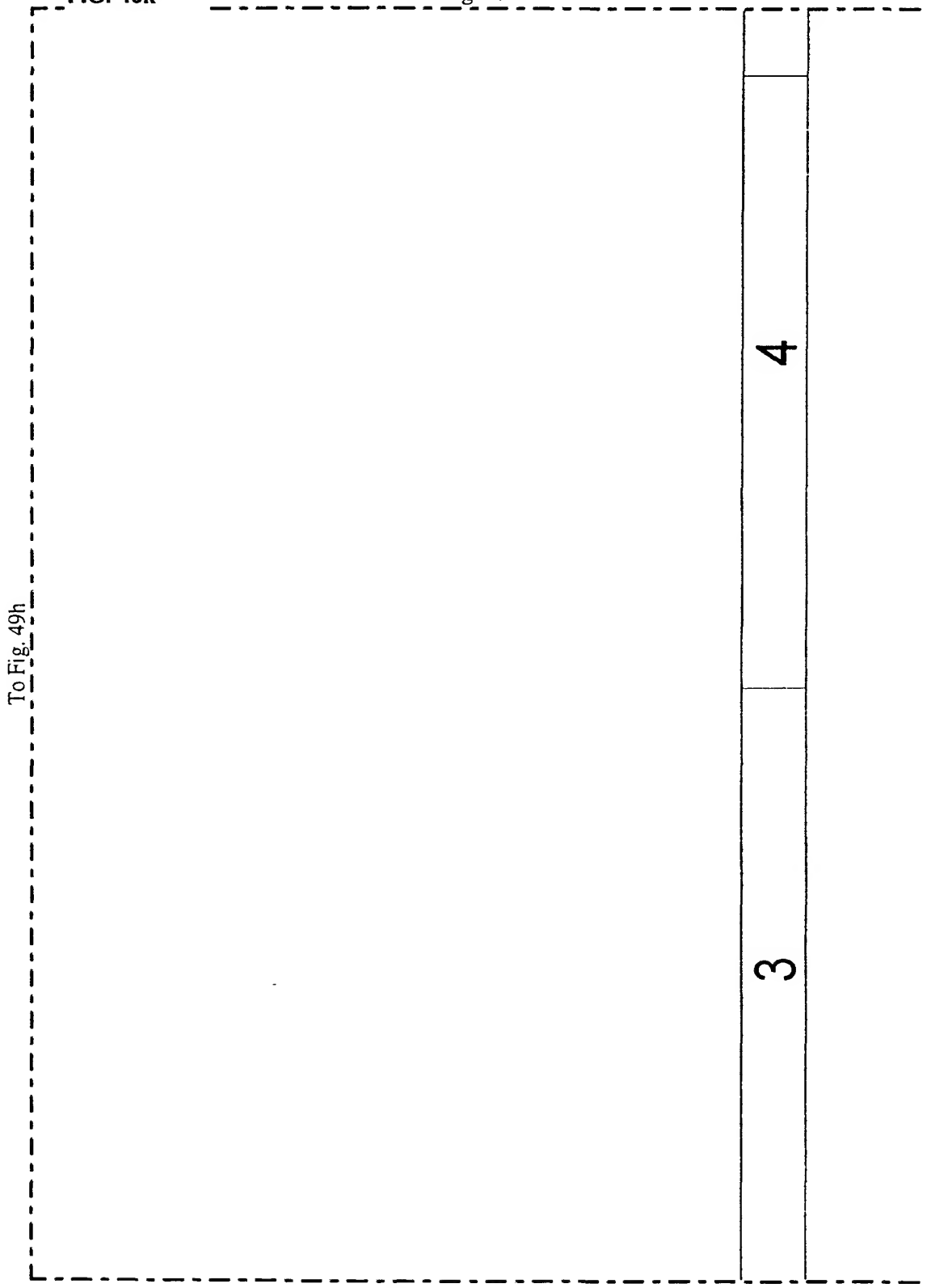


FIG. 49k

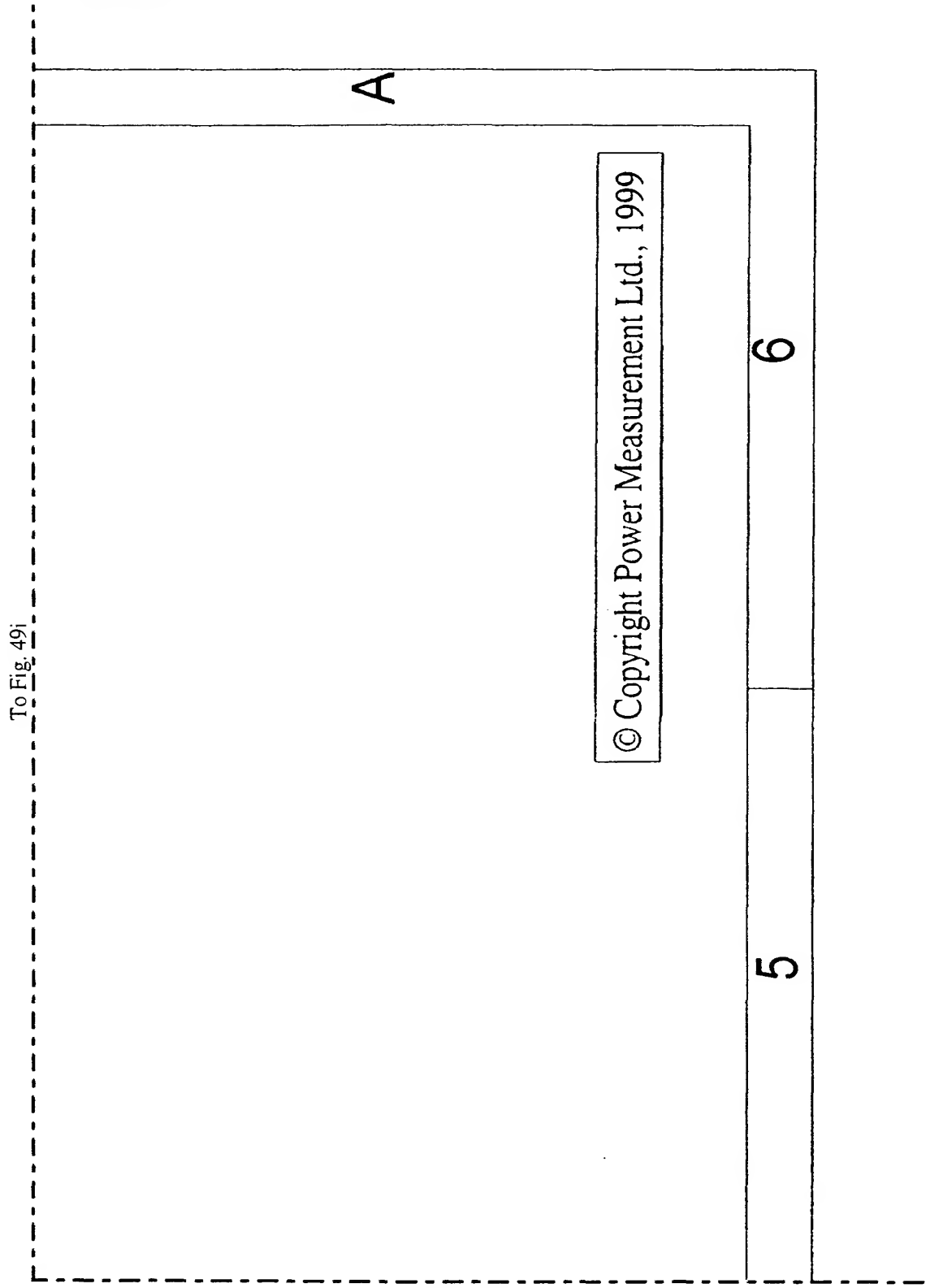
To Fig. 49l



To Fig. 49h

To Fig. 49j

FIG. 49l


A
6
5
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To Fig. 49i
To Fig. 49k

FIG. 50a

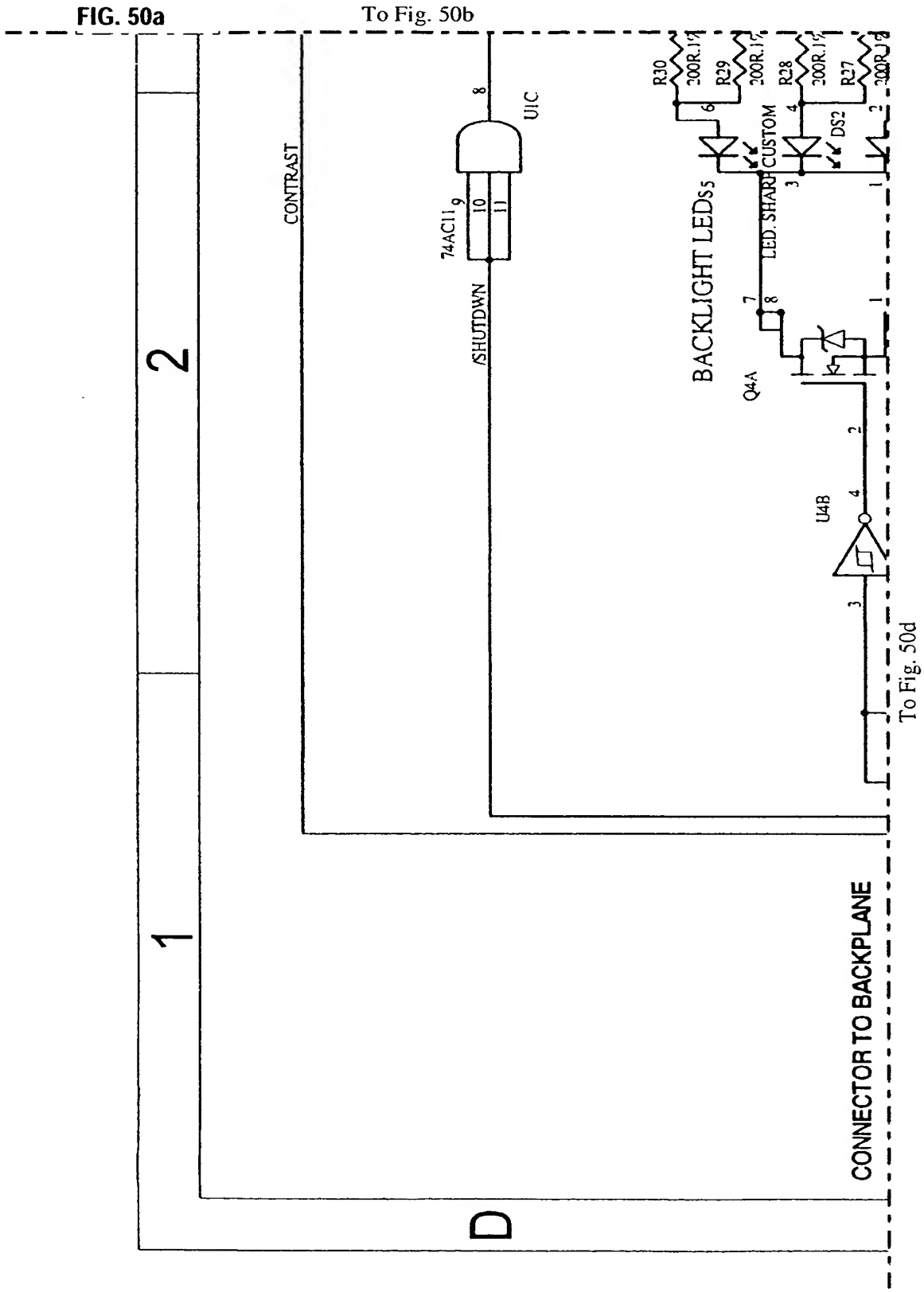

To Fig. 50b
CONTRAST
/SHUTDWN
74AC11
U1C
R30
R29
R28
R27
200R.1%
DS2
CUSTOM
LED SHARE
BACKLIGHT LEDSs
Q4A
U4B
To Fig. 50d
CONNECTOR TO BACKPLANE
2
1
D

FIG. 50b

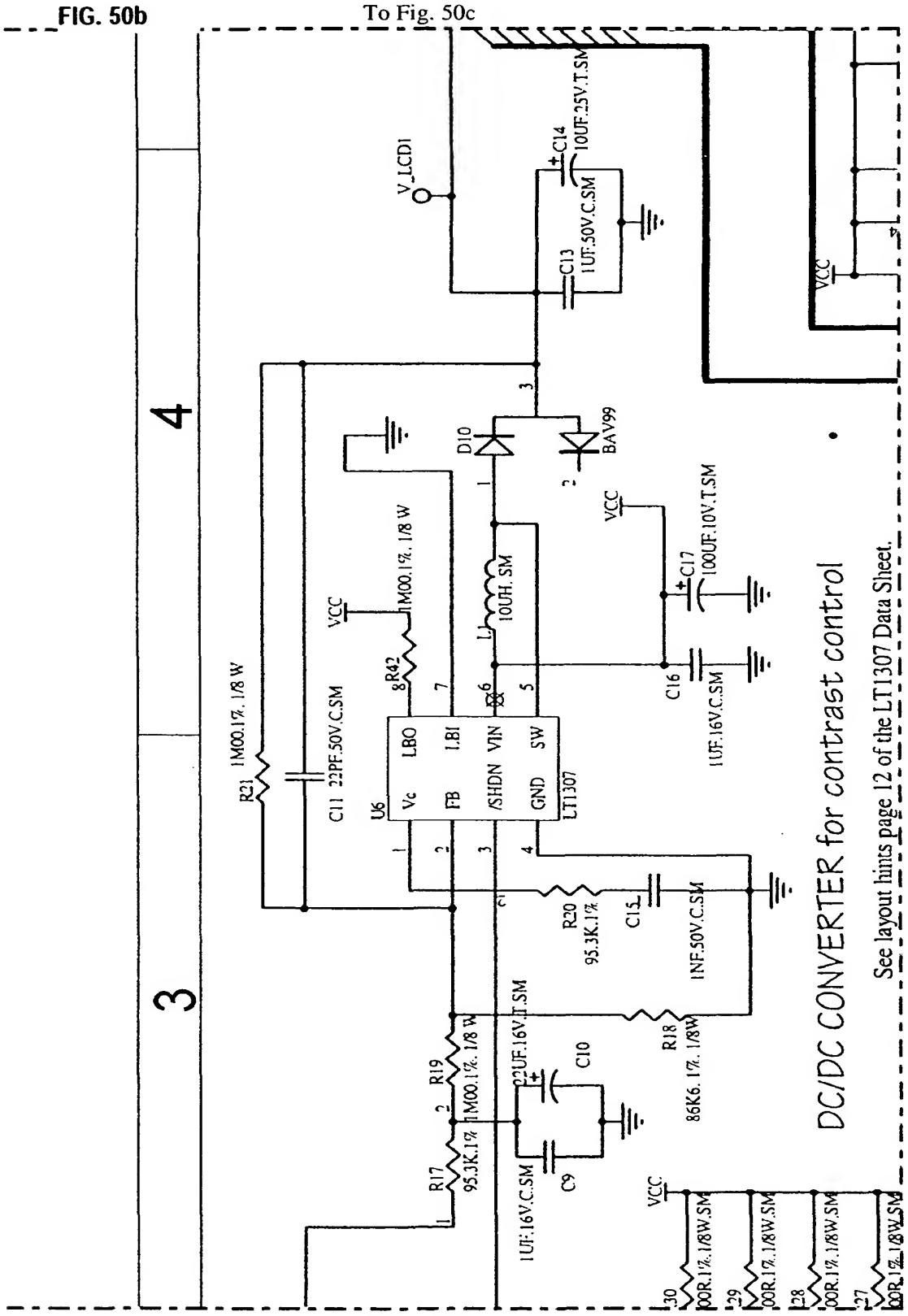

To Fig. 50c
V_LCD1
C14 10UF.25V.T.SM
C13 1UF.50V.C.SM
VCC
D10
BAV99
L1 10UH.SM
C17 100UF.10V.T.SM
C16 1UF.16V.C.SM
R42 1M00.1%.1/8 W
R21 1M00.1%.1/8 W
C11 22PF.50V.C.SM
U6 LT1307
Vc FB /SHDN GND LBO LBI VIN SW
R20 95.3K.1%
C15 1NF.50V.C.SM
R18 86K6.1%.1/8W
R19 1M00.1%.1/8 W
R17 95.3K.1%
C10 22UF.16V.T.SM
C9 1UF.16V.C.SM
R30 R29 R28 R27 00R.1%.1/8W.SM
DC/DC CONVERTER for contrast control
See layout hints page 12 of the LT1307 Data Sheet.
To Fig. 50e
To Fig. 50a

FIG. 50c

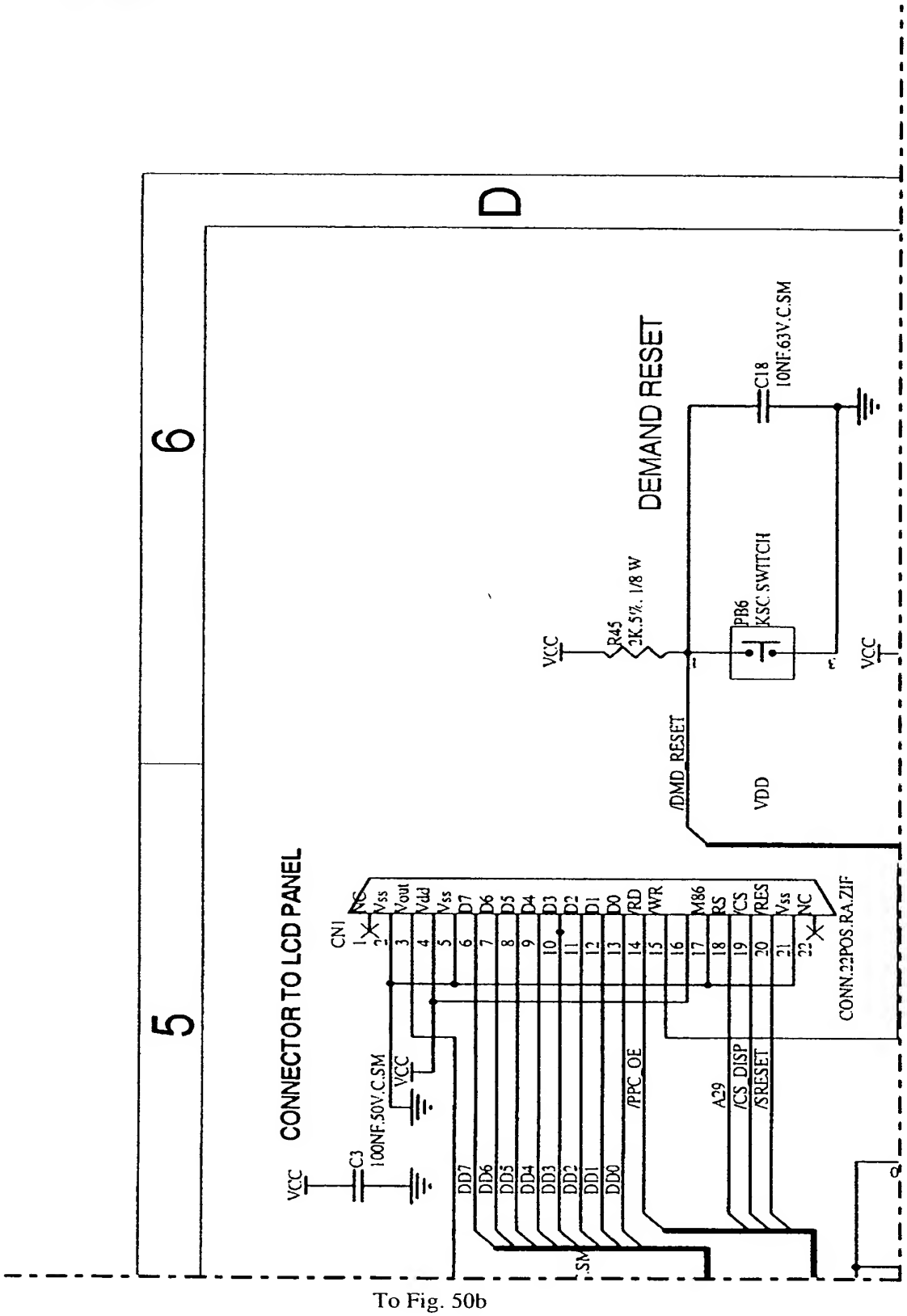

D
6
5
DEMAND RESET
C18
10NF.63V.C.SM
VCC
R45
2K.5%. 1/8 W
PB6
KSC.SWITCH
VCC
/DMD_RESET
VDD
To Fig. 50f
CONNECTOR TO LCD PANEL
CN1
NC
Vss
Vout
Vdd
Vss
D7
D6
D5
D4
D3
D2
D1
D0
/RD
/WR
M86
RS
/CS
/RES
Vss
NC
CONN.22POS.RA.ZIF
VCC
C3
100NF.50V.C.SM
VCC
DD7
DD6
DD5
DD4
DD3
DD2
DD1
DD0
/PPC_OE
A29
/CS_DISP
/SRESET
SM
To Fig. 50b

FIG. 50d

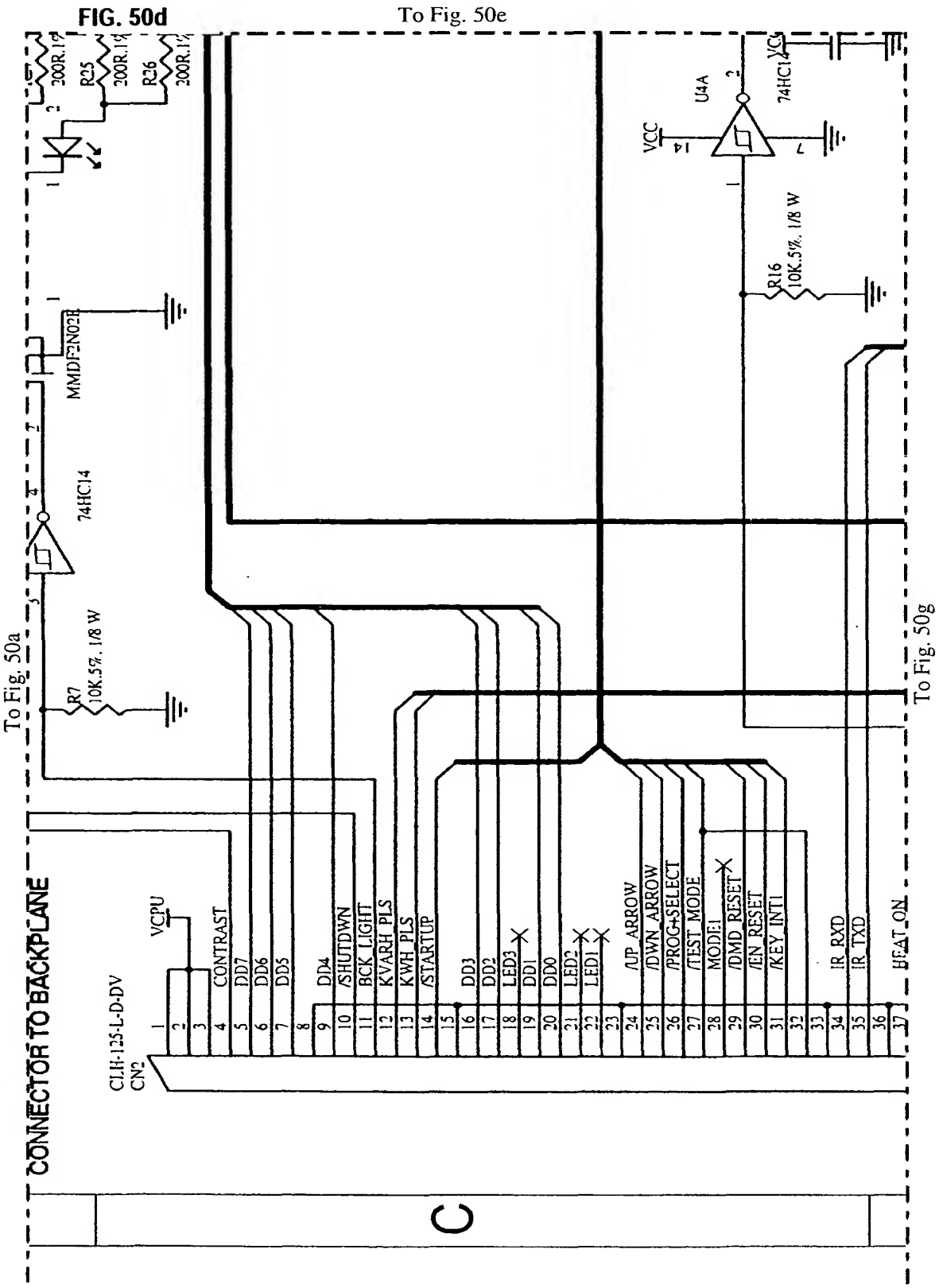

To Fig. 50e
To Fig. 50a
To Fig. 50g
CONNECTOR TO BACKPLANE
CLH-125-L-D-DV
CN2
VCPU
CONTRAST
DD7
DD6
DD5
DD4
/SHUTDWN
BCK_LIGHT
KVARH_PLS
KWH_PLS
/STARTUP
DD3
DD2
LED3
DD1
DD0
LED2
LED1
/UP_ARROW
/DWN_ARROW
/PROG+SELECT
/TEST_MODE
MODE1
/DMD_RESET
/EN_RESET
/KEY_INT1
IR_RXD
IR_TXD
HEAT_ON
74HC14
R7
10K.5%. 1/8 W
MMDF2N02E
R25
200R.1%
R26
200R.1%
U4A
74HC14
VCC
R16
10K.5%. 1/8 W

FIG. 50e

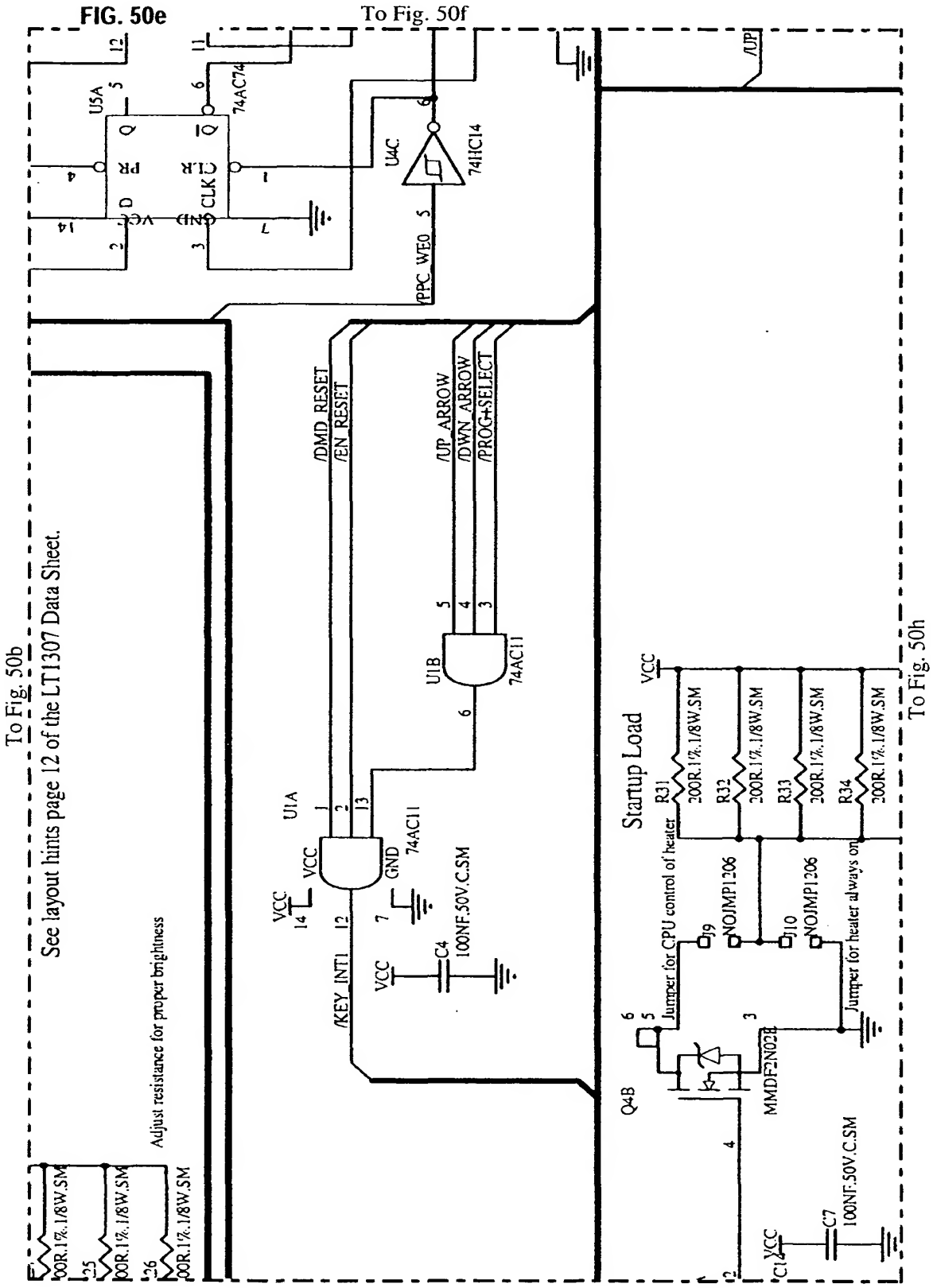

To Fig. 50f
To Fig. 50b
See layout hints page 12 of the LT1307 Data Sheet.
Adjust resistance for proper brightness
To Fig. 50h
To Fig. 50d
74AC74
74HC14
74AC11
74AC11
/DMD_RESET
/EN_RESET
/UP_ARROW
/DWN_ARROW
/PROG+SELECT
/KEY_INT1
/RPC_WE0
/UP
Startup Load
Jumper for CPU control of heater
Jumper for heater always on
MMDF2N02E
100NF.50V.C.SM
200R.1%.1/8W.SM
NOJMP1206
VCC
GND

FIG. 50f

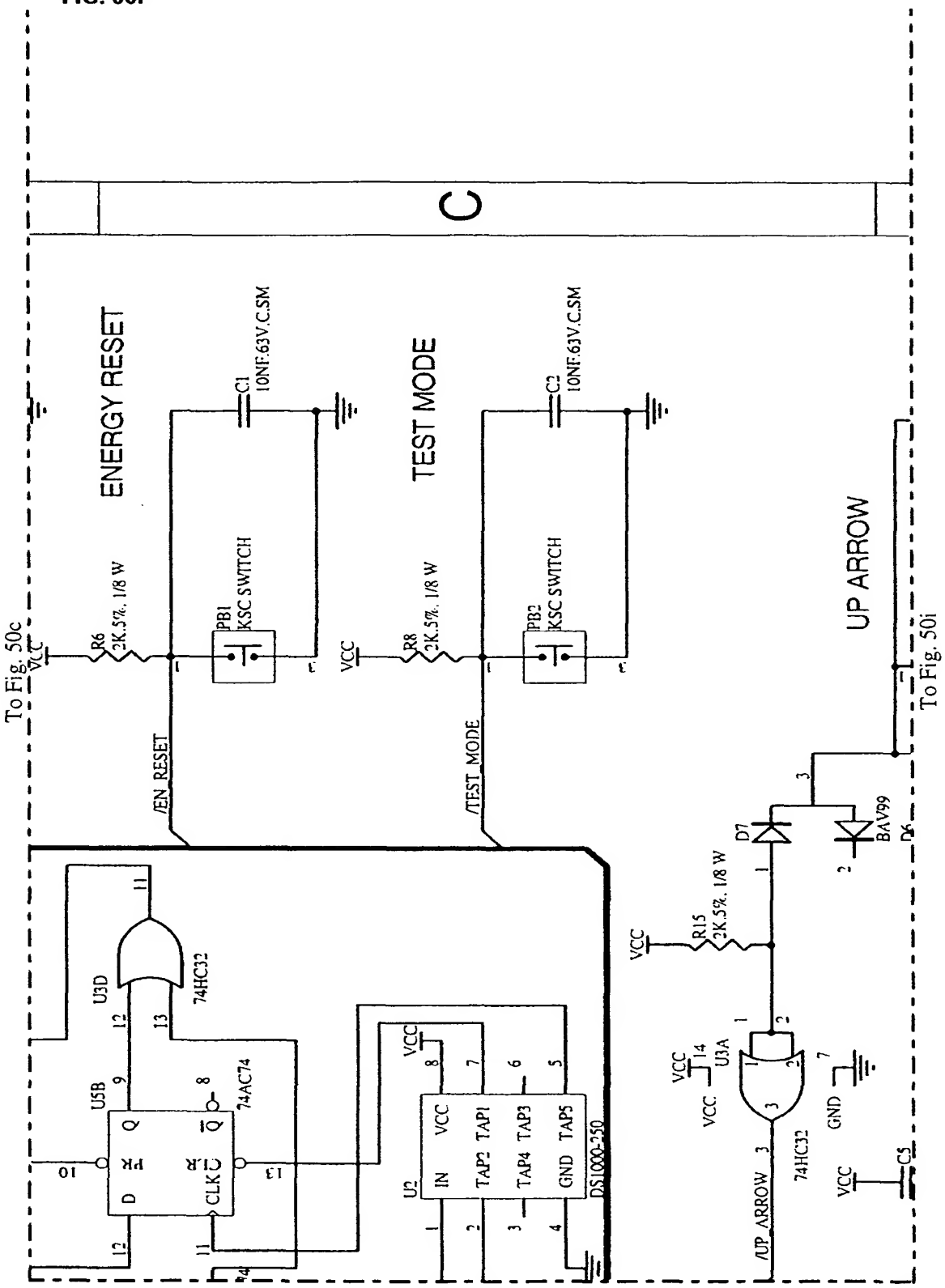

C
ENERGY RESET
TEST MODE
UP ARROW
C1
10NF.63V.C.SM
C2
10NF.63V.C.SM
PB1
KSC SWITCH
PB2
KSC SWITCH
R6
2K.5%. 1/8 W
R8
2K.5%. 1/8 W
R15
2K.5%. 1/8 W
VCC
/EN_RESET
/TEST_MODE
/UP_ARROW
To Fig. 50c
To Fig. 50i
To Fig. 50e
U3D
74HC32
U5B
74AC74
U2
DS1000-250
U3A
74HC32
D7
D6
BAV99
GND
C5

FIG. 50g

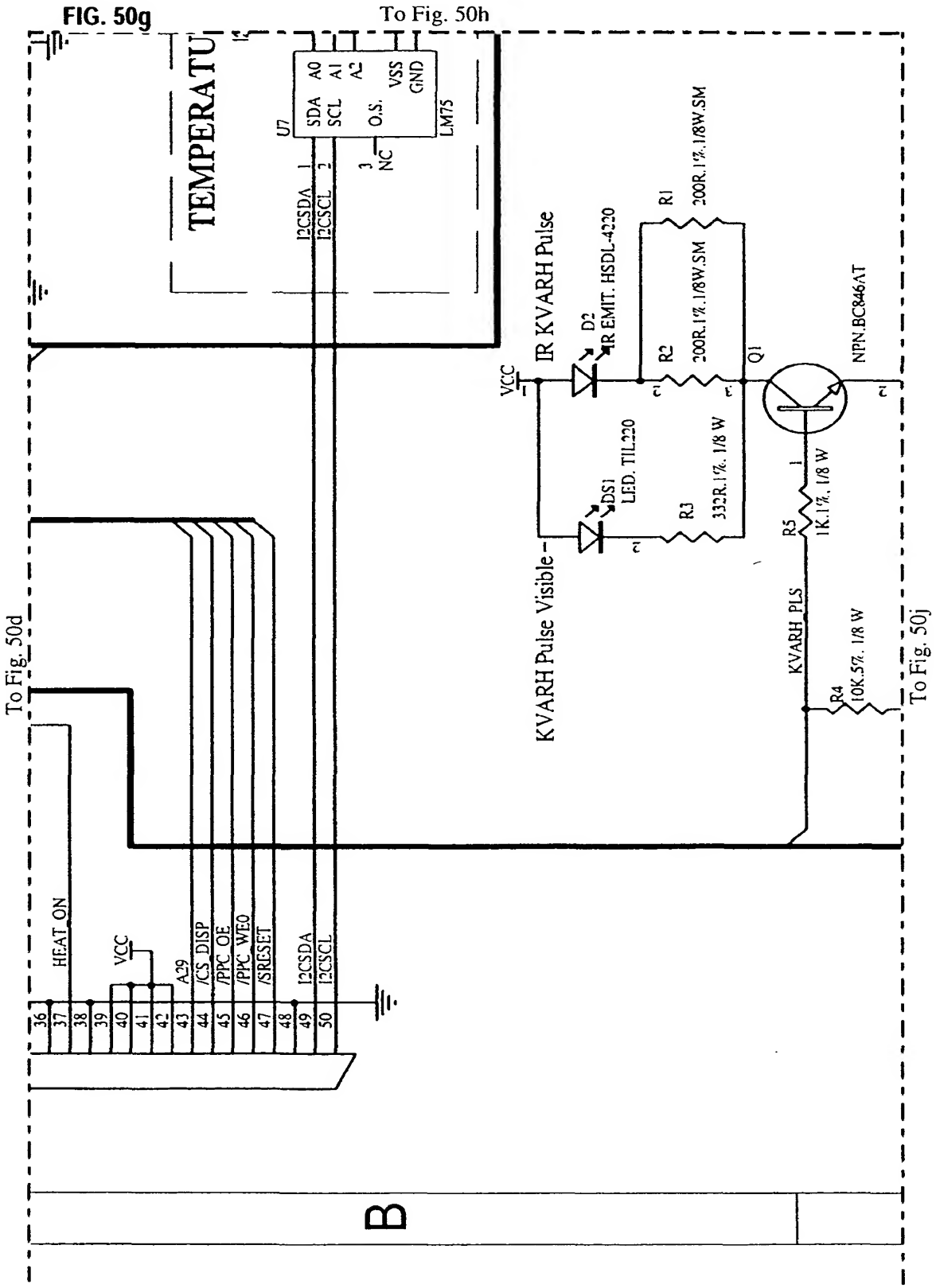
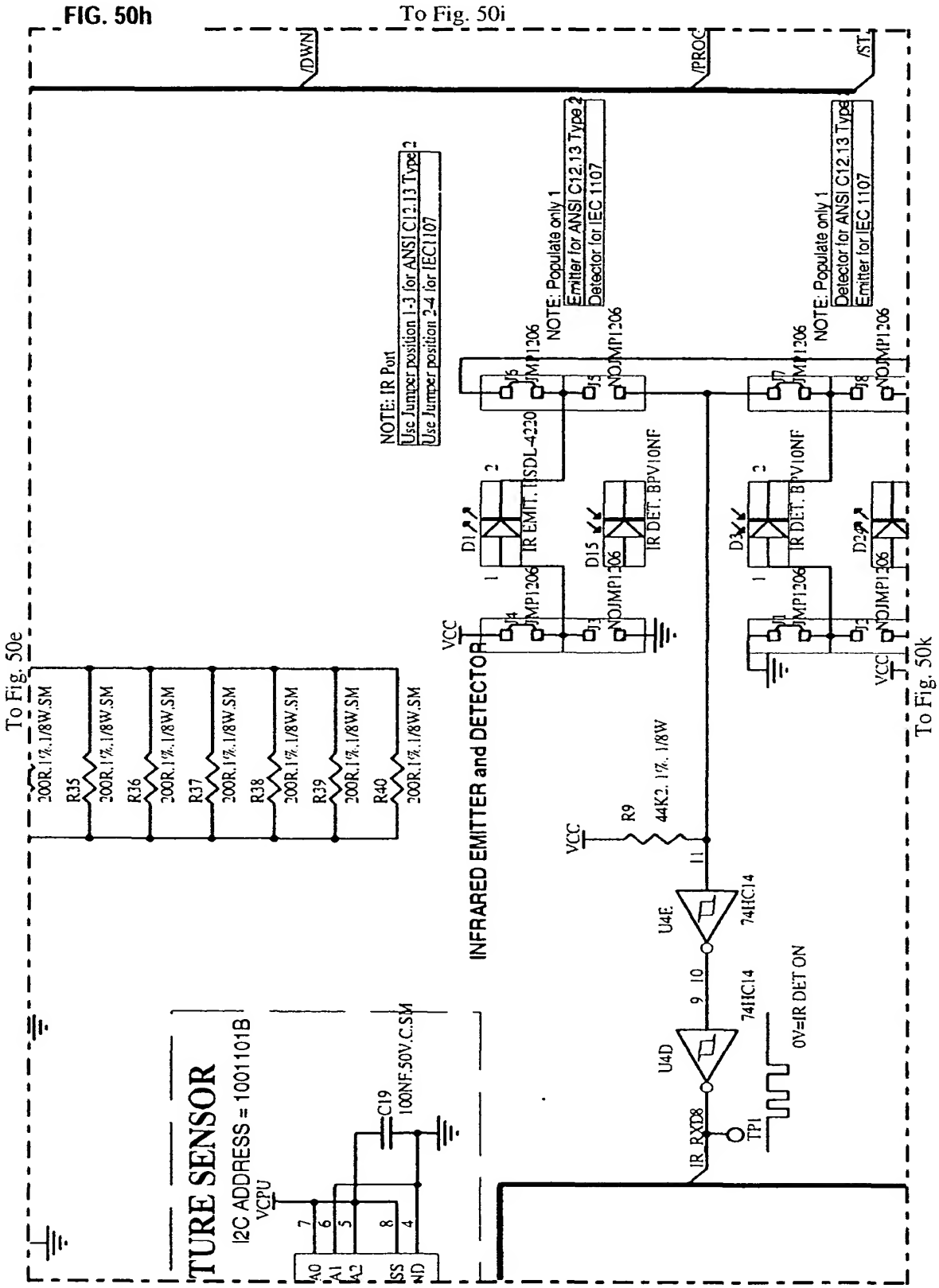

To Fig. 50h
TEMPERATU
U7
SDA
SCL
O.S.
A0
A1
A2
VSS
GND
LM75
NC
I2CSDA
I2CSCL
IR KVARH Pulse
D2
IR EMIT. HSDL-4220
R1
200R.1%.1/8W.SM
R2
200R.1%.1/8W.SM
Q1
NPN.BC846AT
VCC
DS1
LED. TIL220
R3
332R.1%. 1/8 W
R5
1K.1%. 1/8 W
KVARH Pulse Visible
KVARH_PLS
R4
10K.5%. 1/8 W
To Fig. 50j
To Fig. 50d
HEAT_ON
VCC
A29
/CS_DISP
/PPC_OE
/PPC_WE0
/SRESET
I2CSDA
I2CSCL
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
B

FIG. 50h



To Fig. 50g

FIG. 50i

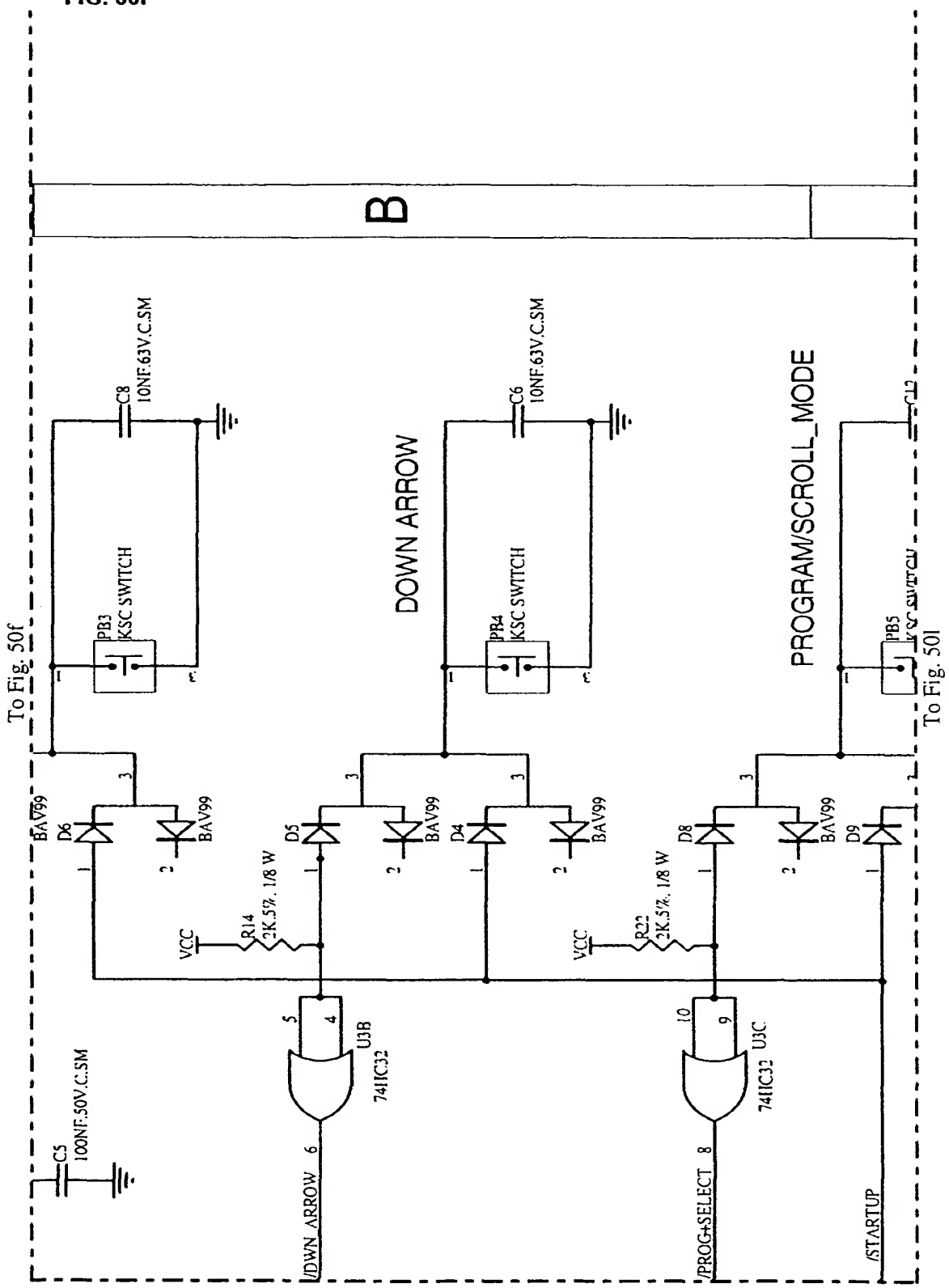

B
DOWN ARROW
PROGRAM/SCROLL_MODE
C8 10NF.63V.C.SM
C6 10NF.63V.C.SM
C12
PB3 KSC SWITCH
PB4 KSC SWITCH
PB5
To Fig. 50f
To Fig. 50l
D6 BAV99
D5 BAV99
D4 BAV99
D8 BAV99
D9
R14 2K.5%. 1/8 W
R22 2K.5%. 1/8 W
VCC
C5 100NF.50V.C.SM
U3B 74HC32
U3C 74HC32
/DWN_ARROW
/PROG+SELECT
/STARTUP
To Fig. 50h

FIG. 50j

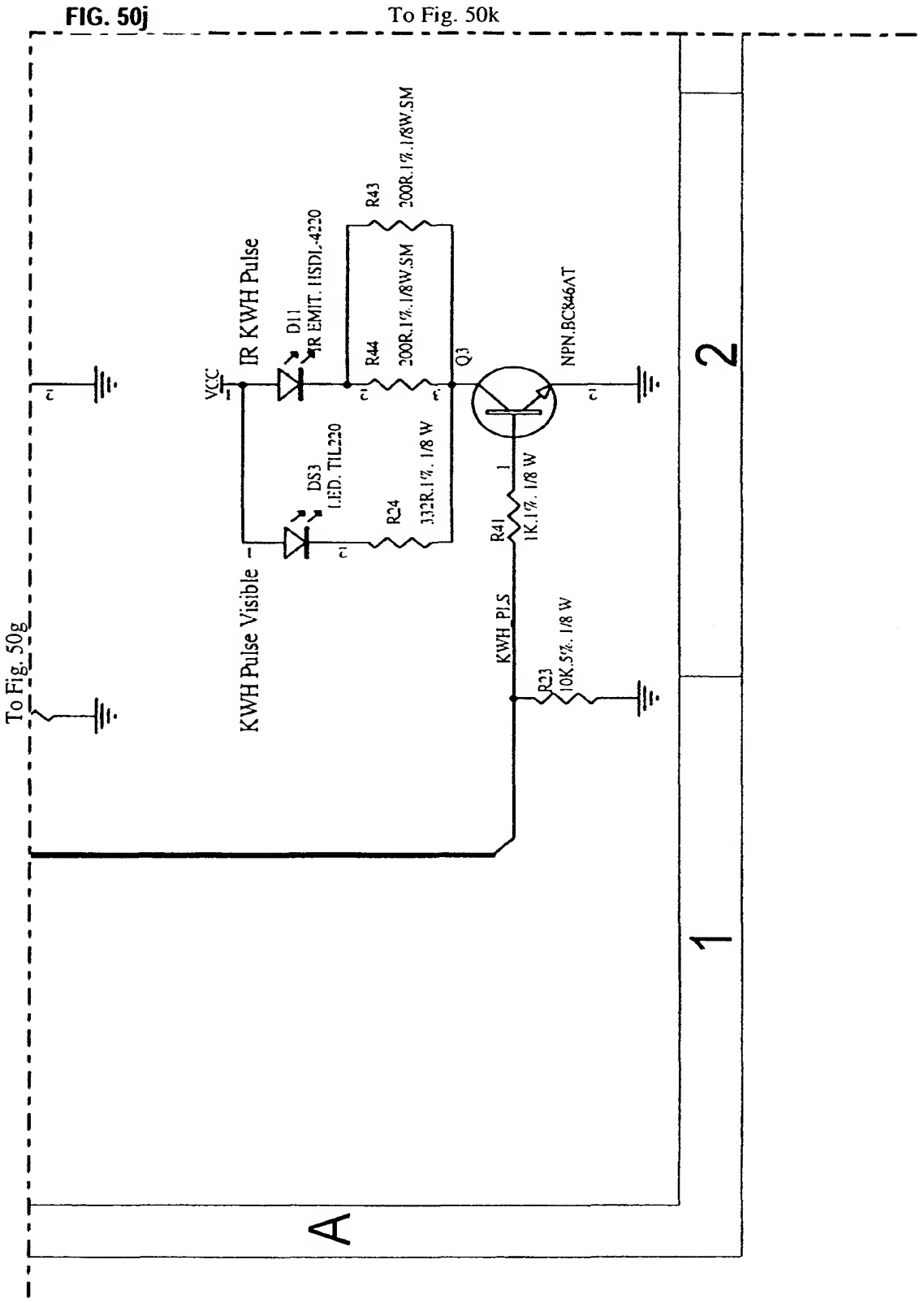

To Fig. 50k
To Fig. 50g
VCC
IR KWH Pulse
KWH Pulse Visible
D11
IR EMIT. HSDL-4220
R43
200R.1%.1/8W.SM
R44
200R.1%.1/8W.SM
Q3
NPN.BC846AT
DS3
LED. TIL220
R24
332R.1%. 1/8 W
R41
1K.1%. 1/8 W
KWH PLS
R23
10K.5%. 1/8 W
1
2
A

FIG. 50k

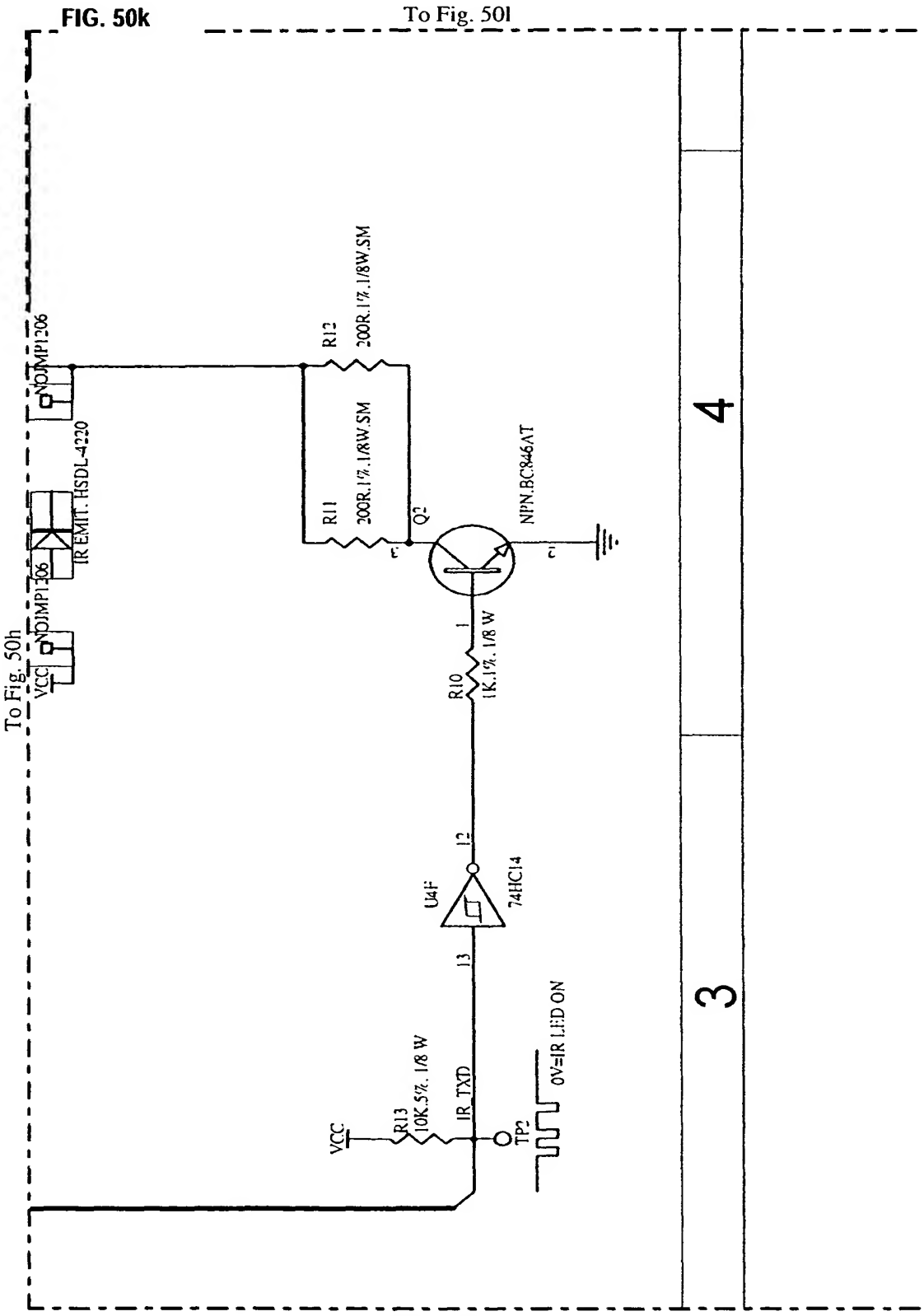
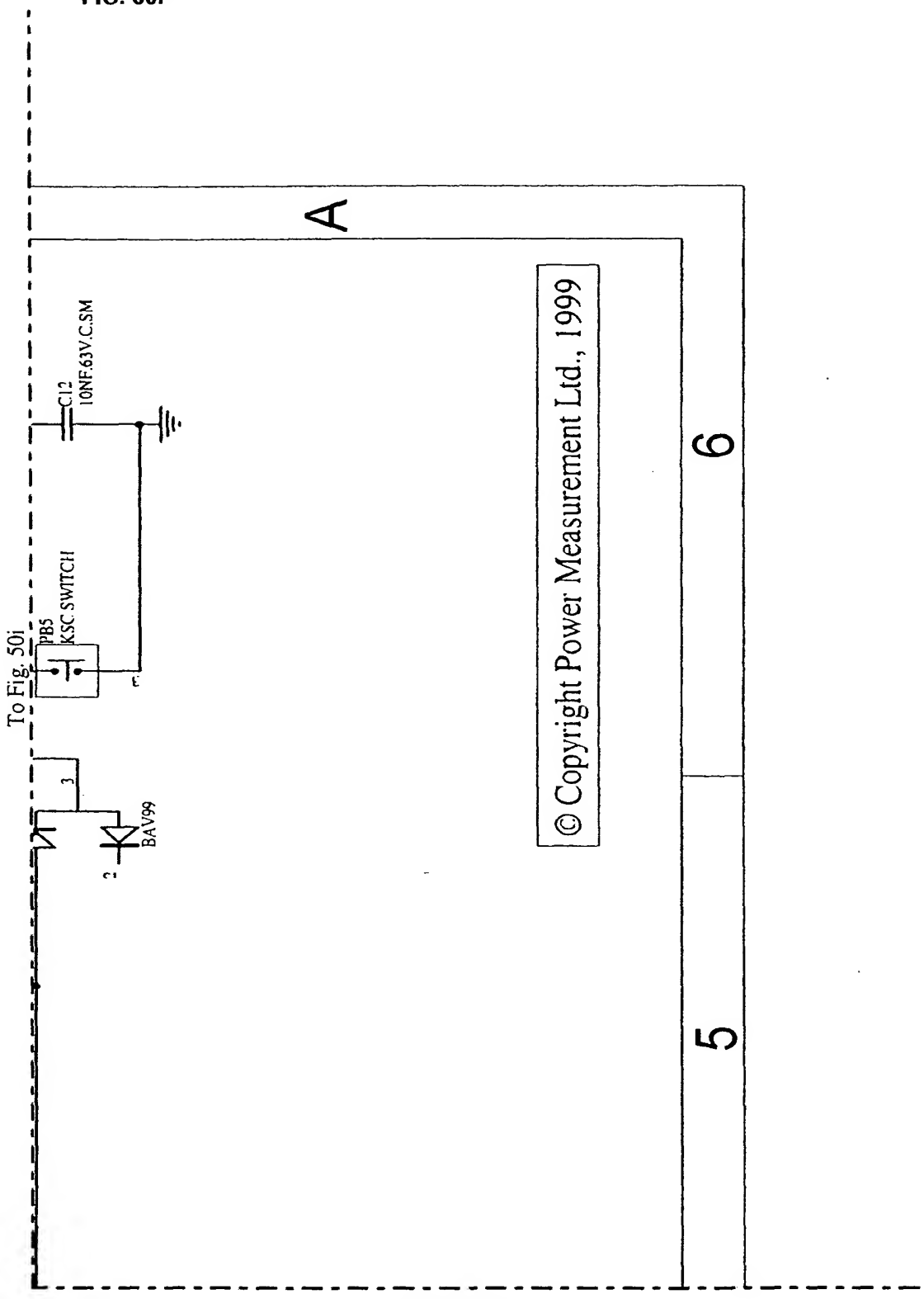

To Fig. 50l
To Fig. 50h
NDJMP1206
IR EMIT. HSDL-4220
NDJMP1206
VCC
R12
200R.1%.1/8W.SM
R11
200R.1%.1/8W.SM
Q2
NPN.BC846AT
R10
1K.1%. 1/8 W
U4F
74HC14
R13
10K.5%. 1/8 W
IR TXD
TP2
0V=IR LED ON
VCC
4
3
To Fig. 50j

FIG. 50l



To Fig. 50k

FIG. 51a

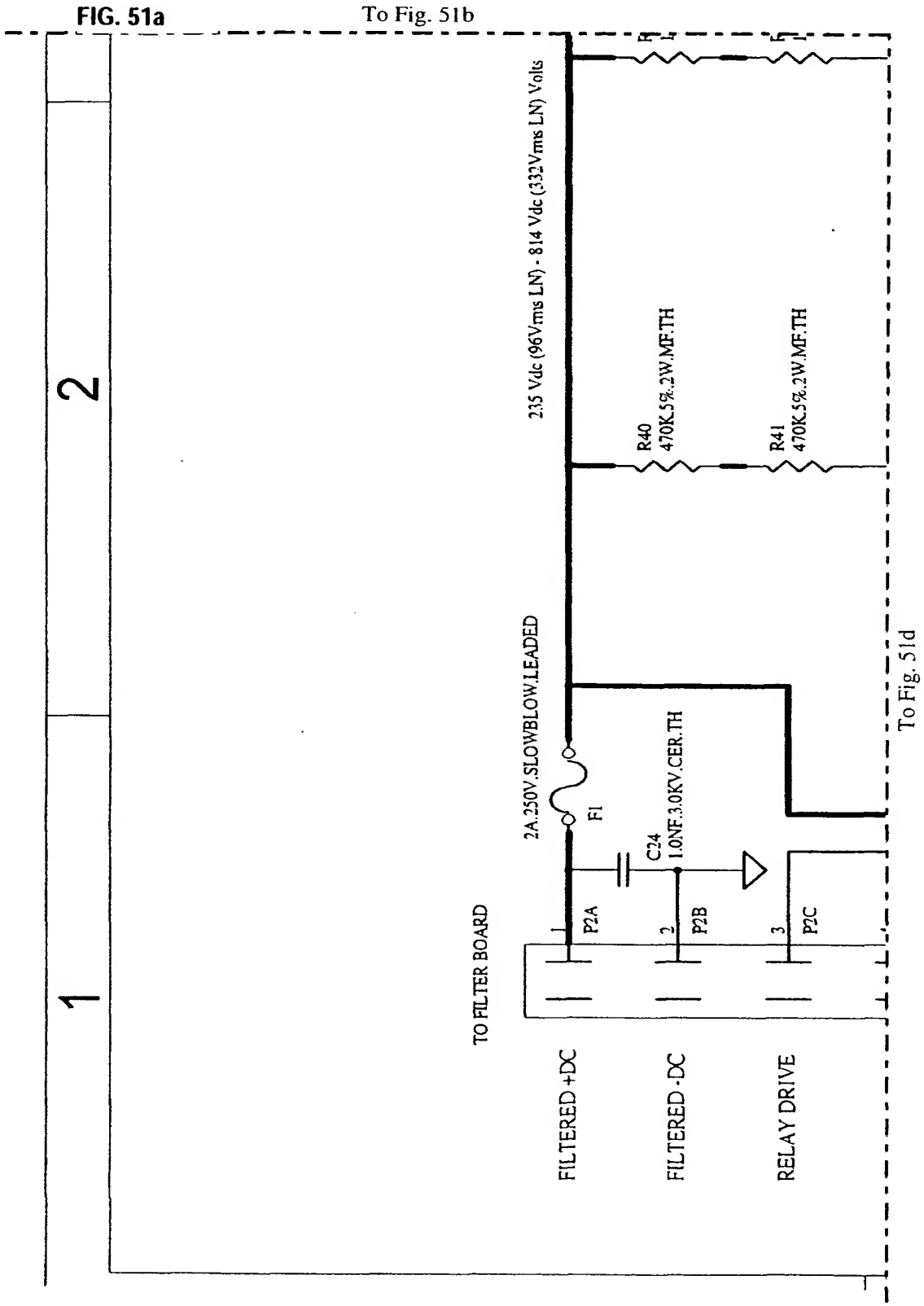

To Fig. 51b
235 Vdc (96Vrms LN) - 814 Vdc (332Vrms LN) Volts
R40
470K.5%.2W.MF.TH
R41
470K.5%.2W.MF.TH
2A.250V.SLOWBLOW.LEADED
F1
C24
1.0NF.3.0KV.CER.TH
TO FILTER BOARD
P2A
P2B
P2C
FILTERED +DC
FILTERED -DC
RELAY DRIVE
To Fig. 51d
1
2

FIG. 51b

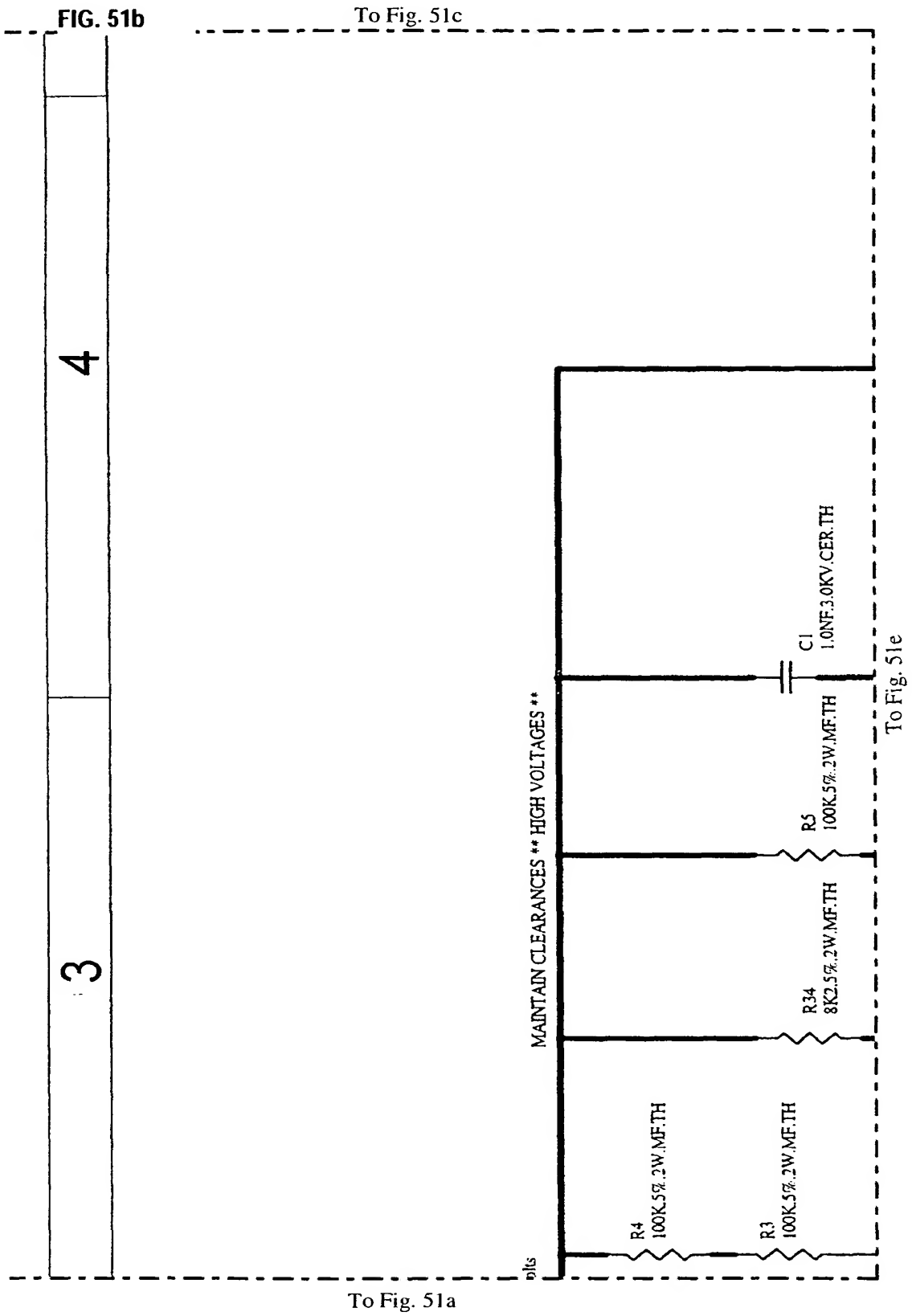

To Fig. 51c
4
3
MAINTAIN CLEARANCES ** HIGH VOLTAGES **
C1
1.0NF.3.0KV.CER.TH
R5
100K.5%.2W.MF.TH
R34
8K2.5%.2W.MF.TH
R4
100K.5%.2W.MF.TH
R3
100K.5%.2W.MF.TH
To Fig. 51e
To Fig. 51a

FIG. 51c

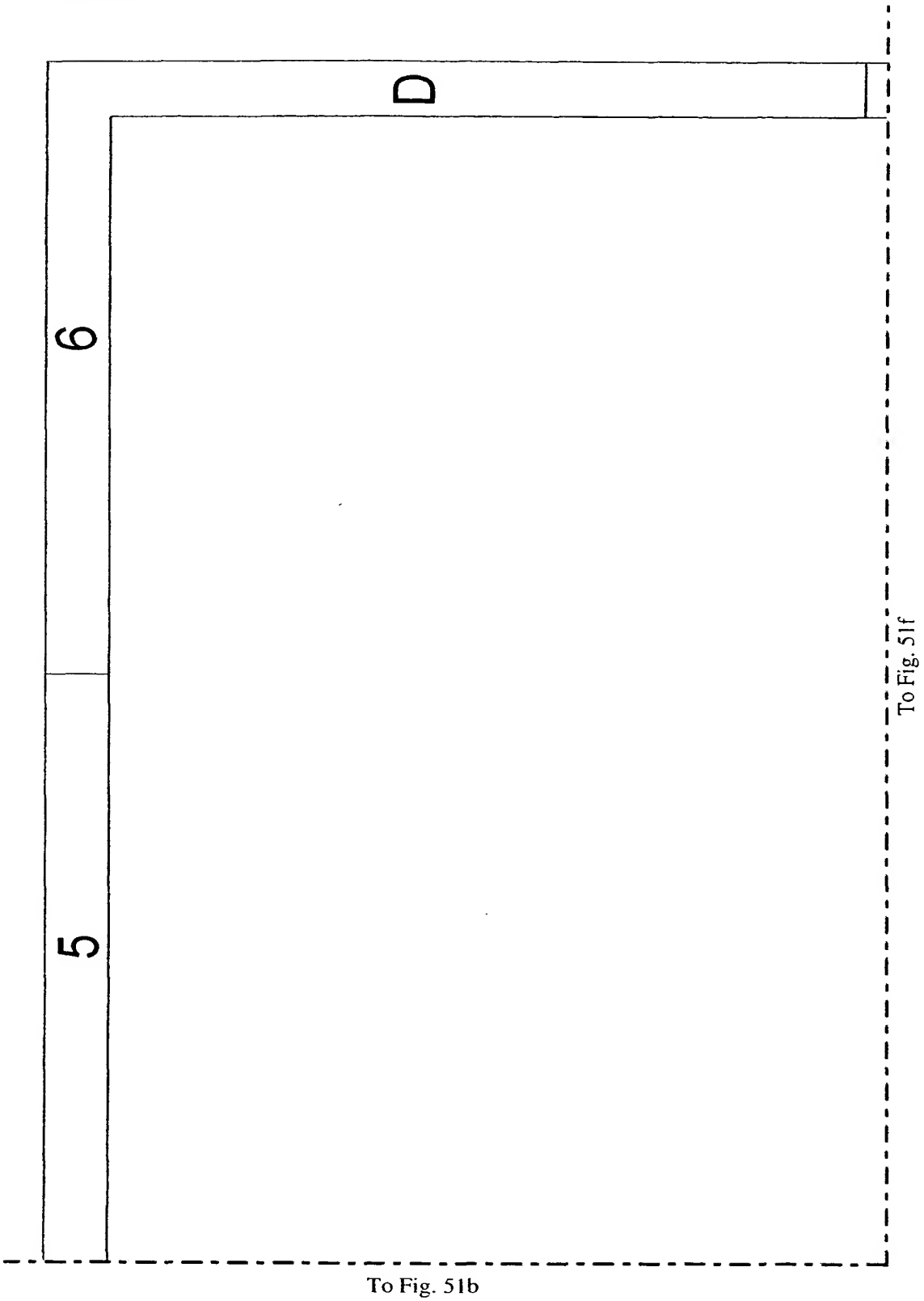


FIG. 51d

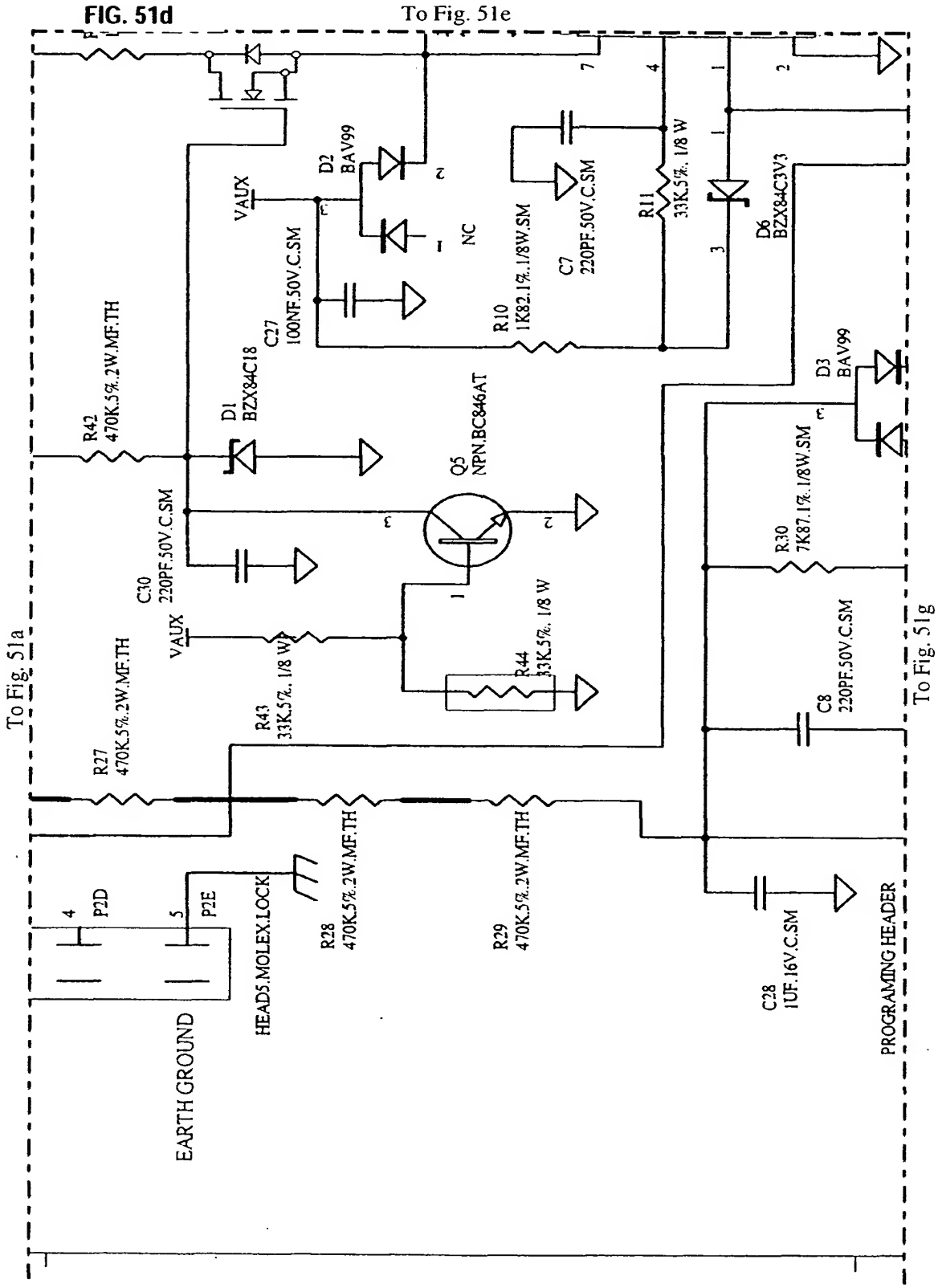

To Fig. 51e
To Fig. 51a
To Fig. 51g
VAUX
D2 BAV99
NC
C27 100NF.50V.C.SM
C7 220PF.50V.C.SM
R11 33K.5%. 1/8 W
D6 BZX84C3V3
R10 1K82.1%.1/8W.SM
R42 470K.5%.2W.MF.TH
D1 BZX84C18
Q5 NPN.BC846AT
D3 BAV99
R30 7K87.1%.1/8W.SM
C30 220PF.50V.C.SM
R44 33K.5%. 1/8 W
R43 33K.5%. 1/8 W
C8 220PF.50V.C.SM
R27 470K.5%.2W.MF.TH
R28 470K.5%.2W.MF.TH
R29 470K.5%.2W.MF.TH
P2D
P2E
HEAD5.MOLEX.LOCK
EARTH GROUND
C28 1UF.16V.C.SM
PROGRAMING HEADER

FIG. 51e

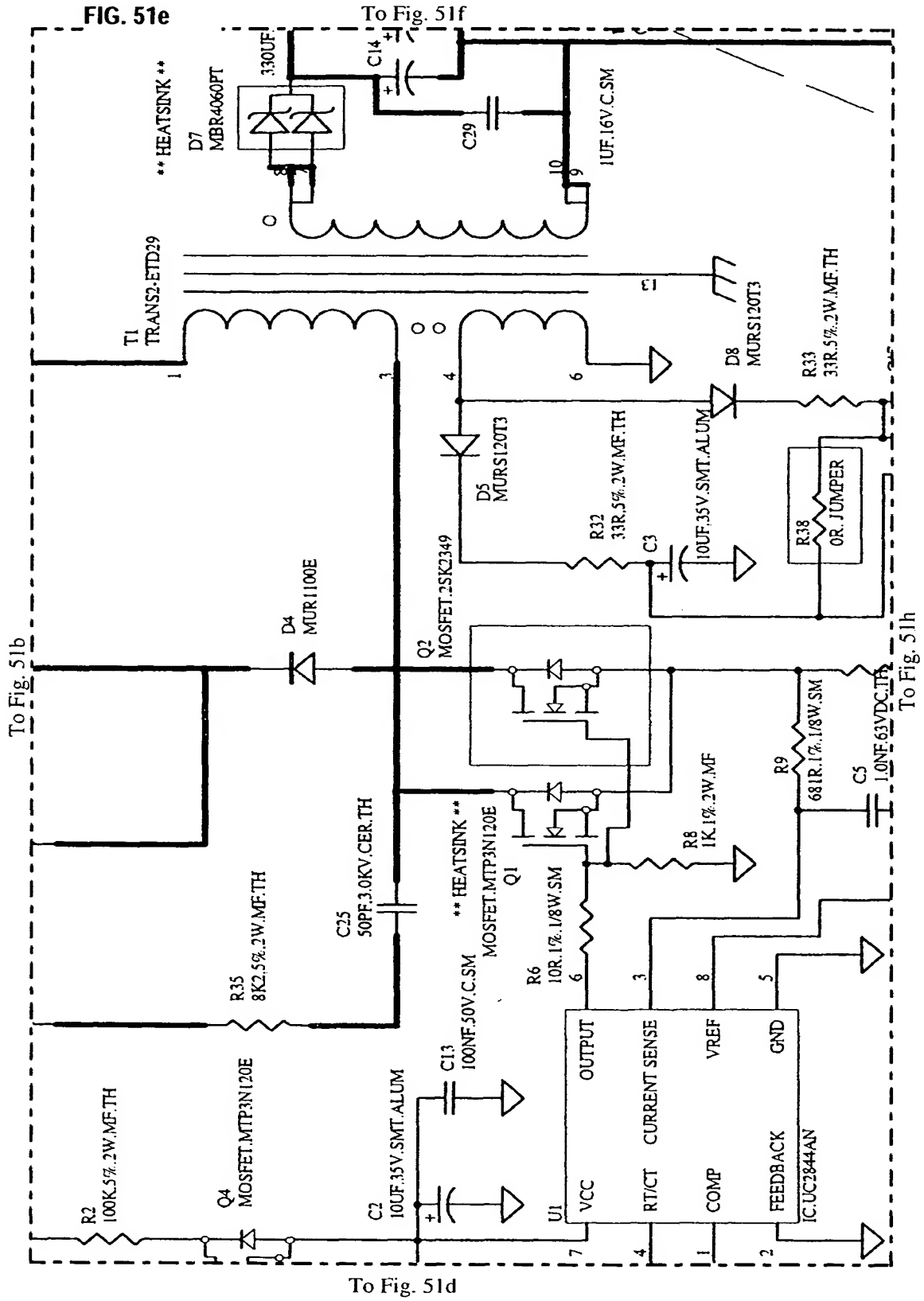

To Fig. 51f
To Fig. 51b
To Fig. 51h
To Fig. 51d
T1 TRANS2:ETD29
D7 MBR4060PT
** HEATSINK **
330UF
C14
C29
1UF.16V.C.SM
D8 MURS120T3
R33 33R.5%.2W.MF.TH
D5 MURS120T3
R32 33R.5%.2W.MF.TH
C3 10UF.35V.SMT.ALUM
R38 0R.JUMPER
D4 MUR1100E
Q2 MOSFET.2SK2349
R9 681R.1%.1/8W.SM
C5 1.0NF.63VDC.TF
R8 1K.1%.2W.MF
** HEATSINK **
Q1 MOSFET.MTP3N120E
C25 50PF.3.0KV.CER.TH
R35 8K2.5%.2W.MF.TH
R6 10R.1%.1/8W.SM
C13 100NF.50V.C.SM
Q4 MOSFET.MTP3N120E
R2 100K.5%.2W.MF.TH
C2 10UF.35V.SMT.ALUM
U1 IC.UC2844AN
OUTPUT
CURRENT SENSE
VREF
GND
VCC
RT/CT
COMP
FEEDBACK

FIG. 51f

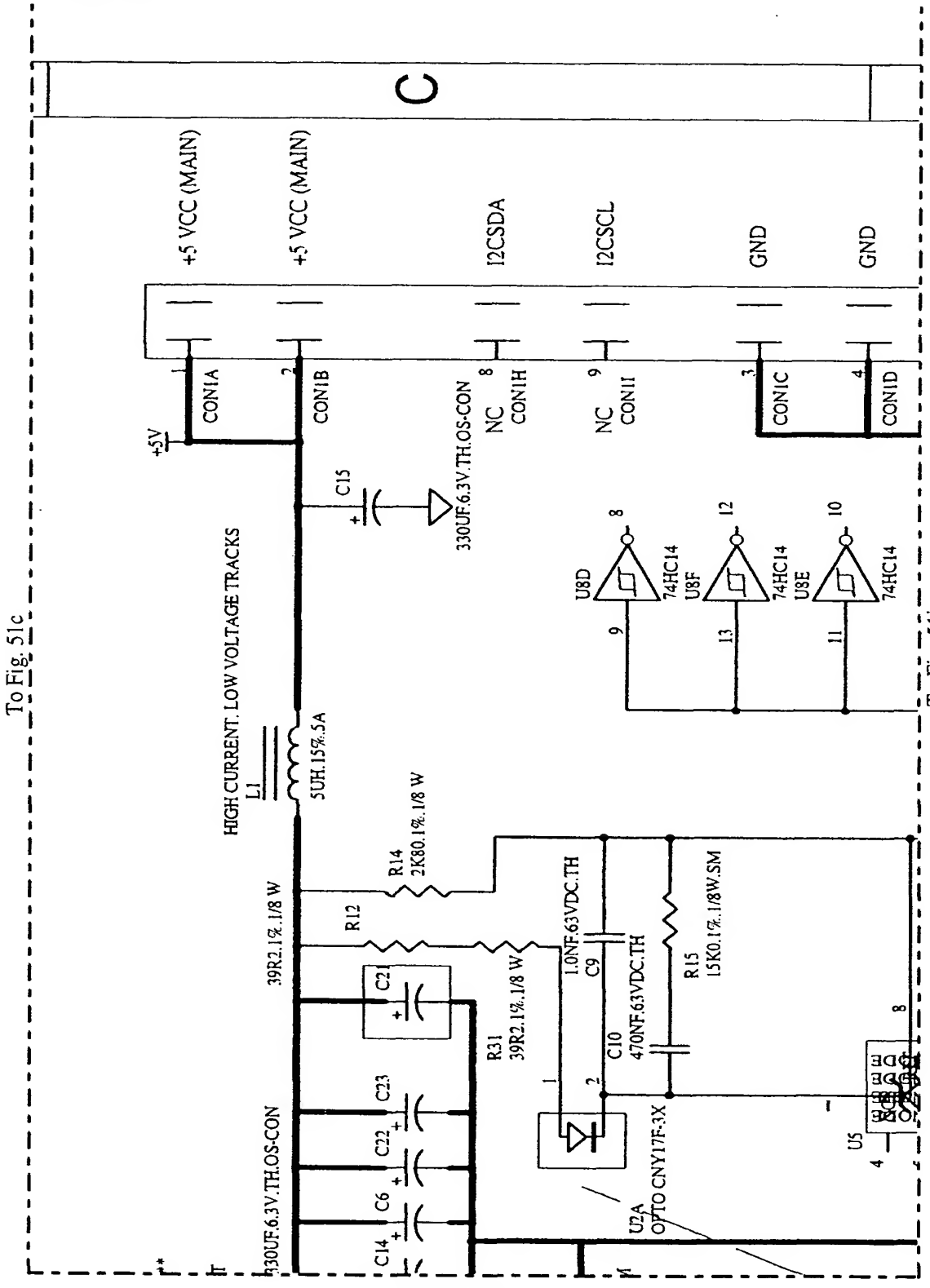

C
+5 VCC (MAIN)
+5 VCC (MAIN)
I2CSDA
I2CSCL
GND
GND
CON1A
CON1B
CON1H
CON1I
CON1C
CON1D
+5V
C15
330UF.6.3V.TH.OS-CON
NC
NC
U8D
74HC14
U8F
74HC14
U8E
74HC14
To Fig. 51c
To Fig. 51i
HIGH CURRENT. LOW VOLTAGE TRACKS
L1
5UH.15%.5A
R14
2K80.1%.1/8 W
R12
39R2.1%.1/8 W
C21
R31
39R2.1%.1/8 W
1.0NF.63VDC.TH
C9
C10
470NF.63VDC.TH
R15
15K0.1%.1/8W.SM
C23
C22
C6
C14
330UF.6.3V.TH.OS-CON
U2A
OPTO CNY17F-3X
U5
To Fig. 51e

FIG. 51g

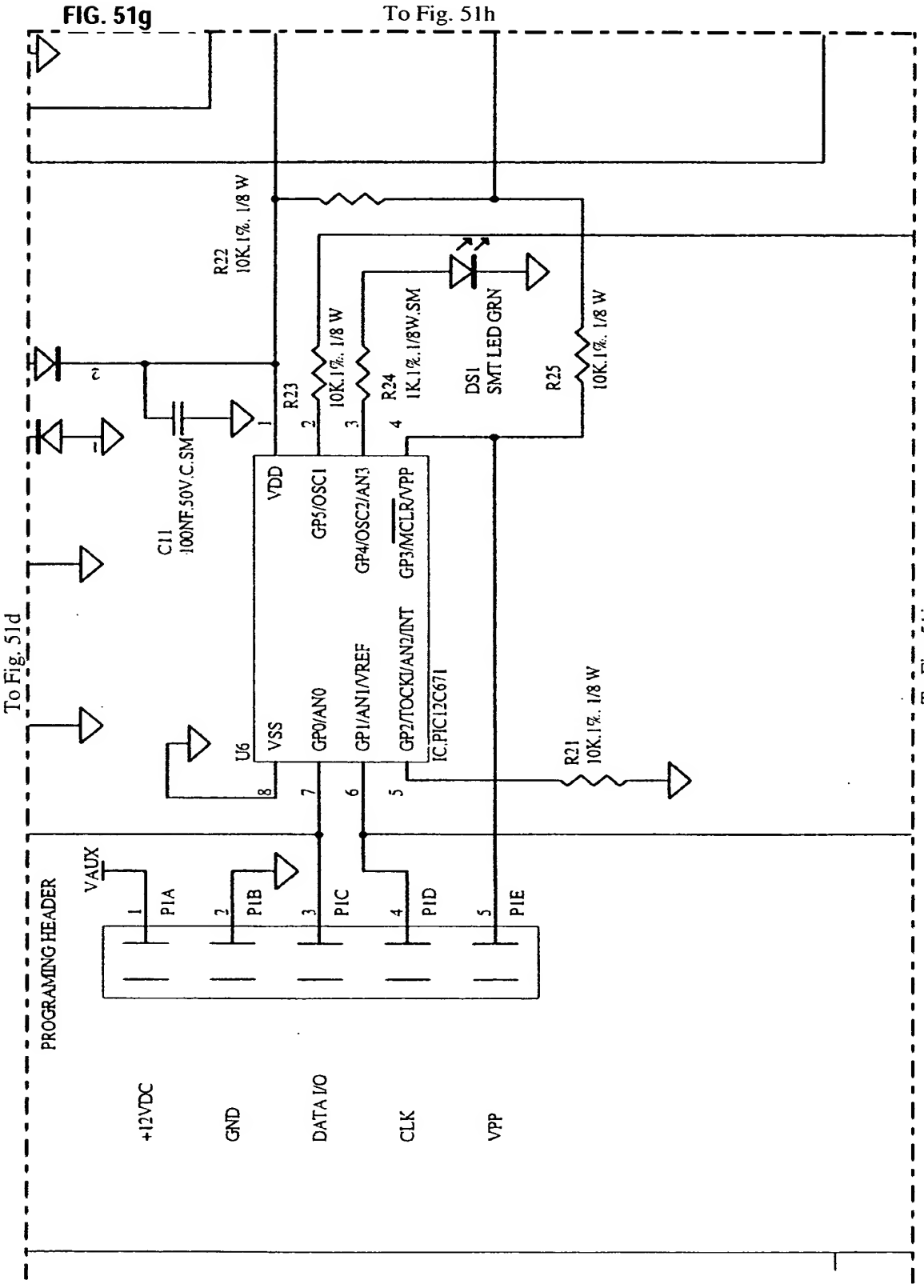

To Fig. 51h
To Fig. 51d
To Fig. 51j
R22
10K.1%. 1/8 W
R23
10K.1%. 1/8 W
R24
1K.1%.1/8W.SM
DS1
SMT LED GRN
R25
10K.1%. 1/8 W
C11
100NF.50V.C.SM
U6
IC.PIC12C671
VDD
GP5/OSC1
GP4/OSC2/AN3
GP3/MCLR/VPP
VSS
GP0/AN0
GP1/AN1/VREF
GP2/T0CKI/AN2/INT
R21
10K.1%. 1/8 W
PROGRAMING HEADER
VAUX
P1A
P1B
P1C
P1D
P1E
+12VDC
GND
DATA I/O
CLK
VPP

FIG. 51h

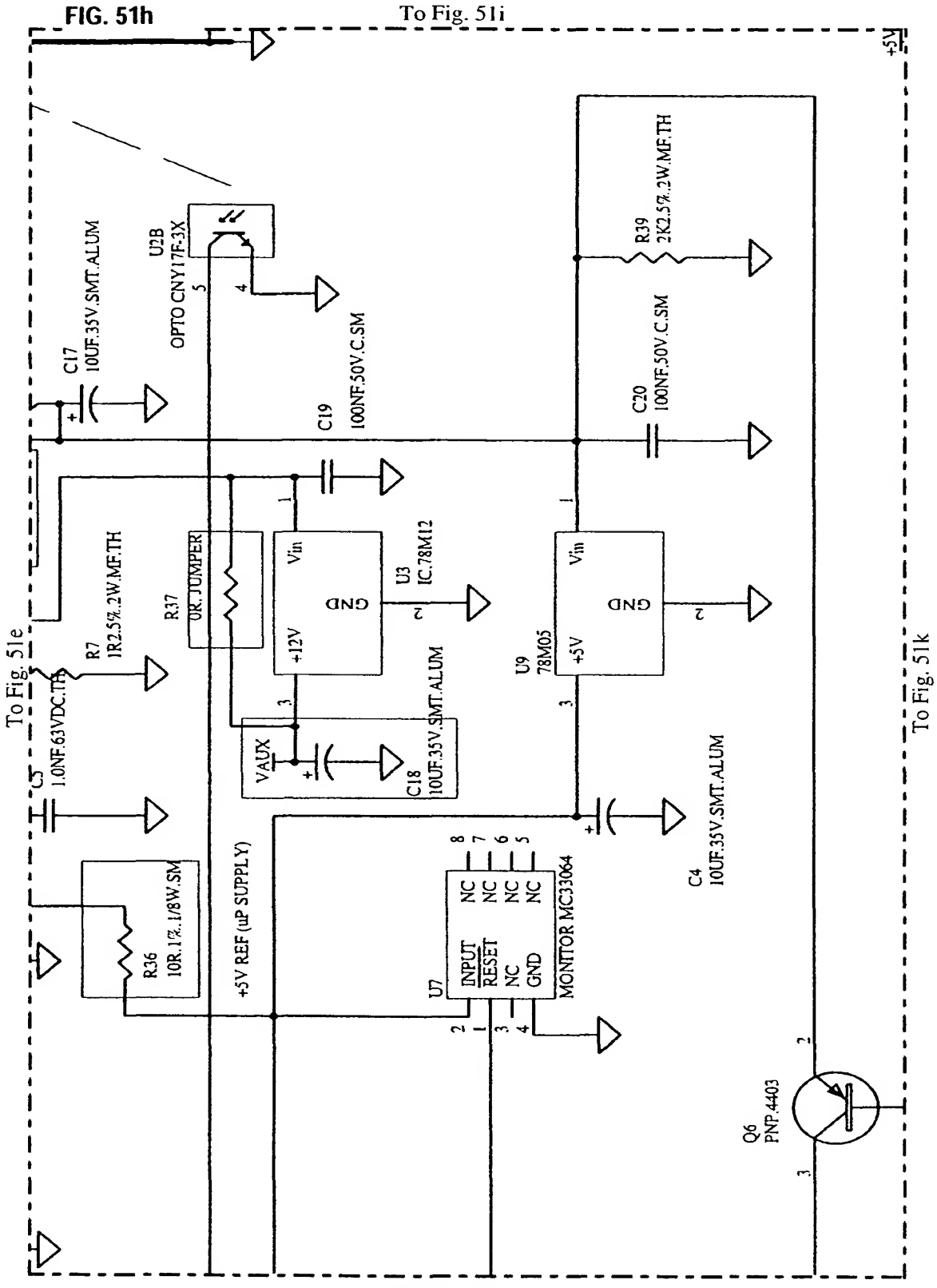
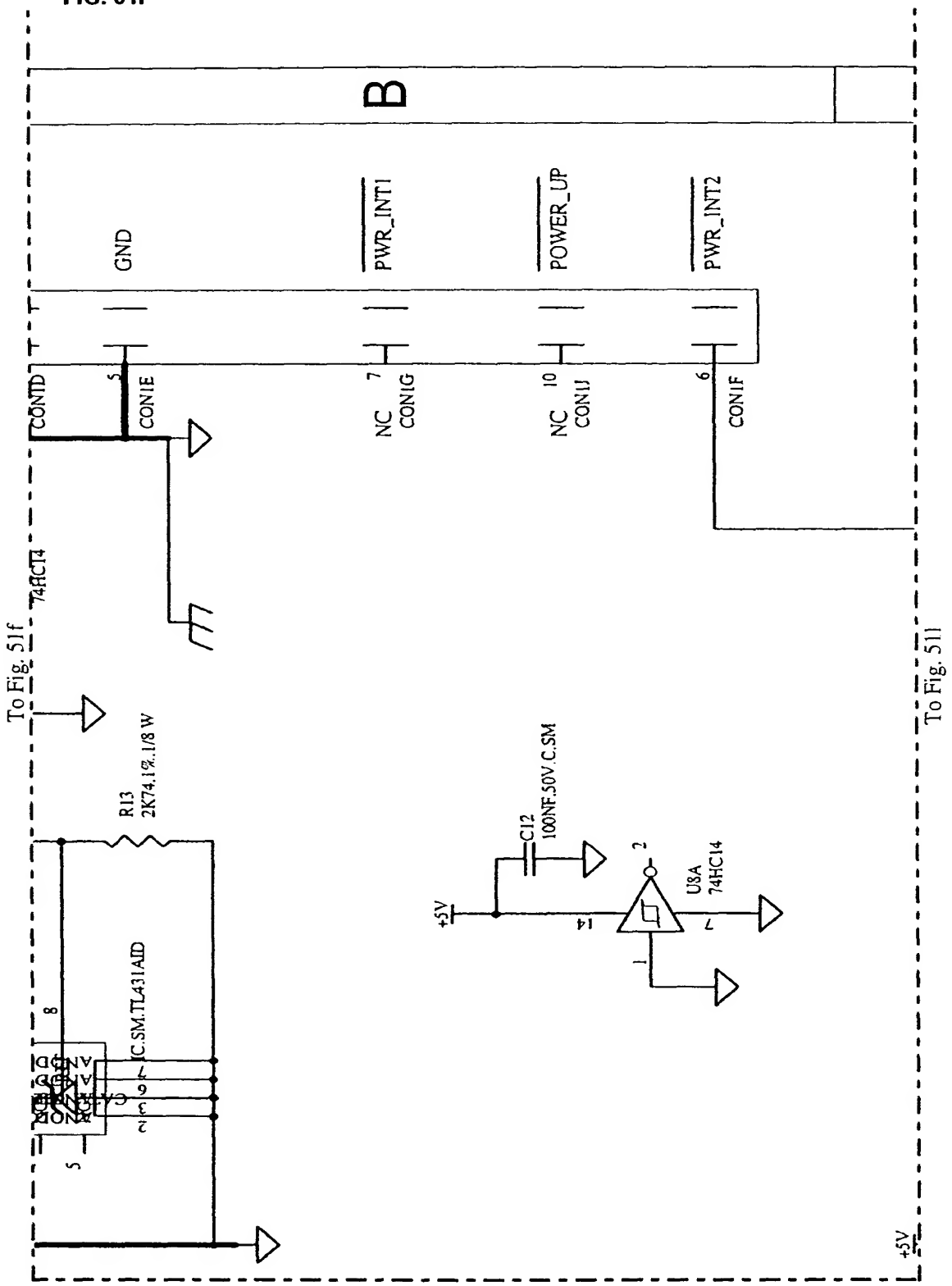

To Fig. 51i
To Fig. 51e
To Fig. 51k
To Fig. 51g
+5V
U2B
OPTO CNY17F-3X
C17
10UF.35V.SMT.ALUM
C19
100NF.50V.C.SM
R39
2K2.5%.2W.MF.TH
C20
100NF.50V.C.SM
R37
0R.JUMPER
R7
1R2.5%.2W.MF.TH
U3
IC.78M12
+12V
GND
Vin
U9
78M05
+5V
VAUX
C18
10UF.35V.SMT.ALUM
C3
1.0NF.63VDC.TH
R36
10R.1%.1/8W.SM
+5V REF (uP SUPPLY)
U7
MONITOR MC33064
INPUT
RESET
NC
GND
C4
10UF.35V.SMT.ALUM
Q6
PNP.4403

FIG. 51i



To Fig. 51h

FIG. 51j

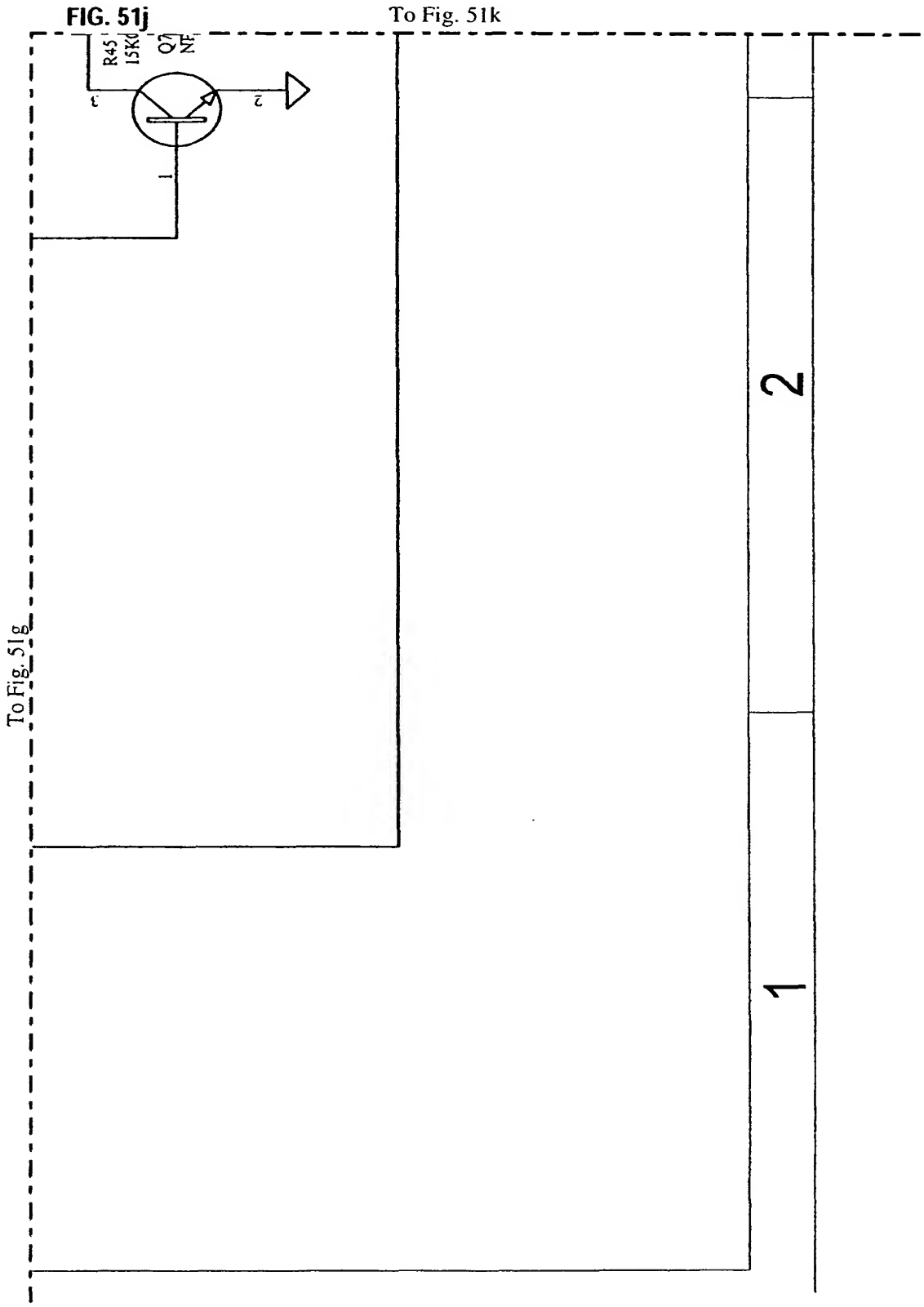


FIG. 51k

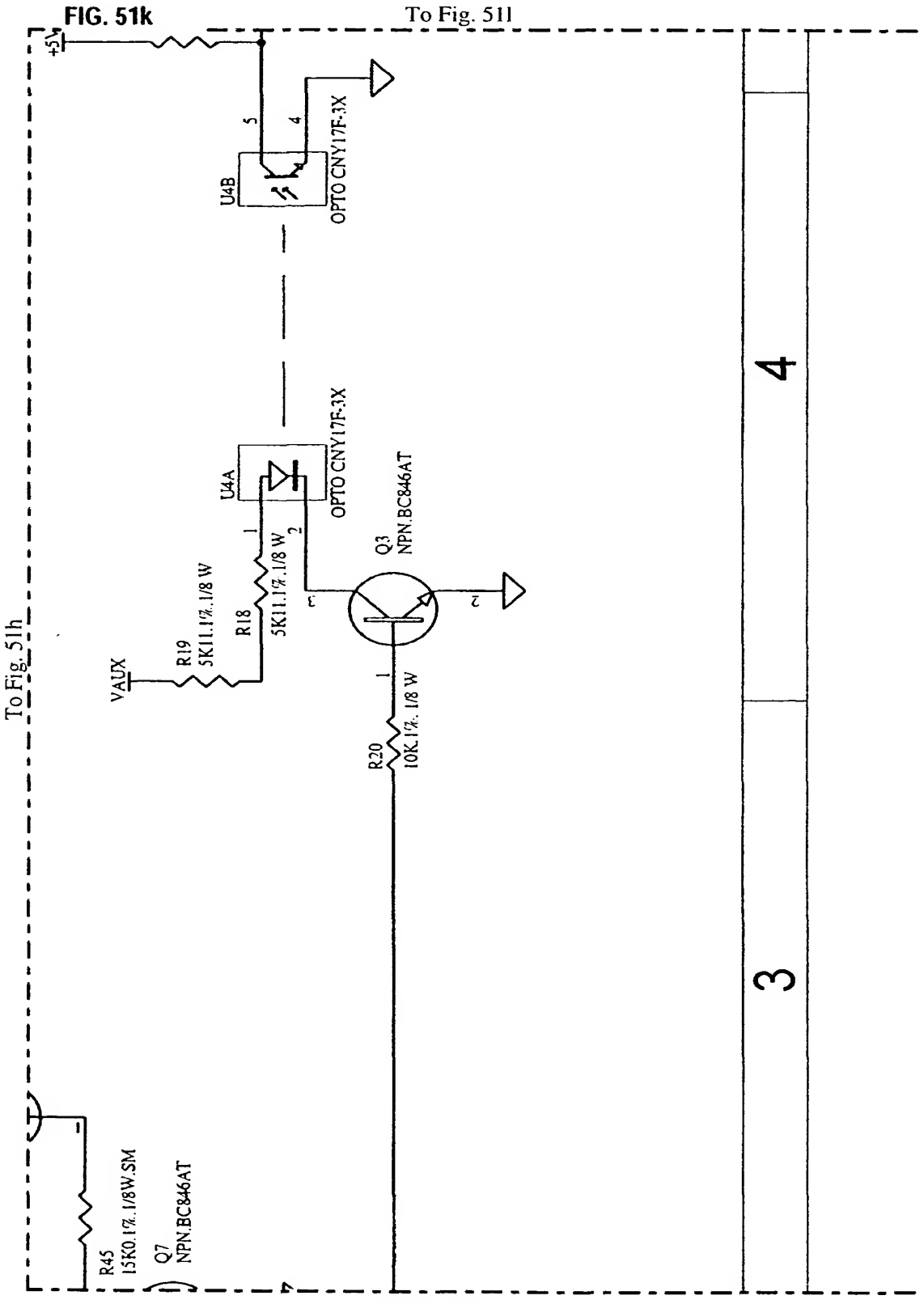

To Fig. 51l
To Fig. 51h
To Fig. 51j
+5V
U4B
OPTO CNY17F-3X
U4A
OPTO CNY17F-3X
Q3
NPN.BC846AT
R18
5K11.1%.1/8 W
R19
5K11.1%.1/8 W
VAUX
R20
10K.1%. 1/8 W
R45
15K0.1%.1/8W.SM
Q7
NPN.BC846AT
4
3

FIG. 51l

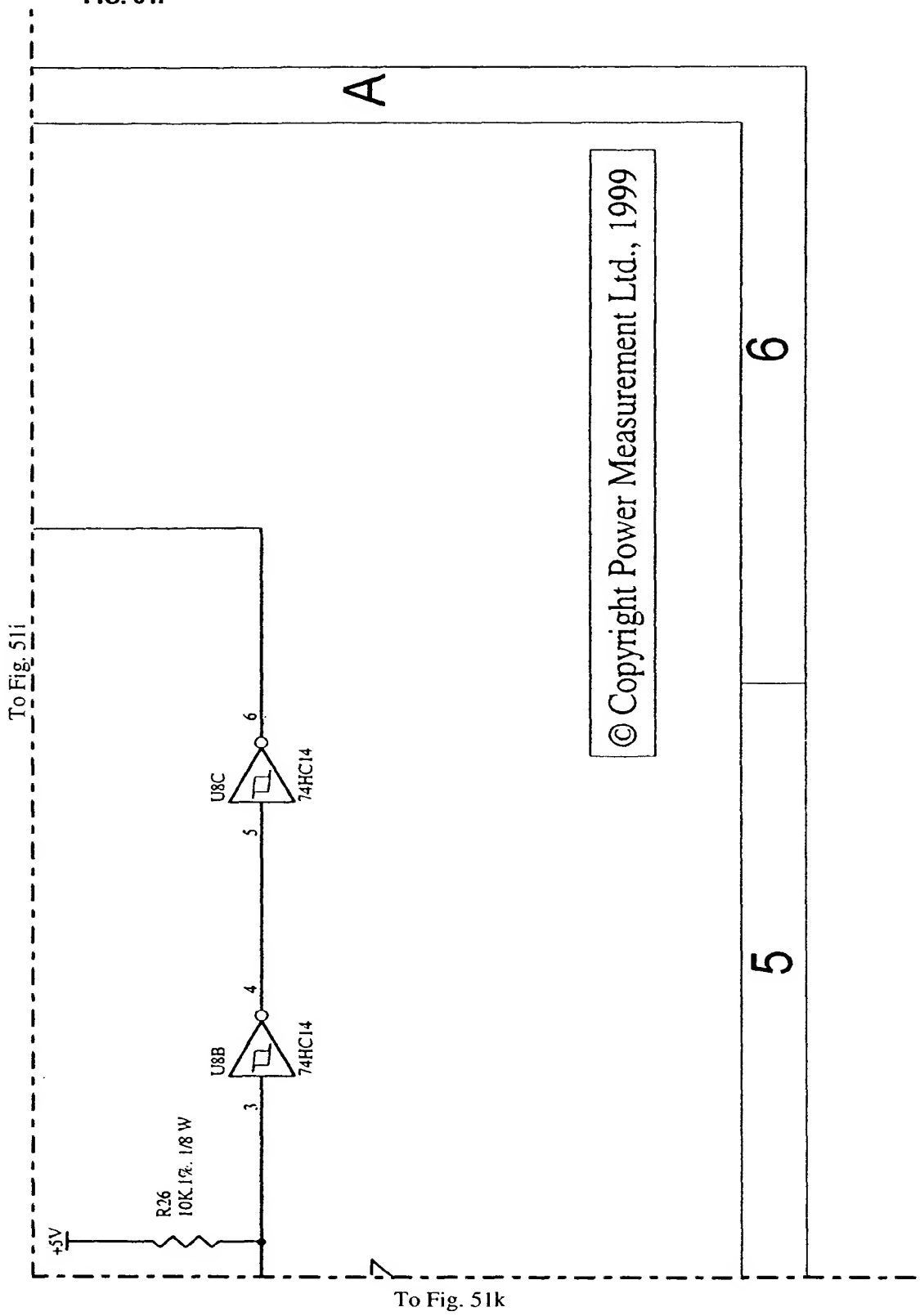

A
6
5
© Copyright Power Measurement Ltd., 1999
To Fig. 51i
U8C
74HC14
U8B
74HC14
R26
10K 1%, 1/8 W
+5V
To Fig. 51k

FIG. 52a

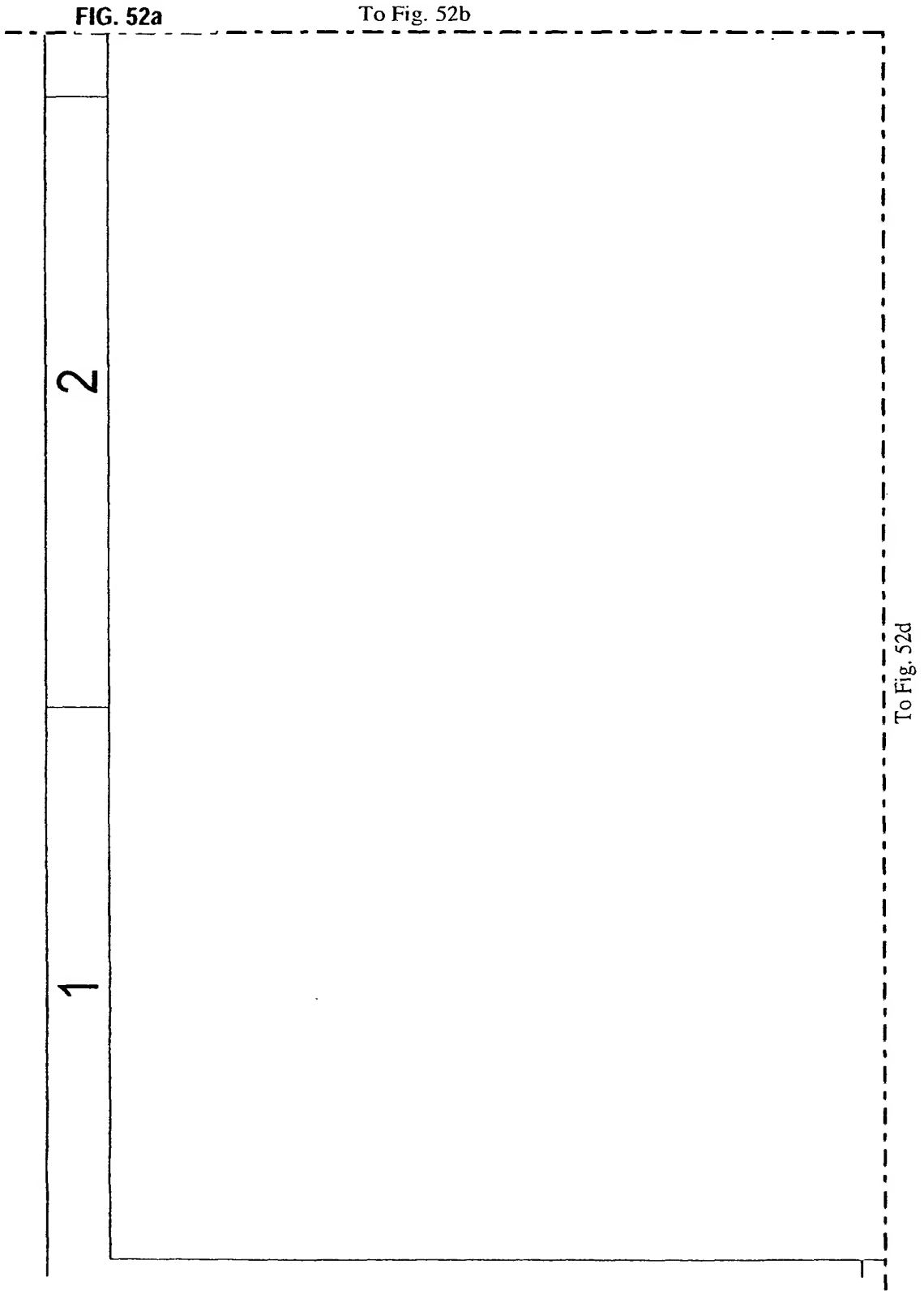


FIG. 52b

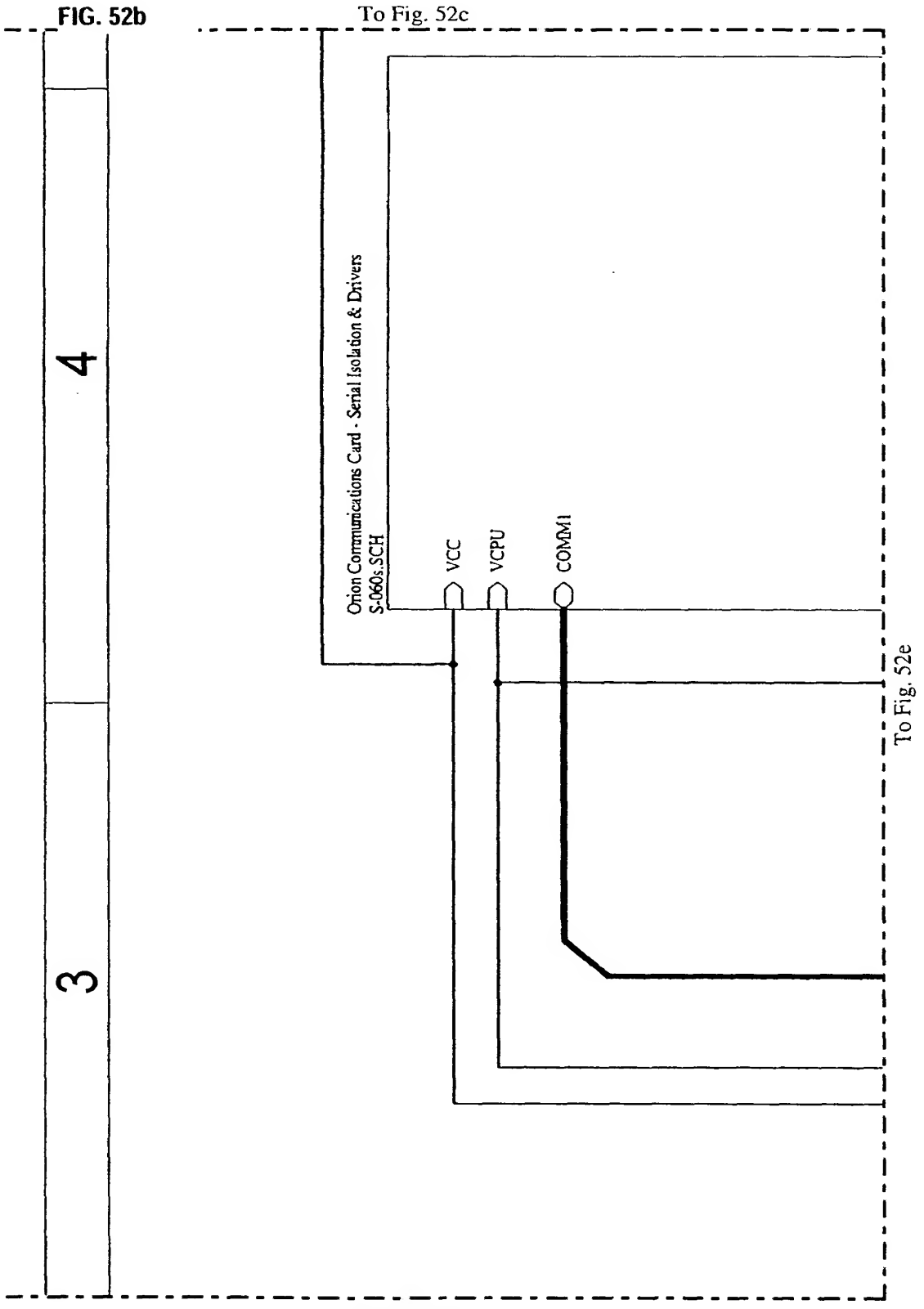

To Fig. 52c
4
3
Orion Communications Card - Serial Isolation & Drivers
S-060s.SCH
VCC
VCPU
COMM1
To Fig. 52e
To Fig. 52a

FIG. 52c

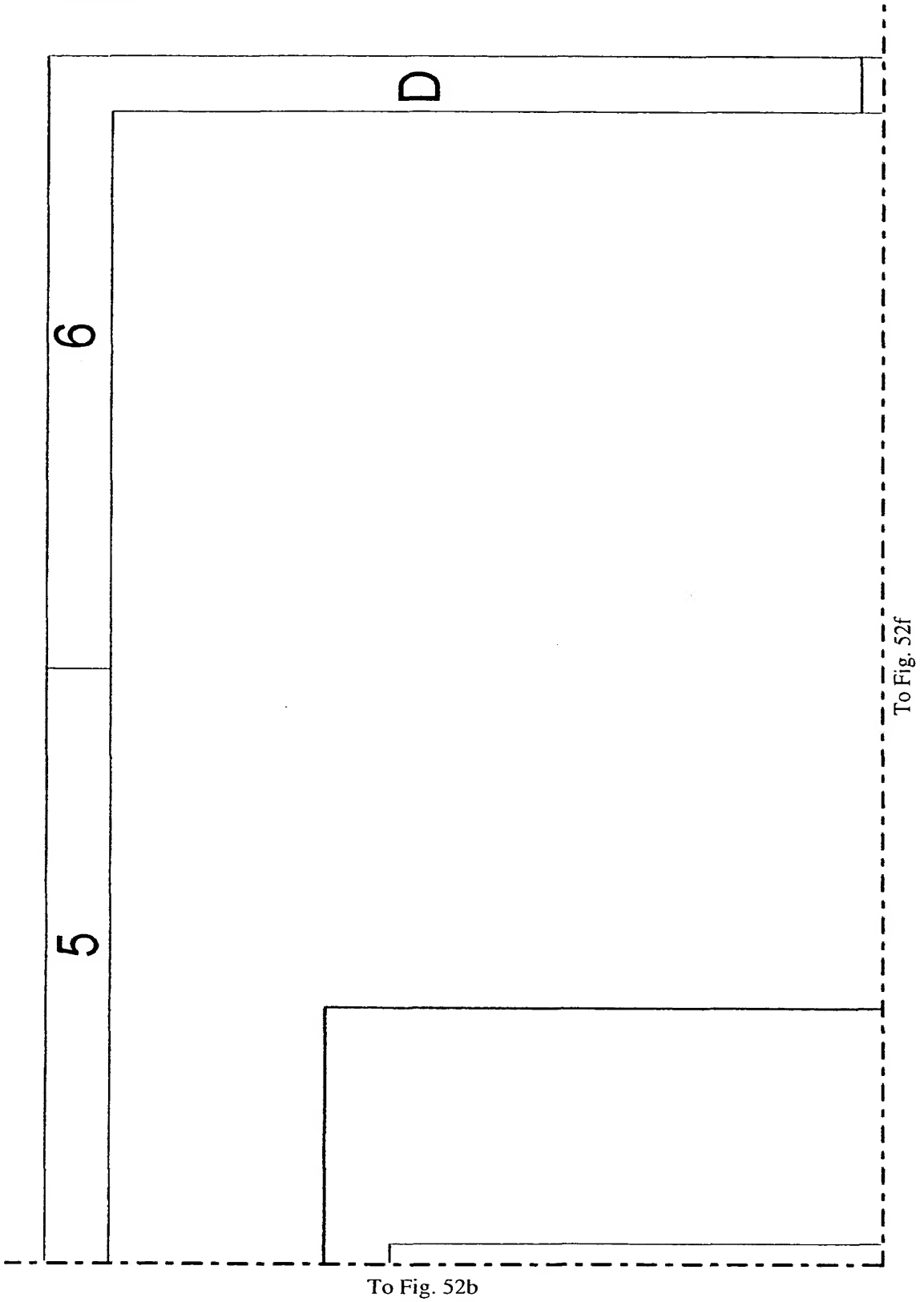


FIG. 52d

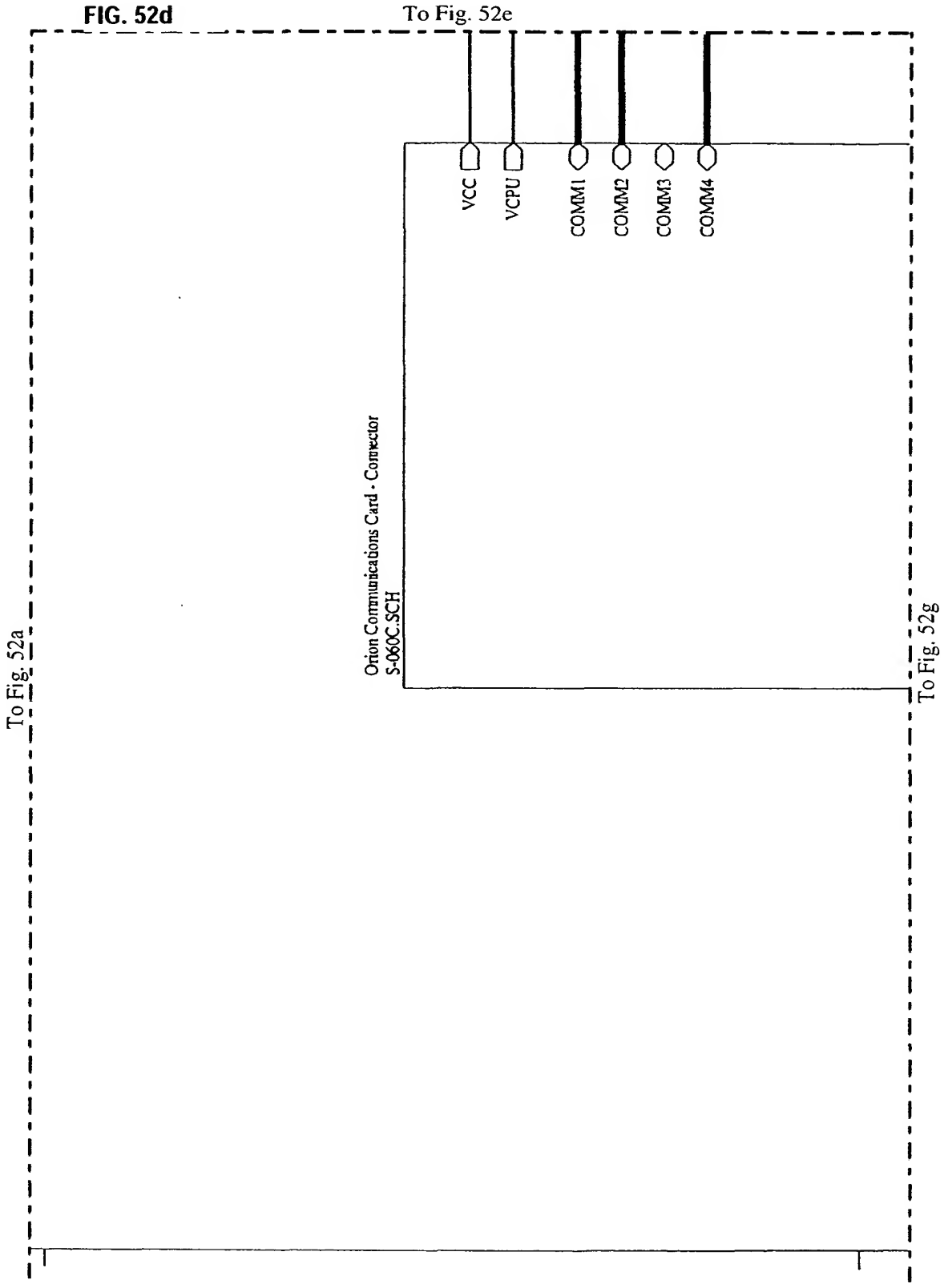

To Fig. 52e
VCC
VCPU
COMM1
COMM2
COMM3
COMM4
Orion Communications Card - Connector
S-060C.SCH
To Fig. 52a
To Fig. 52g

FIG. 52e

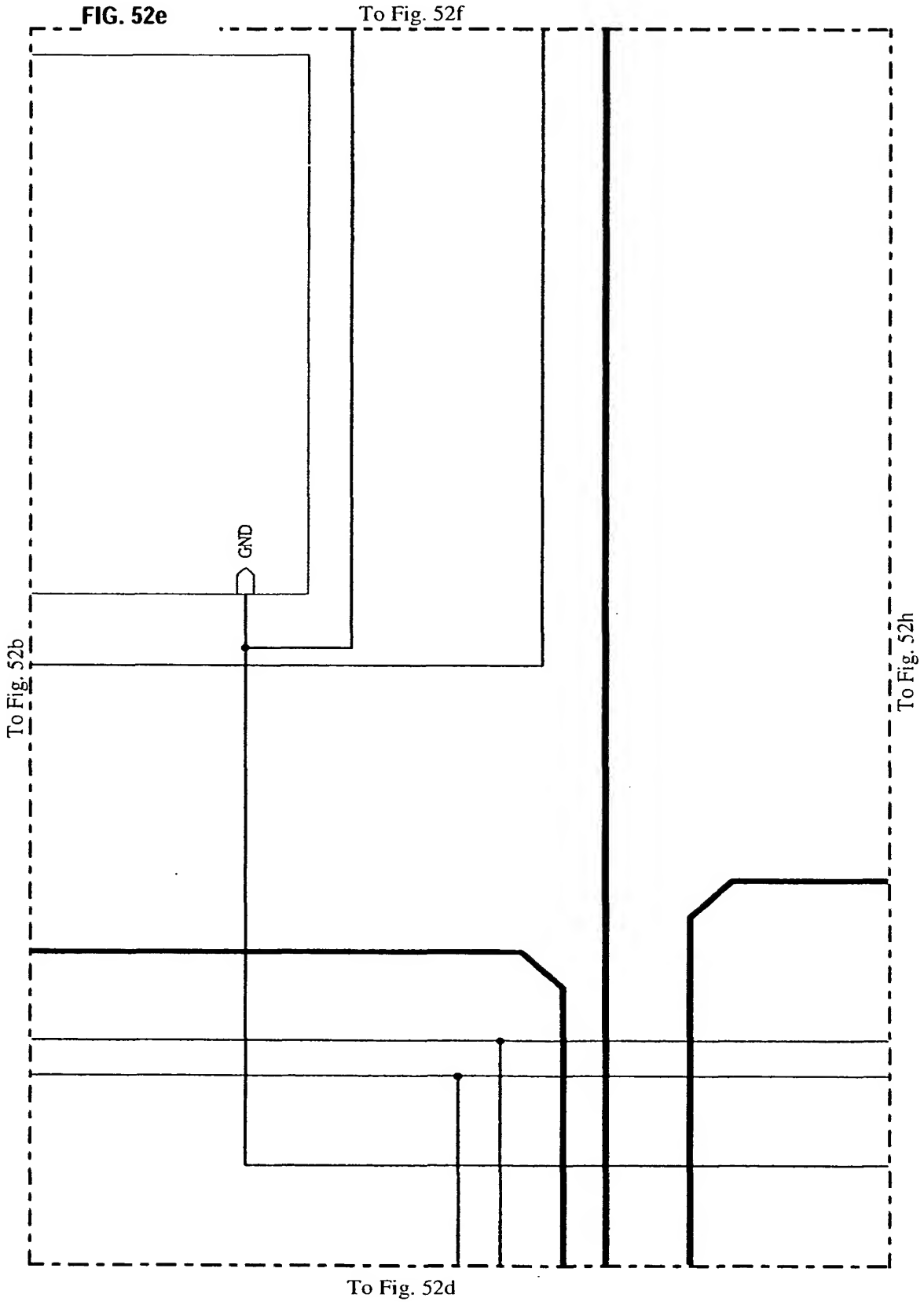


FIG. 52f

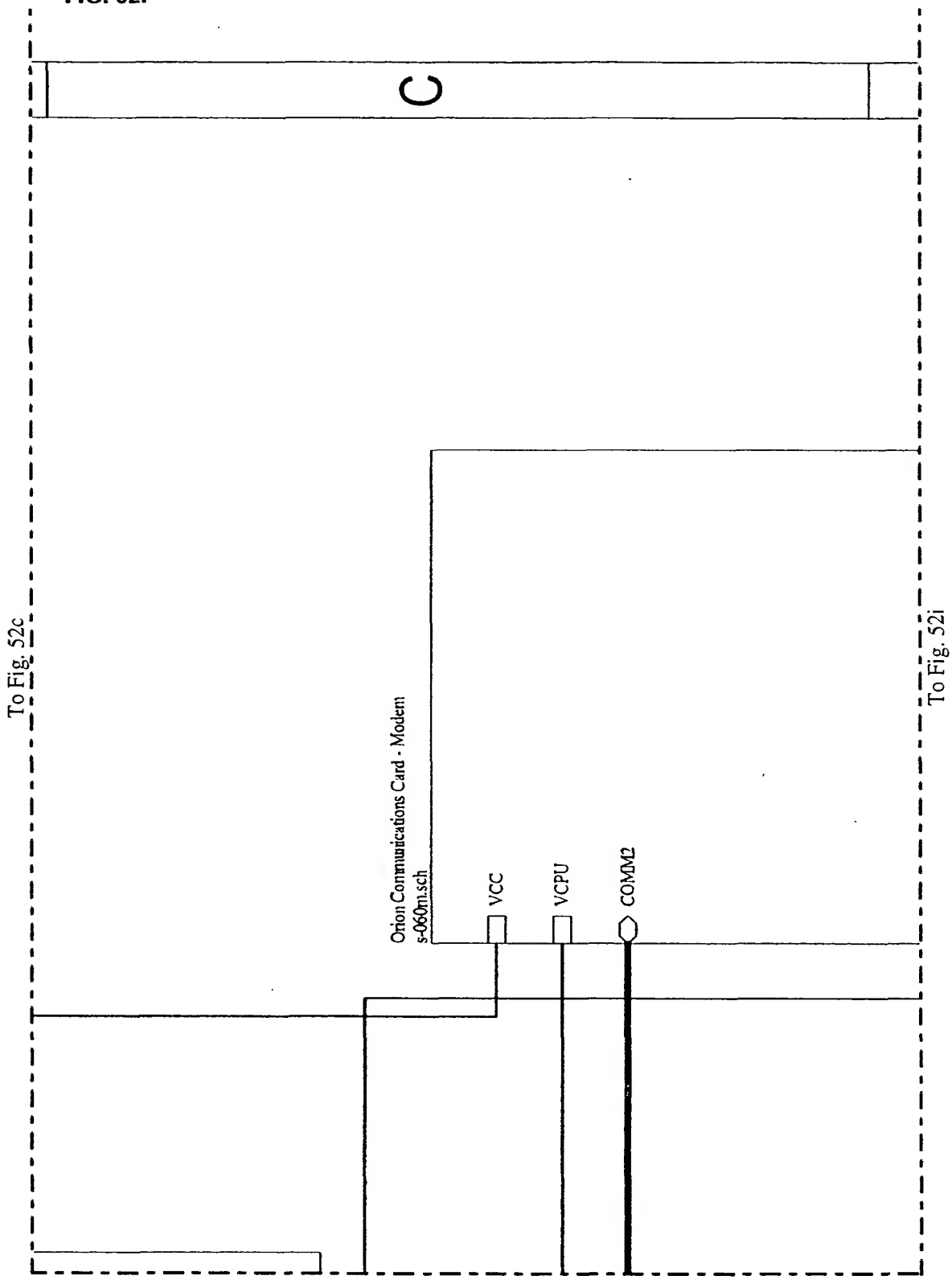

C
To Fig. 52c
To Fig. 52i
Orion Communications Card - Modem
s-060m.sch
VCC
VCPU
COMM2
To Fig. 52e

FIG. 52g

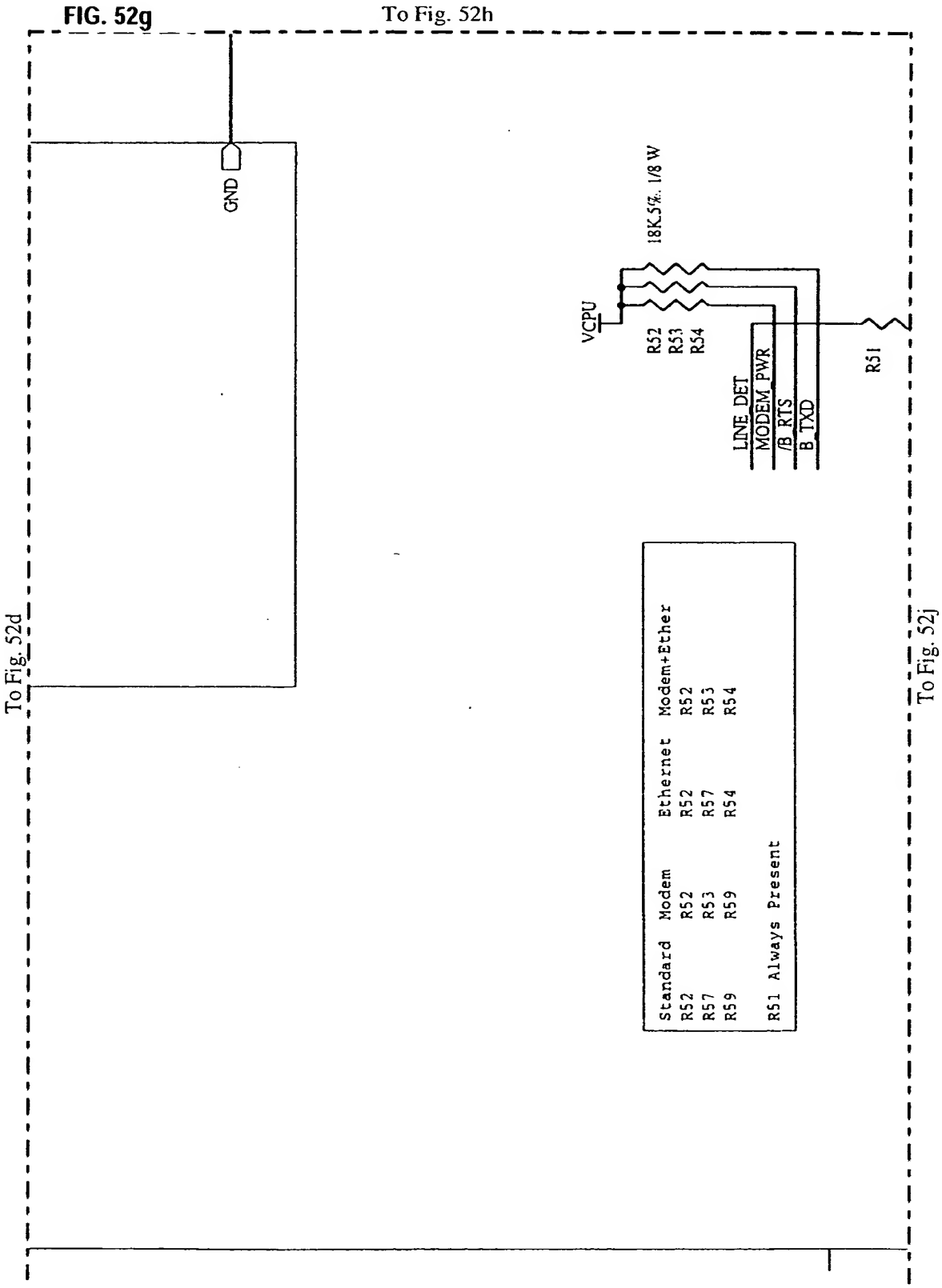

To Fig. 52h
GND
18K,5%, 1/8 W
VCPU
R52
R53
R54
R51
LINE DET
MODEM_PWR
/B_RTS
B_TXD
To Fig. 52d
To Fig. 52j
Standard Modem Ethernet Modem+Ether
R52 R52 R52 R52
R57 R53 R57 R53
R59 R59 R54 R54
R51 Always Present

FIG. 52h

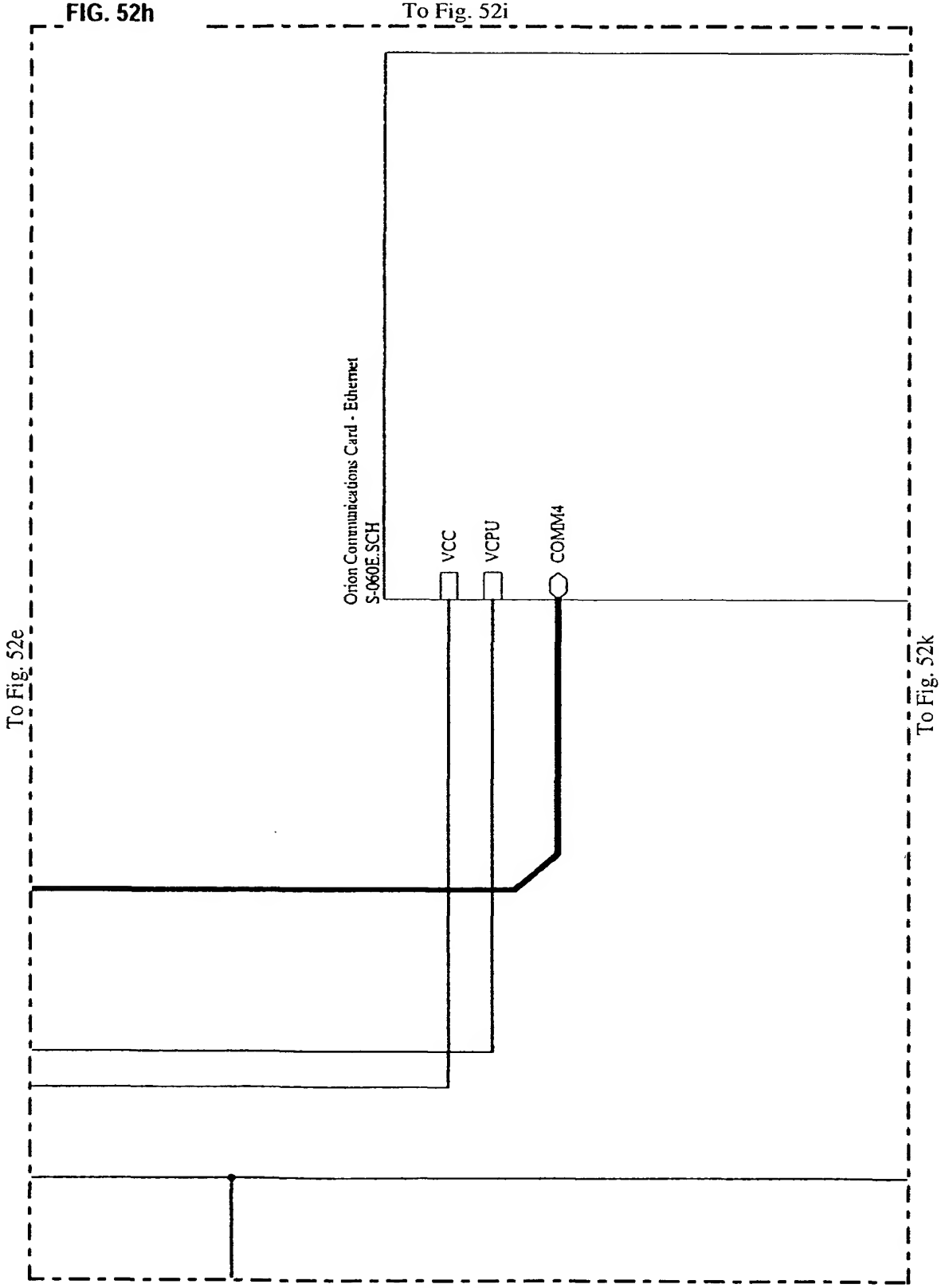

To Fig. 52i
Orion Communications Card - Ethernet
S-060E.SCH
VCC
VCPU
COMM4
To Fig. 52e
To Fig. 52k
To Fig. 52g

FIG. 52i

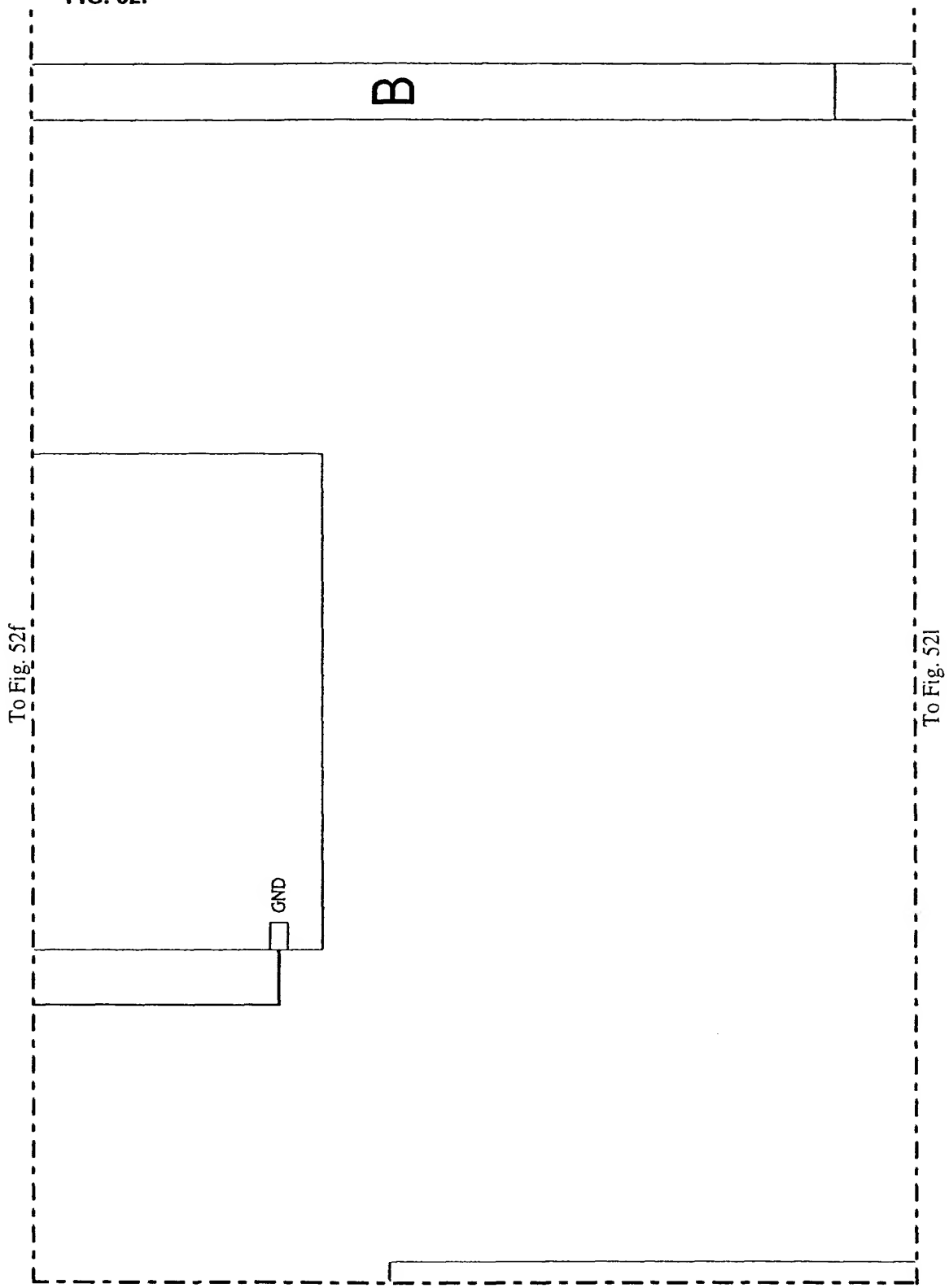


FIG. 52j

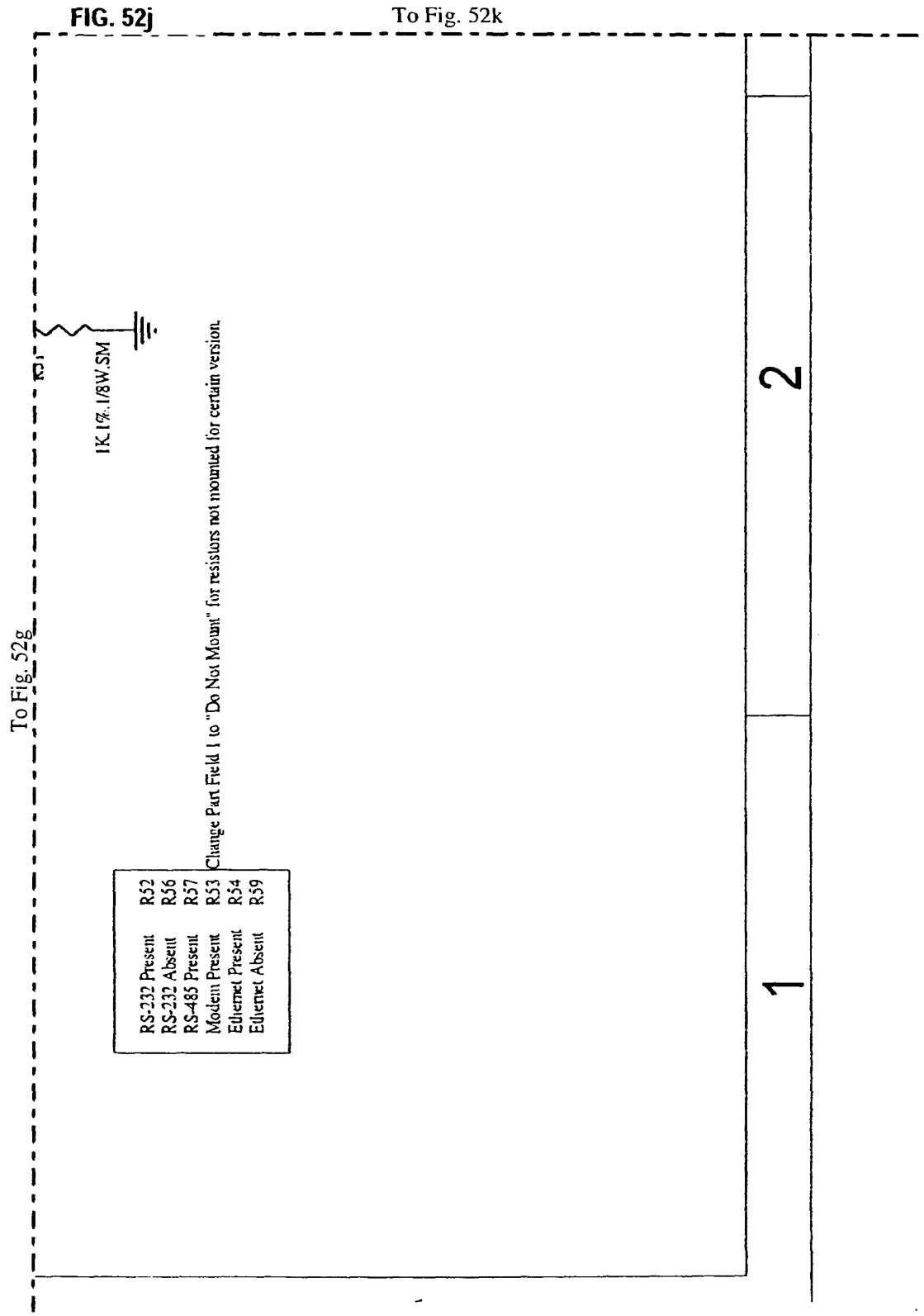

To Fig. 52k
To Fig. 52g
R1
1K.1%.1/8W.SM
Change Part Field 1 to "Do Not Mount" for resistors not mounted for certain version.
RS-232 Present R52
RS-232 Absent R56
RS-485 Present R57
Modem Present R53
Ethernet Present R54
Ethernet Absent R59
2
1

FIG. 52k

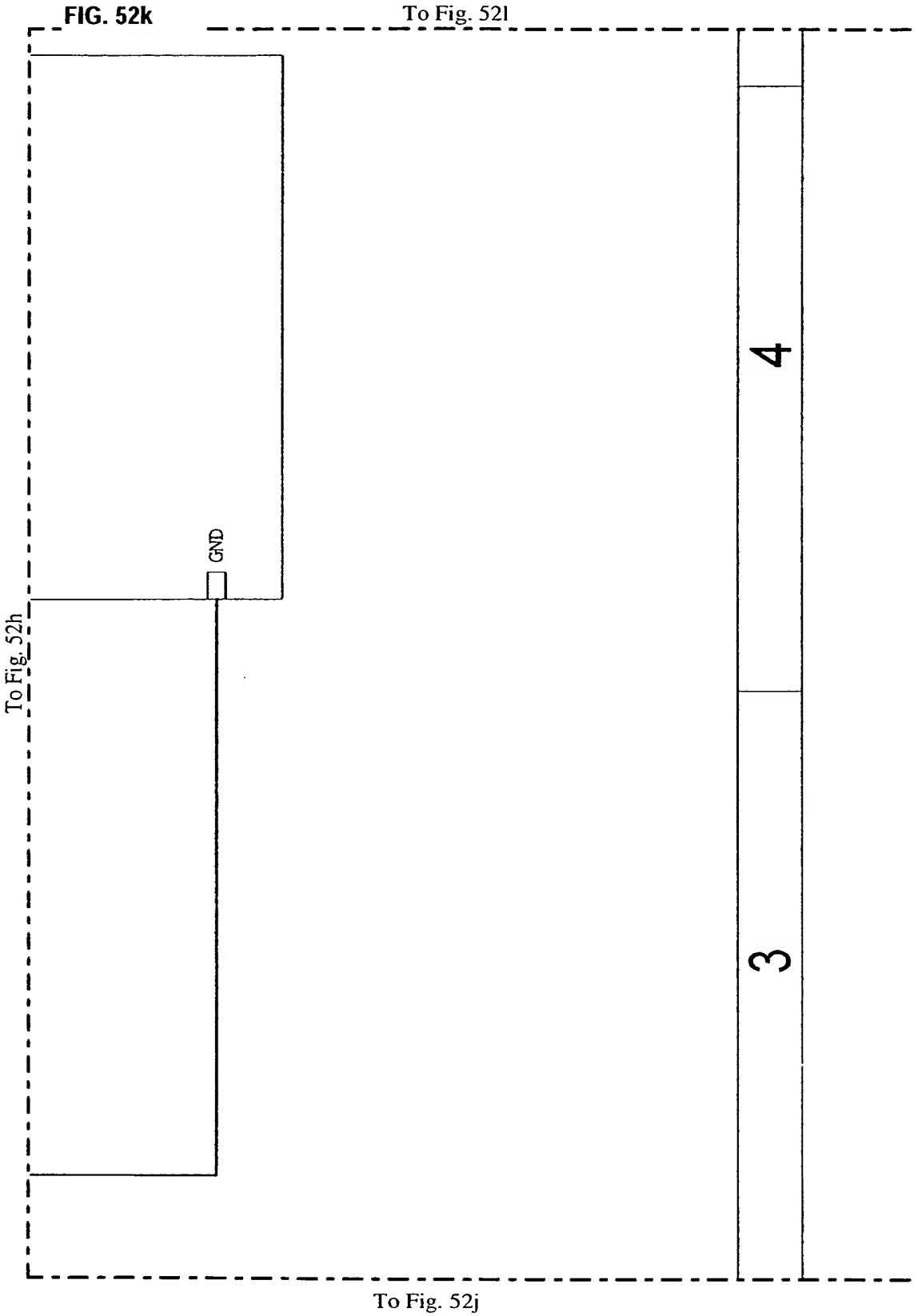


FIG. 52I

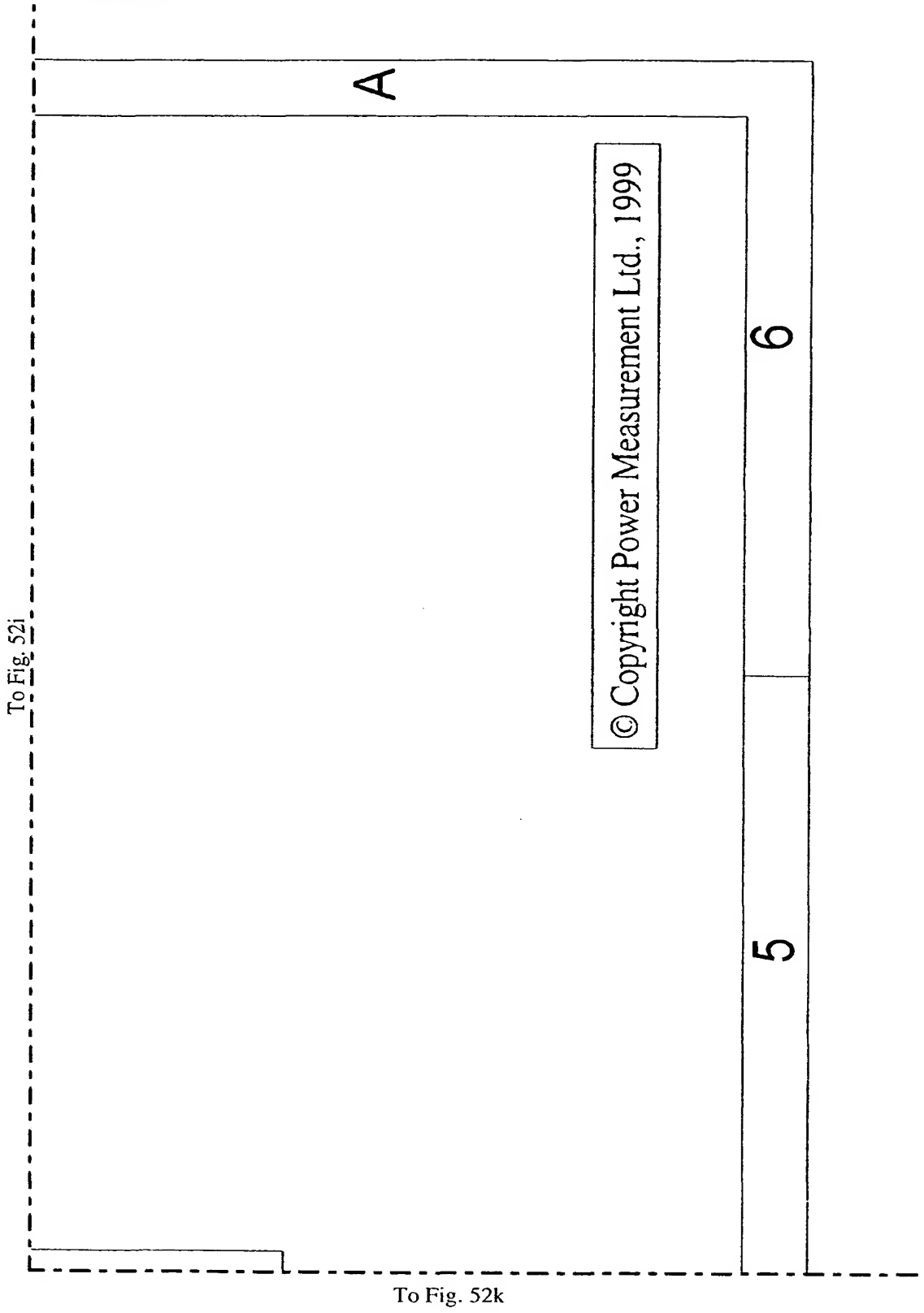

A
6
5
© Copyright Power Measurement Ltd., 1999
To Fig. 52i
To Fig. 52k

FIG. 53a

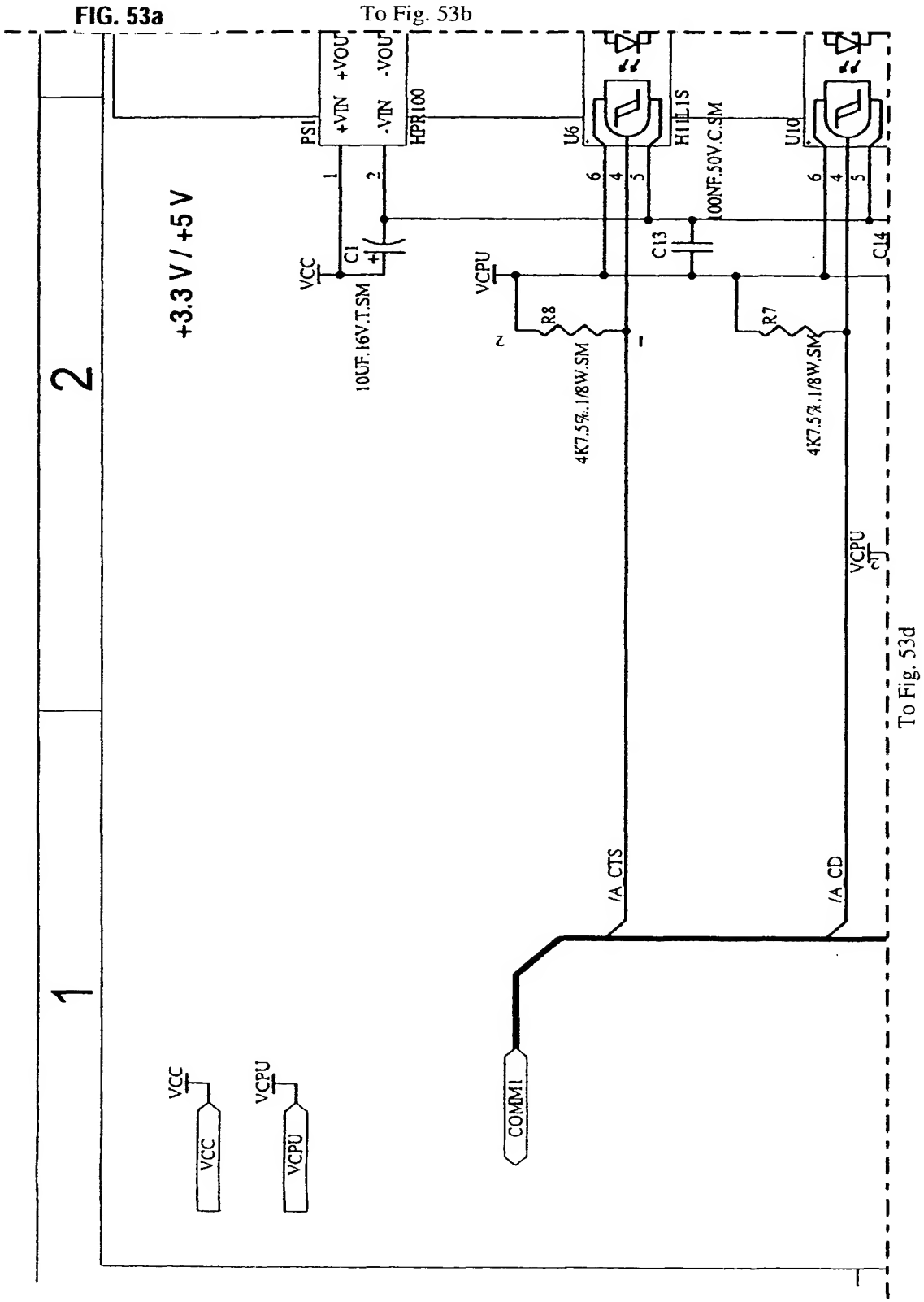

To Fig. 53b
+3.3 V / +5 V
PS1
+VOUT
-VOUT
+VIN
-VIN
HPR100
U6
H11L1S
U10
100NF.50V.C.SM
C1
10UF.16V.T.SM
C13
C14
VCC
VCPU
R8
R7
4K7.5%..1/8W.SM
4K7.5%..1/8W.SM
/A_CTS
/A_CD
COMM1
To Fig. 53d

FIG. 53b

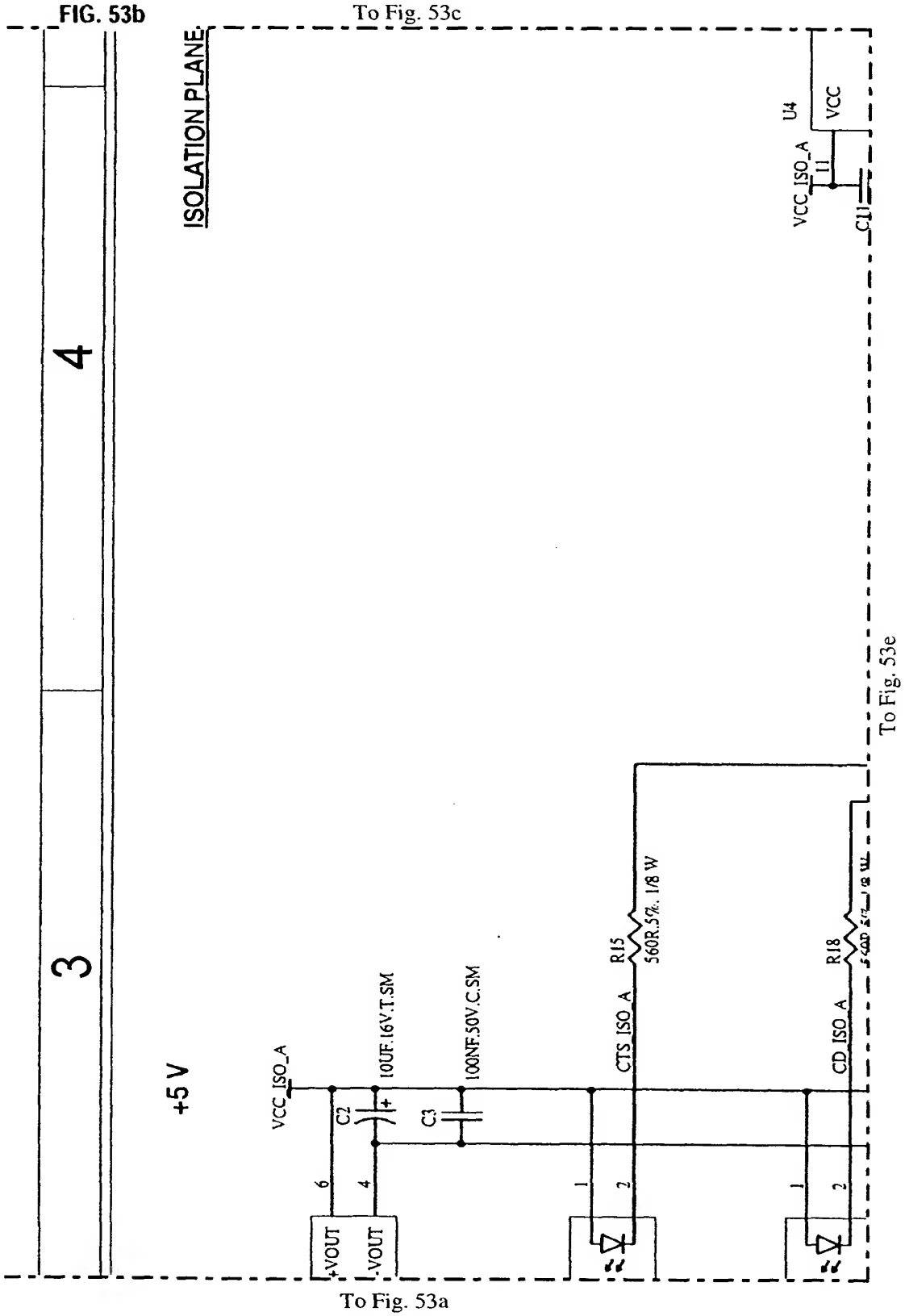
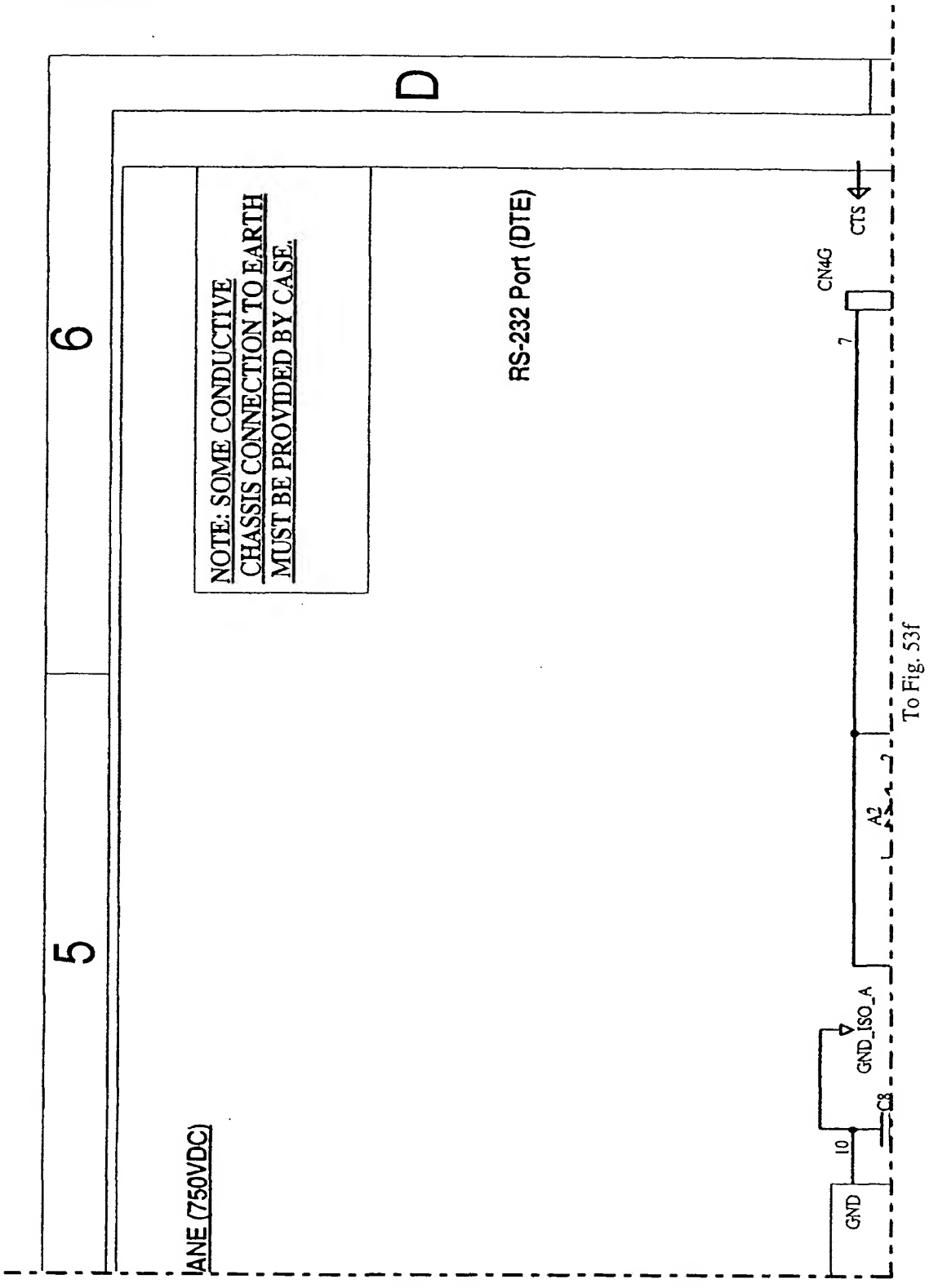

To Fig. 53c
ISOLATION PLANE
4
3
U4
VCC
VCC_ISO_A
L1
C11
+5 V
VCC_ISO_A
C2
10UF.16V.T.SM
C3
100NF.50V.C.SM
R15
560R.5%. 1/8 W
CTS_ISO_A
R18
CD_ISO_A
6
4
1
2
+VOUT
-VOUT
To Fig. 53e
To Fig. 53a

FIG. 53c



To Fig. 53b

FIG. 53d

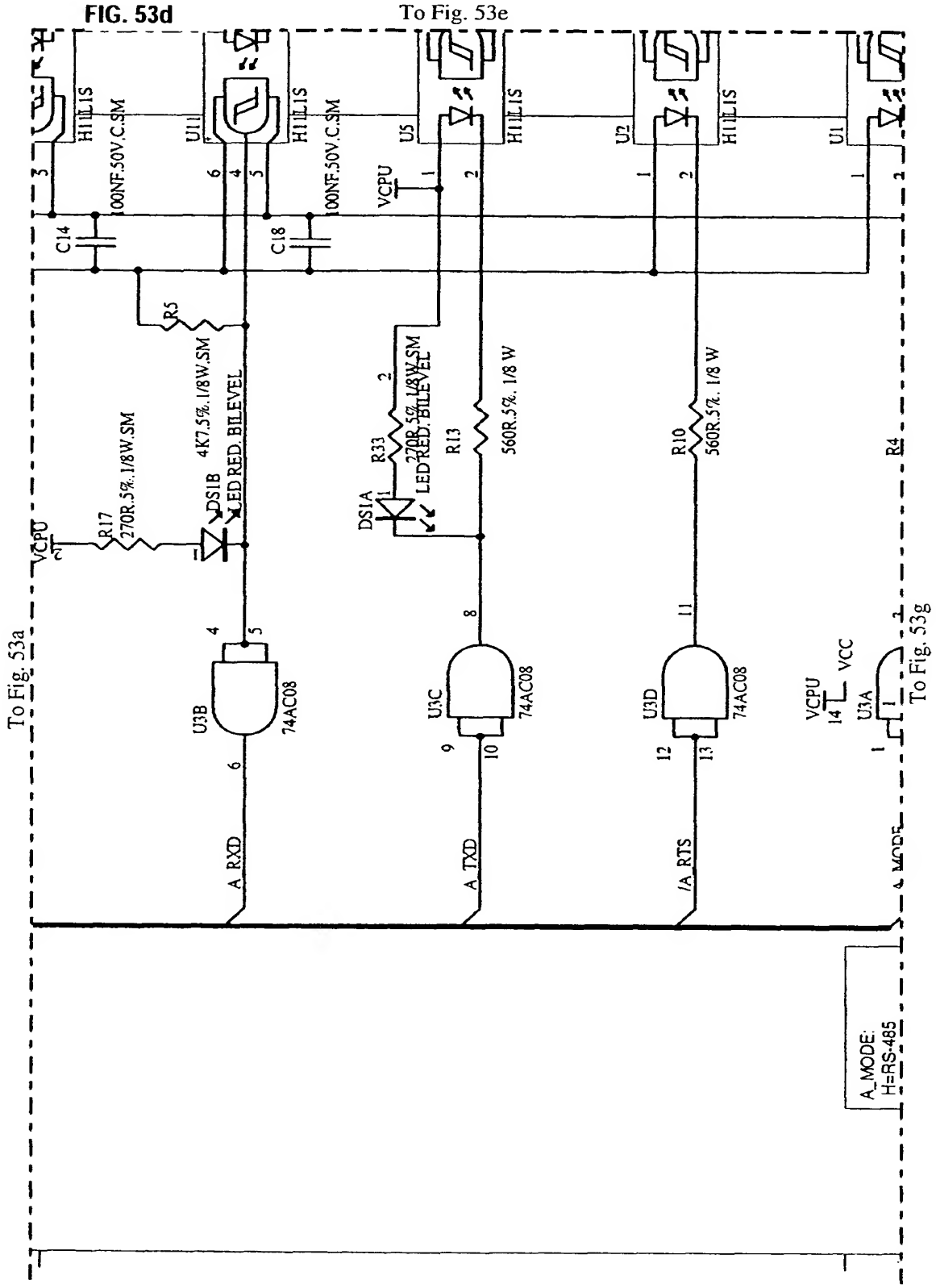

To Fig. 53e
To Fig. 53a
To Fig. 53g
H11L1S
100NF.50V.C.SM
U11
U5
U2
U1
VCPU
C14
C18
R5
4K7.5%.1/8W.SM
DS1B
LED RED. BILEVEL
R17
270R.5%.1/8W.SM
R33
270R.5%.1/8W.SM
DS1A
LED RED. BILEVEL
R13
560R.5%. 1/8 W
R10
560R.5%. 1/8 W
R4
U3B
U3C
U3D
U3A
74AC08
VCC
A_RXD
A_TXD
/A_RTS
A_MODE:
H=RS-485

FIG. 53e

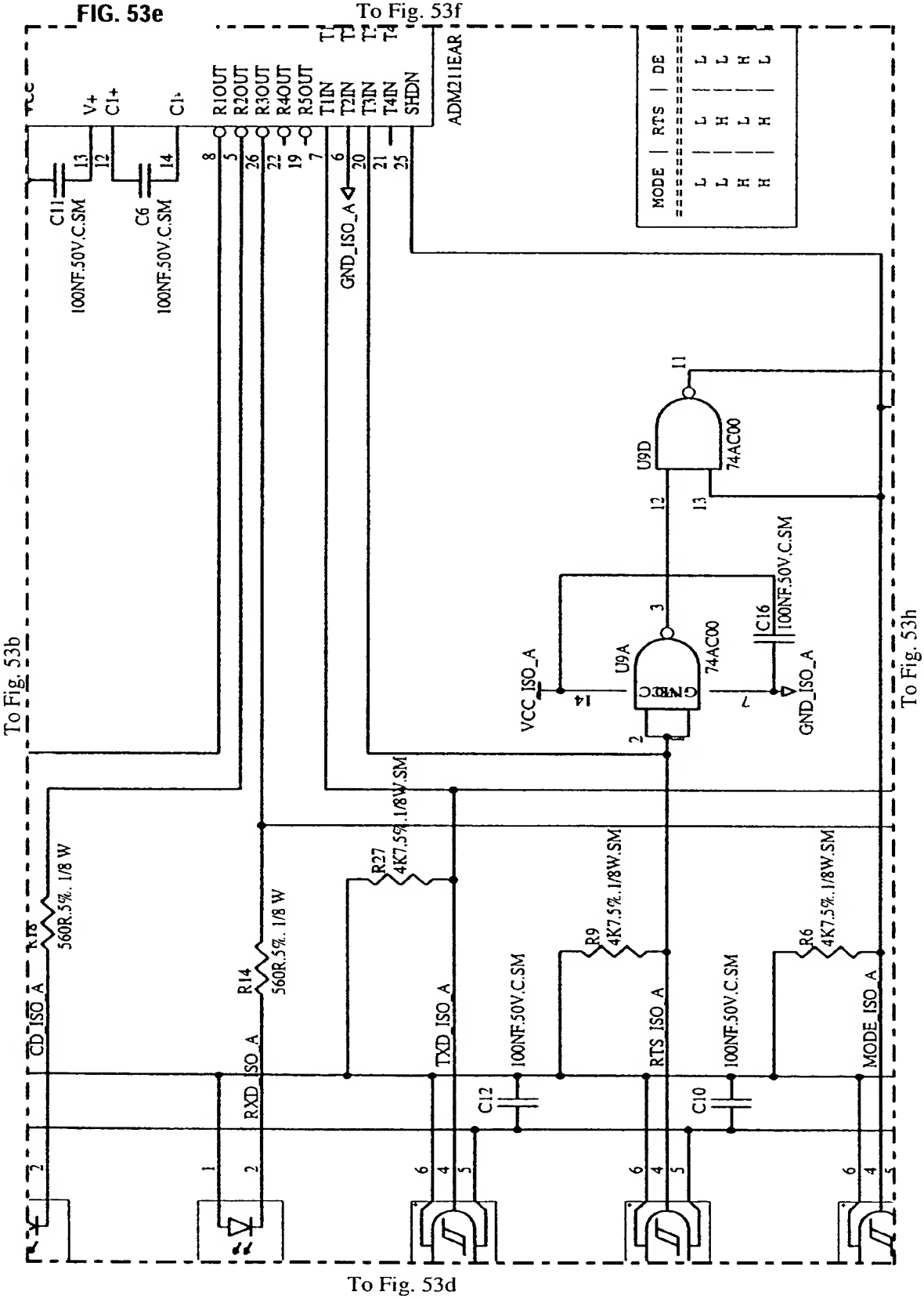

To Fig. 53f
To Fig. 53b
To Fig. 53h
To Fig. 53d
ADM211EAR
V+
C1+
C1-
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
T1IN
T2IN
T3IN
T4IN
SHDN
GND_ISO_A
C11
100NF.50V.C.SM
C6
100NF.50V.C.SM
MODE | RTS | DE
U9D
74AC00
U9A
74AC00
VCC_ISO_A
GND_ISO_A
C16
100NF.50V.C.SM
R27
4K7.5%.1/8W.SM
R9
4K7.5%.1/8W.SM
R6
4K7.5%.1/8W.SM
R18
560R.5%.1/8 W
R14
560R.5%.1/8 W
CD_ISO_A
RXD_ISO_A
TXD_ISO_A
RTS_ISO_A
MODE_ISO_A
C12
100NF.50V.C.SM
C10
100NF.50V.C.SM

FIG. 53f

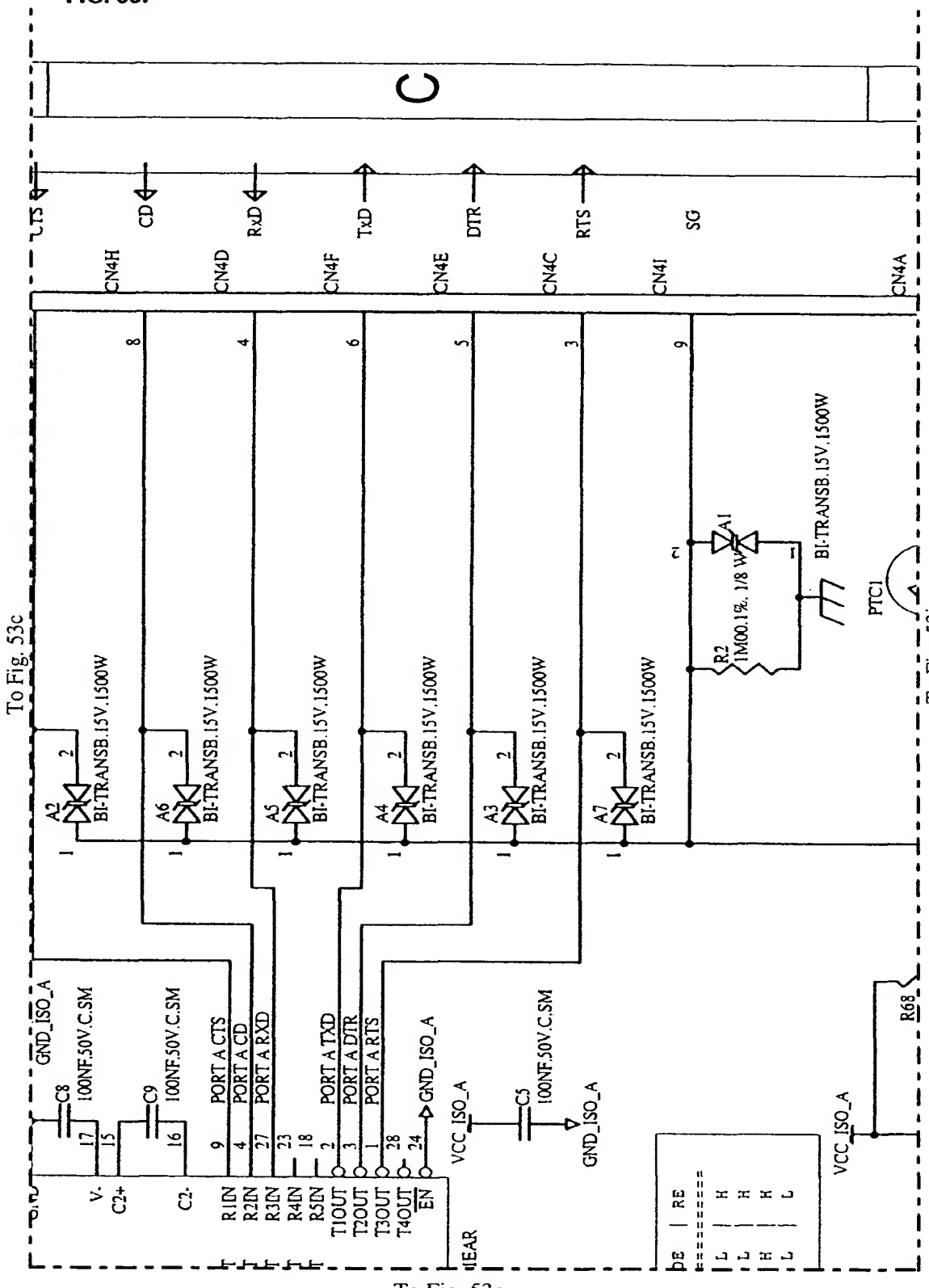

To Fig. 53c
To Fig. 53i
To Fig. 53e
CD
RxD
TxD
DTR
RTS
SG
CN4H
CN4D
CN4F
CN4E
CN4C
CN4I
CN4A
BI-TRANSB.15V.1500W
A1
A2
A3
A4
A5
A6
A7
R2
1M00.1%. 1/8 W
PTC1
R68
C8
C9
C5
100NF.50V.C.SM
GND_ISO_A
VCC_ISO_A
PORT A CTS
PORT A CD
PORT A RXD
PORT A TXD
PORT A DTR
PORT A RTS
V-
C2+
C2-
R1IN
R2IN
R3IN
R4IN
R5IN
T1OUT
T2OUT
T3OUT
T4OUT
EN
EAR

FIG. 53g

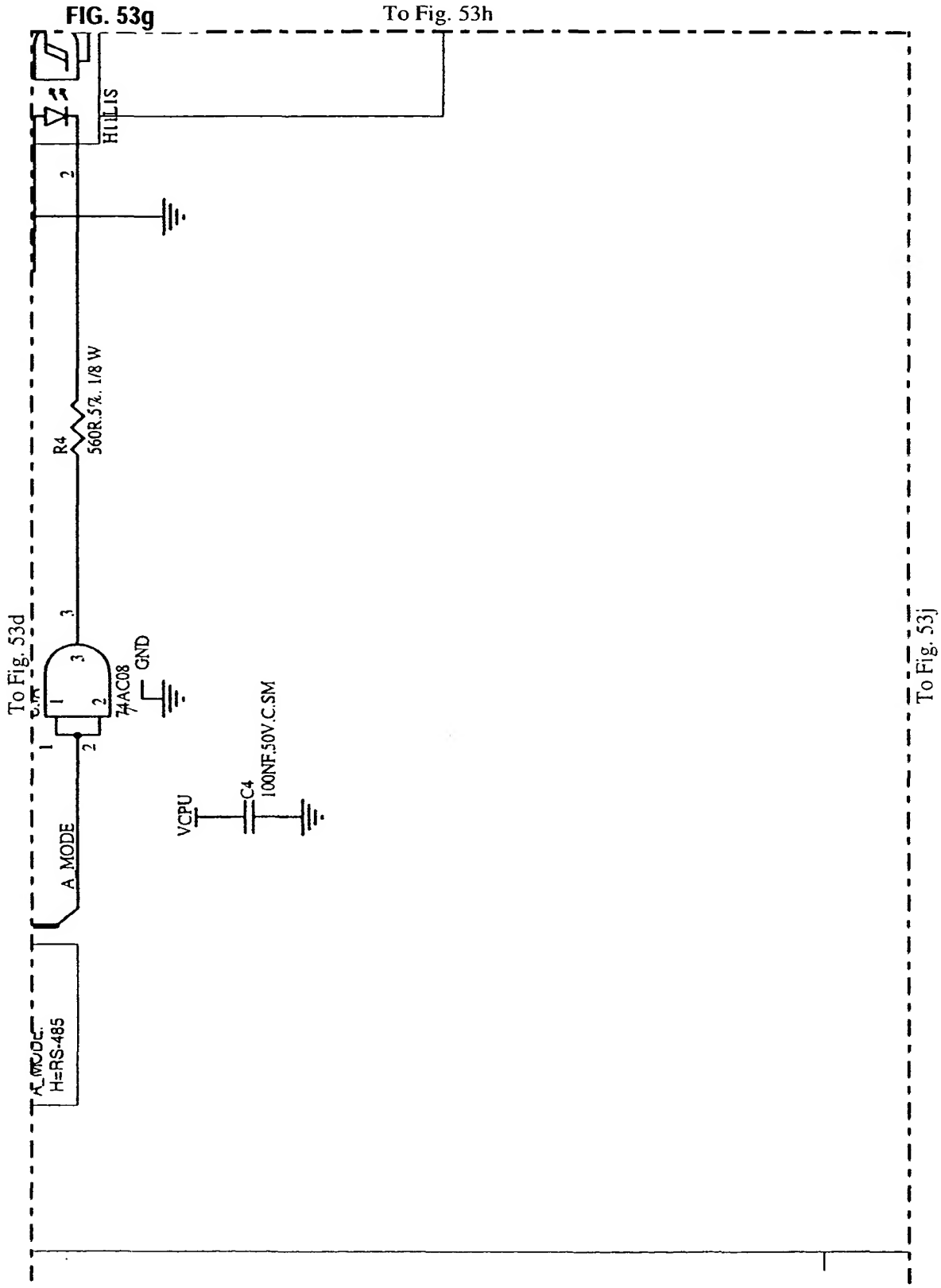

To Fig. 53h
H1LLIS
2
R4
560R.5%. 1/8 W
3
3
74AC08
GND
To Fig. 53d
1
2
A_MODE
VCPU
C4
100NF.50V.C.SM
A_MODE
H=RS-485
To Fig. 53j

FIG. 53h

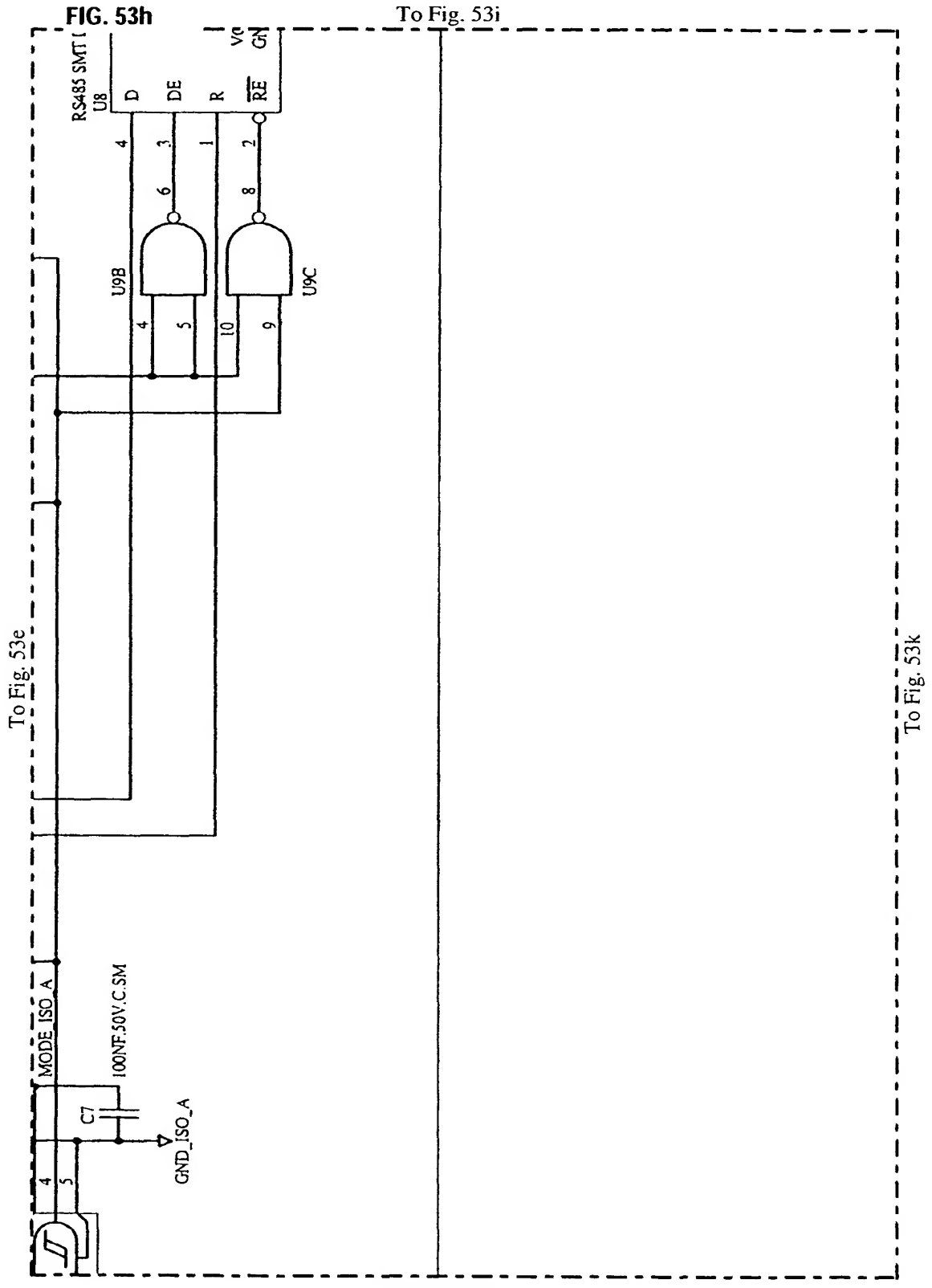

To Fig. 53i
To Fig. 53e
To Fig. 53k
To Fig. 53g
RS485 SMT
U8
D
DE
R
RE
U9B
U9C
MODE_ISO_A
100NF.50V.C.SM
C7
GND_ISO_A

FIG. 53i

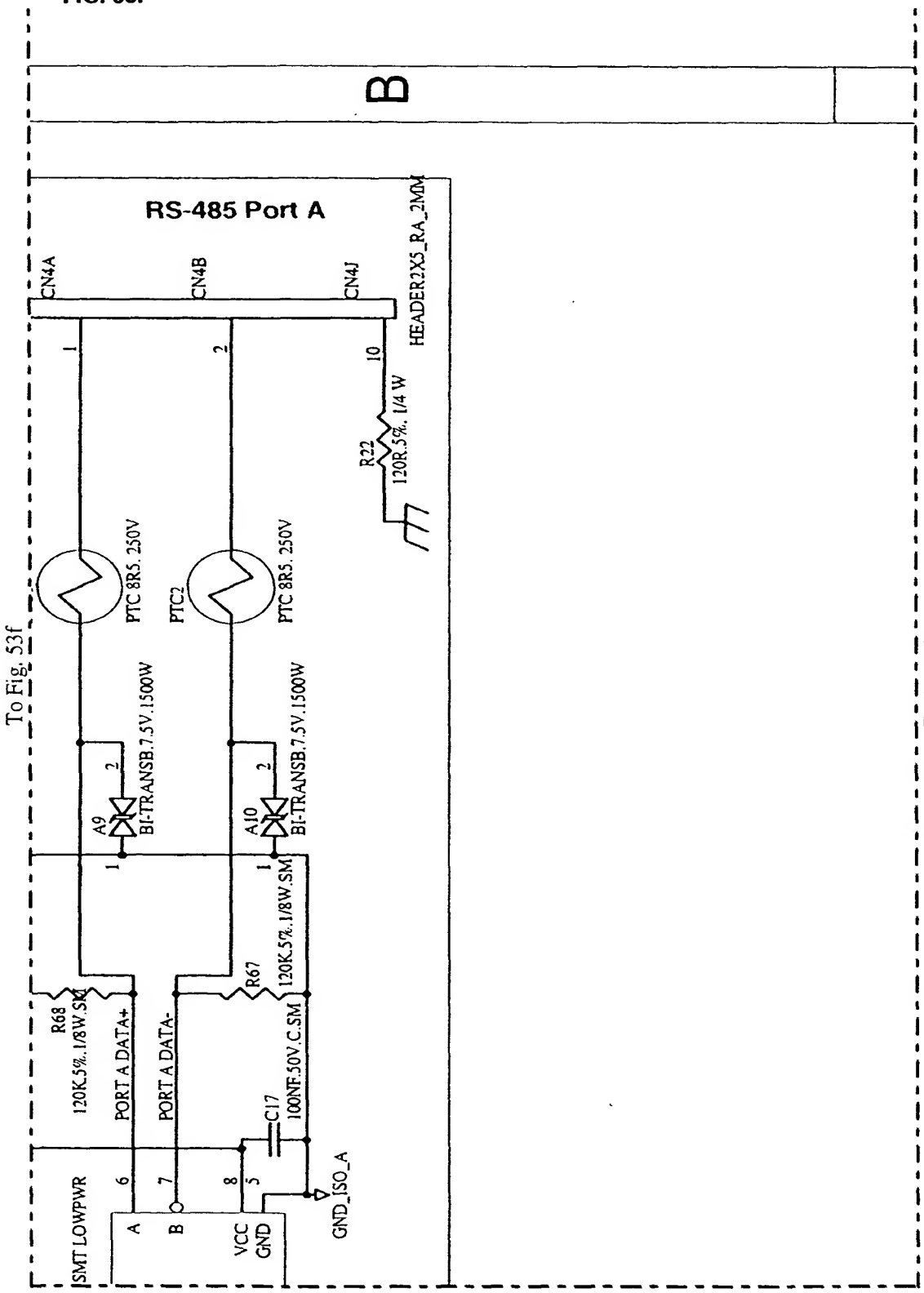

B
RS-485 Port A
CN4A
CN4B
CN4J
HEADER2X5_RA_2MM
R22
120R.5%. 1/4 W
PTC1
PTC 8R5. 250V
PTC2
PTC 8R5. 250V
A9
BI-TRANSB.7.5V.1500W
A10
BI-TRANSB.7.5V.1500W
R68
120K.5%.1/8W.SM
R67
120K.5%.1/8W.SM
PORT A DATA+
PORT A DATA-
C17
100NF.50V.C.SM
SMT LOWPWR
A
B
VCC
GND
GND_ISO_A
To Fig. 53f
To Fig. 53l
To Fig. 53h

FIG. 53j

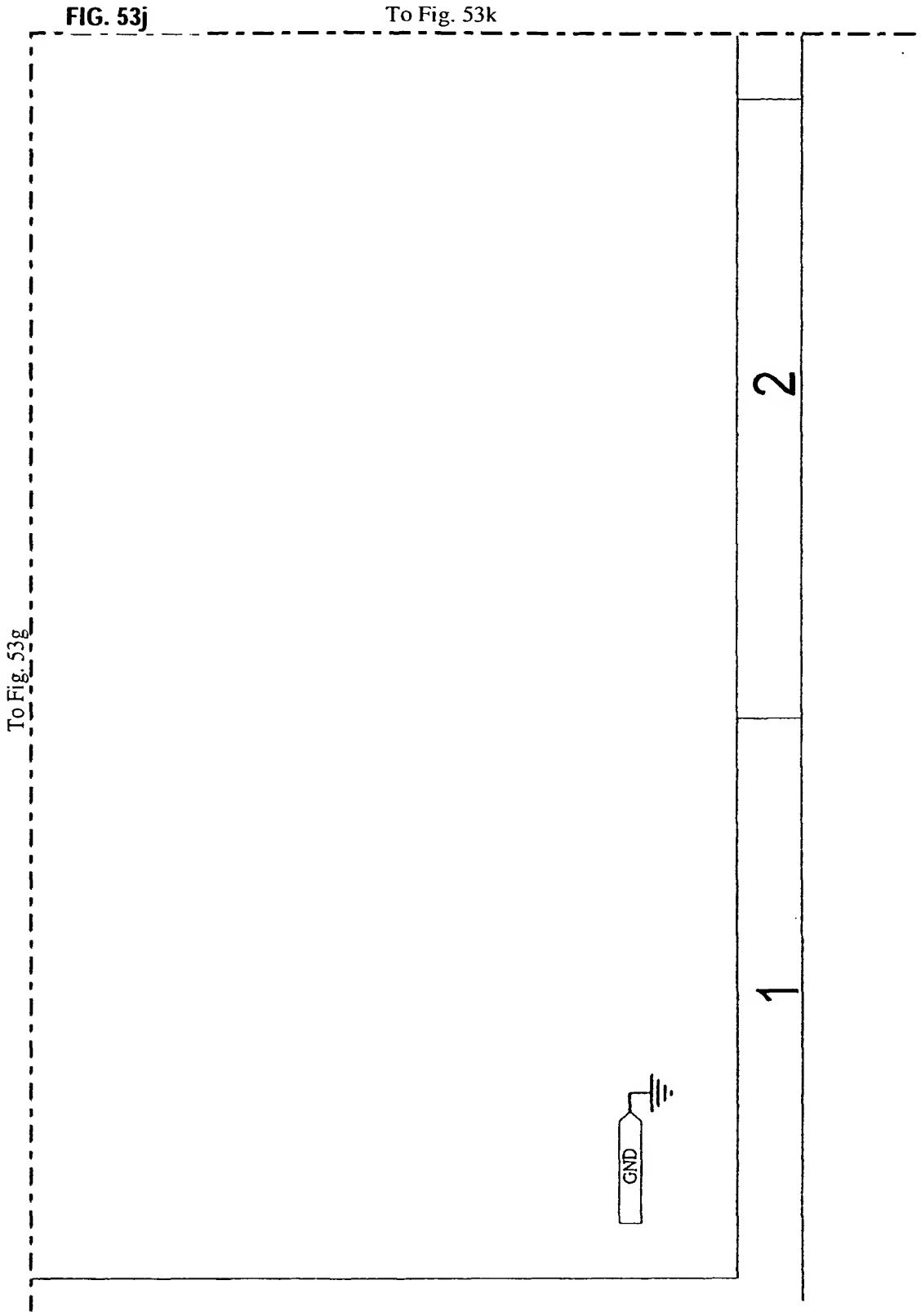
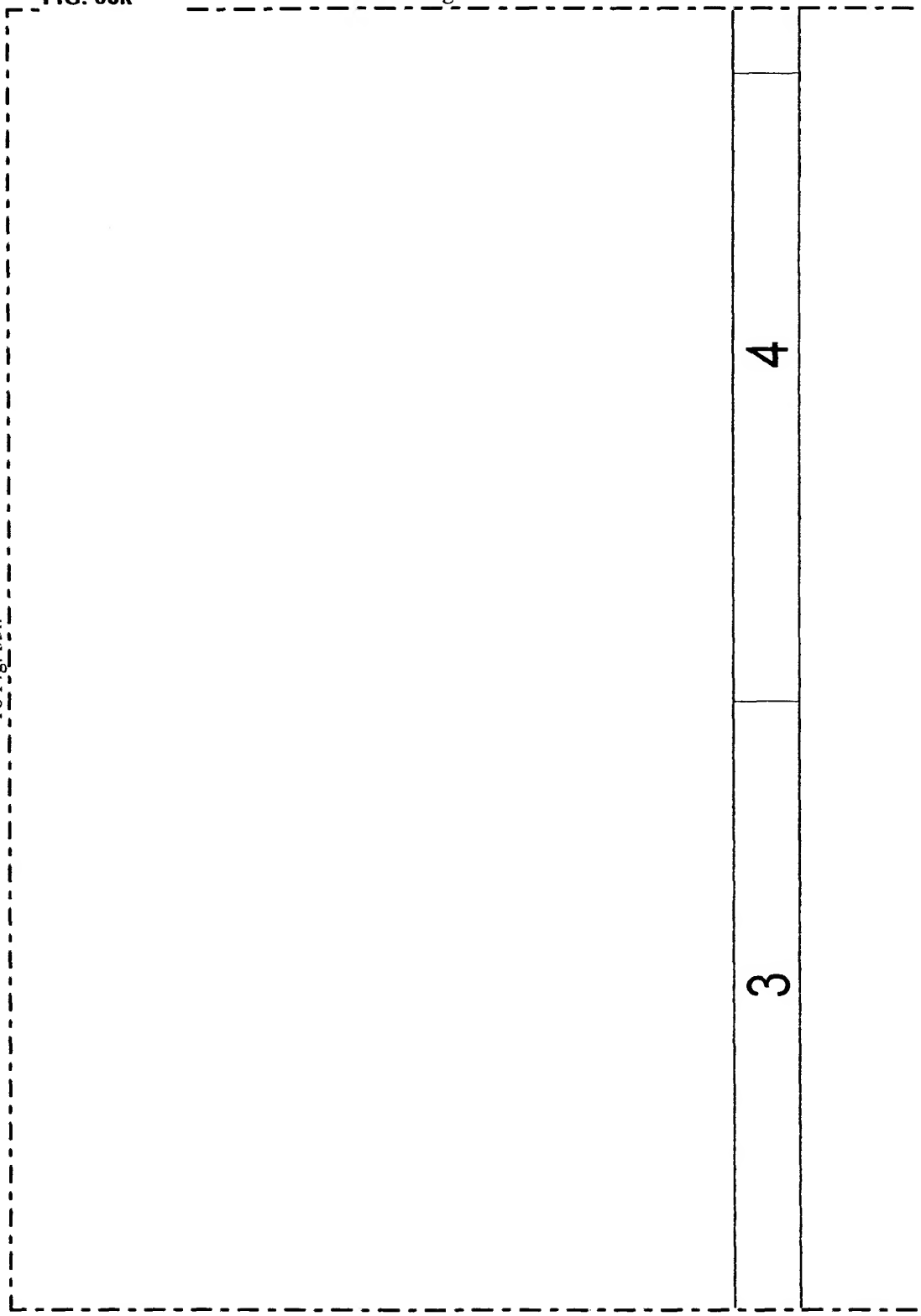


FIG. 53k

To Fig. 53l



To Fig. 53h

To Fig. 53j

FIG. 53l

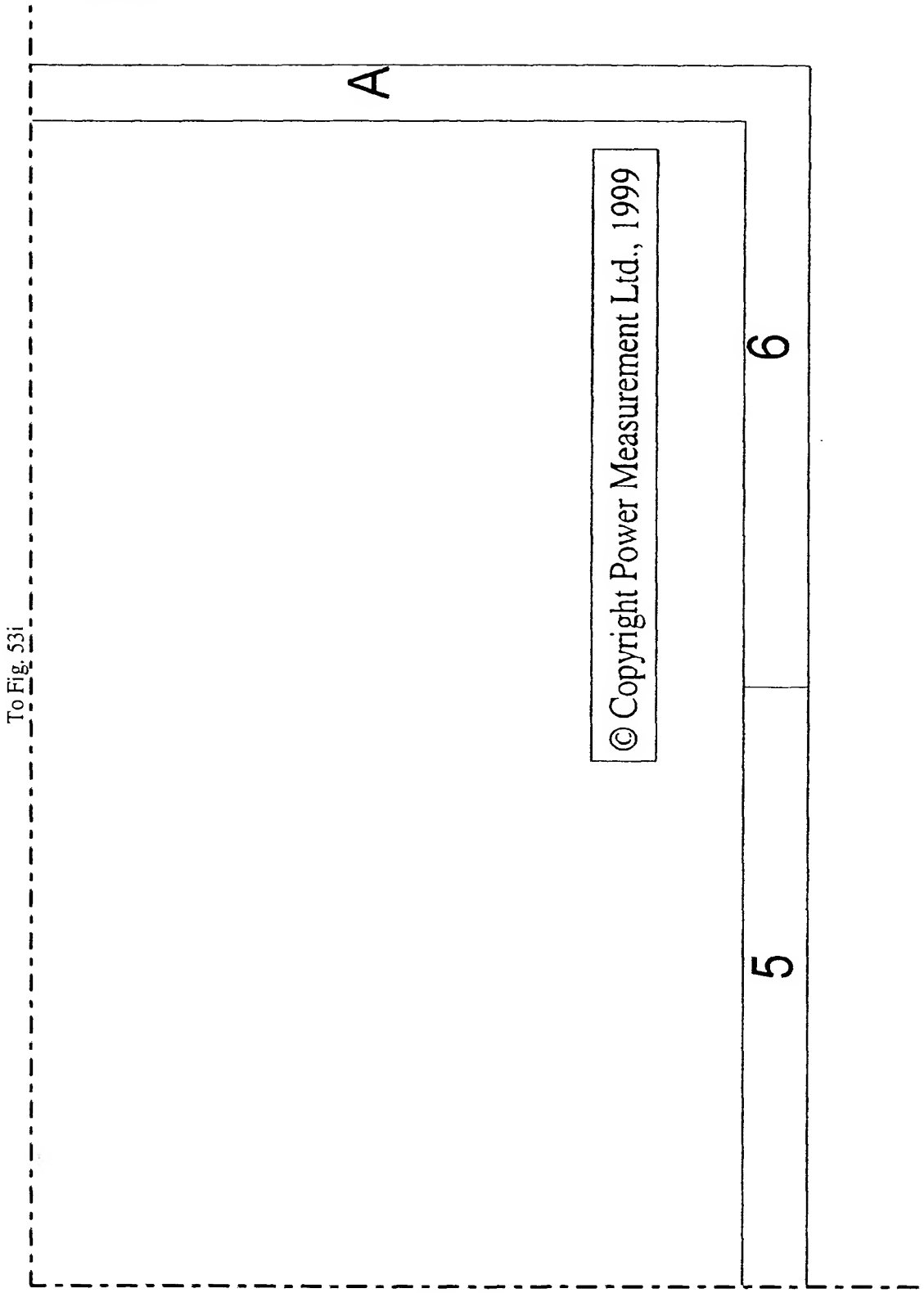

A
6
5
© Copyright Power Measurement Ltd., 1999
To Fig. 53i
To Fig. 53k

FIG. 54a

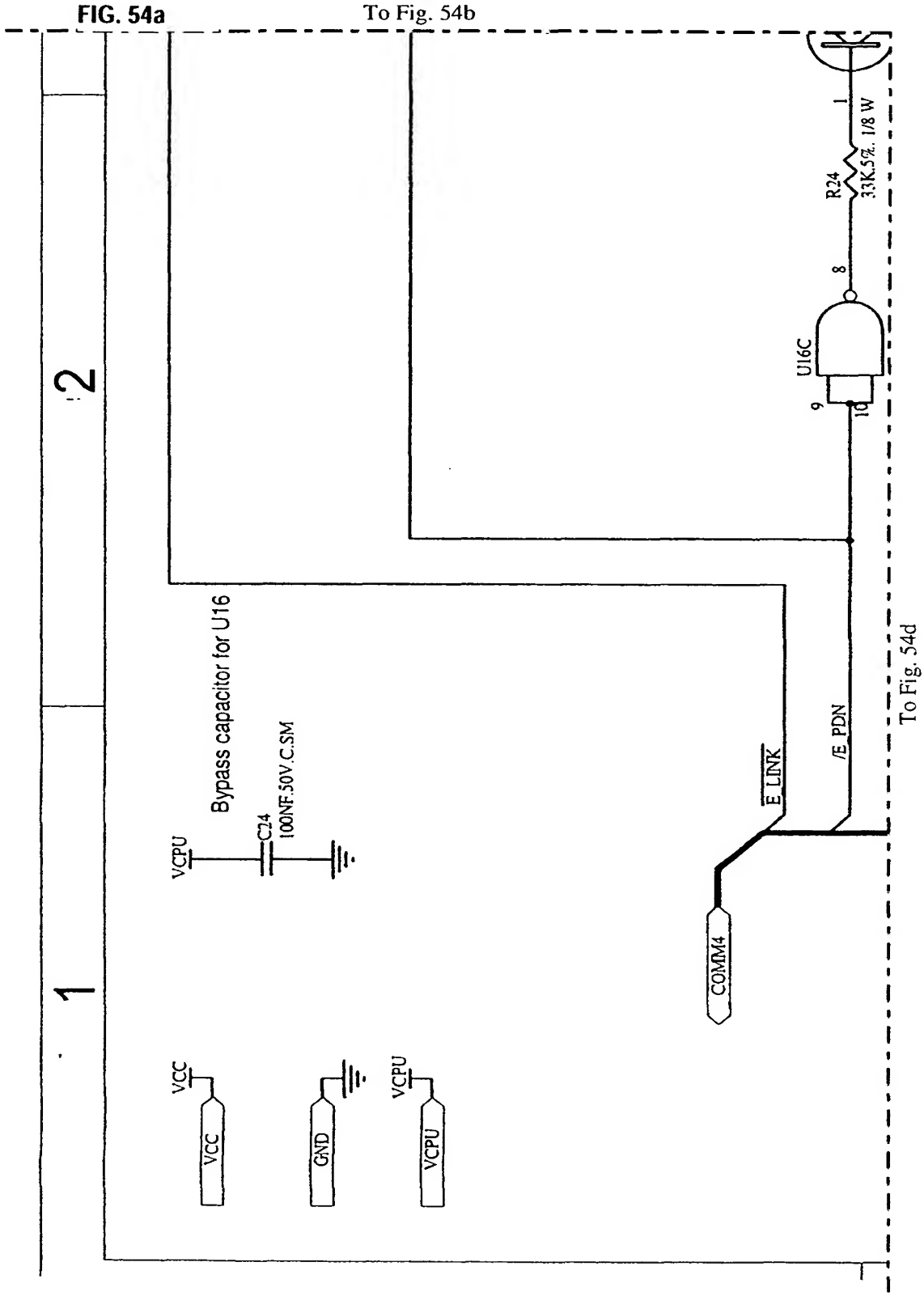

To Fig. 54b
2
1
R24
33K.5%. 1/8 W
8
U16C
9
10
Bypass capacitor for U16
C24
100NF.50V.C.SM
VCPU
E_LINK
/E_PDN
To Fig. 54d
COMM4
VCC
VCC
GND
VCPU
VCPU

FIG. 54b

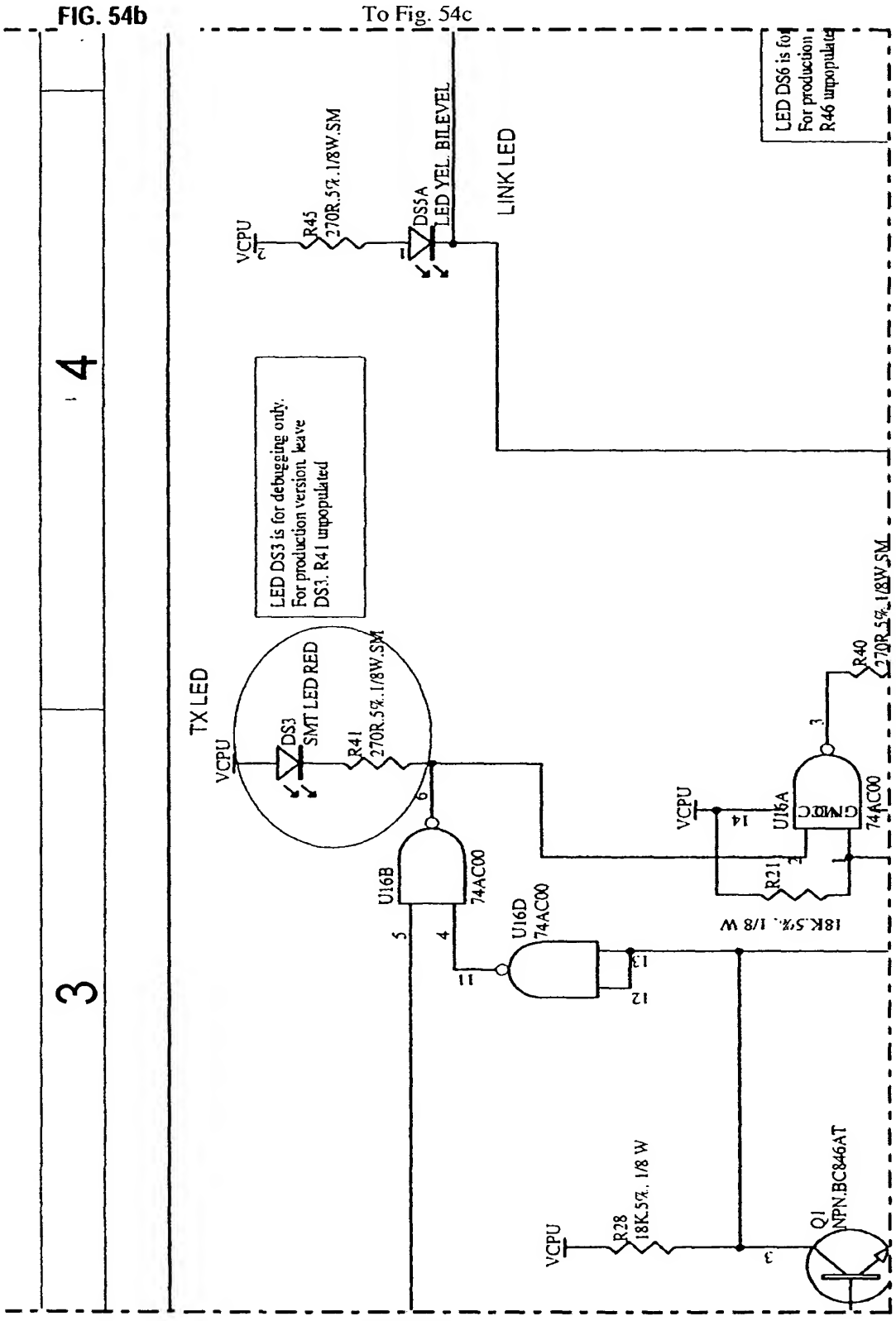

To Fig. 54c
LED DS6 is for
For production
R46 unpopulate
LINK LED
VCPU
R45
270R.5%.1/8W.SM
DS5A
LED YEL. BILEVEL
LED DS3 is for debugging only.
For production version leave
DS3. R41 unpopulated
TX LED
DS3
SMT LED RED
R41
270R.5%.1/8W.SM
R40
270R.5%.1/8W.SM
U16A
74AC00
U16B
74AC00
U16D
74AC00
R21
18K.5%. 1/8 W
R28
18K.5%. 1/8 W
Q1
NPN.BC846AT
To Fig. 54e
To Fig. 54a

FIG. 54c

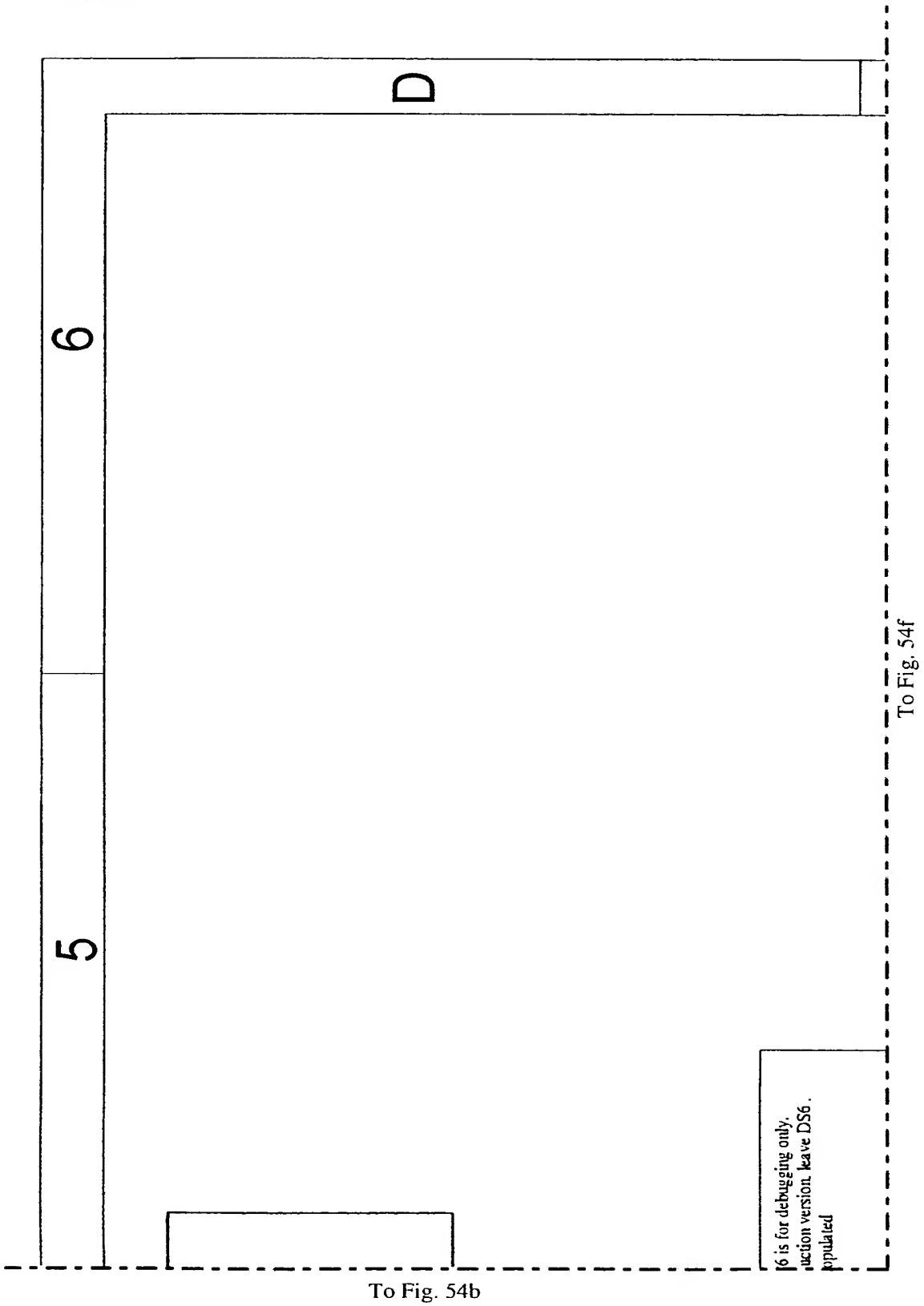

D
6
5
To Fig. 54f
6 is for debugging only,
uction version, leave DS6 .
ppulated
To Fig. 54b

FIG. 54d

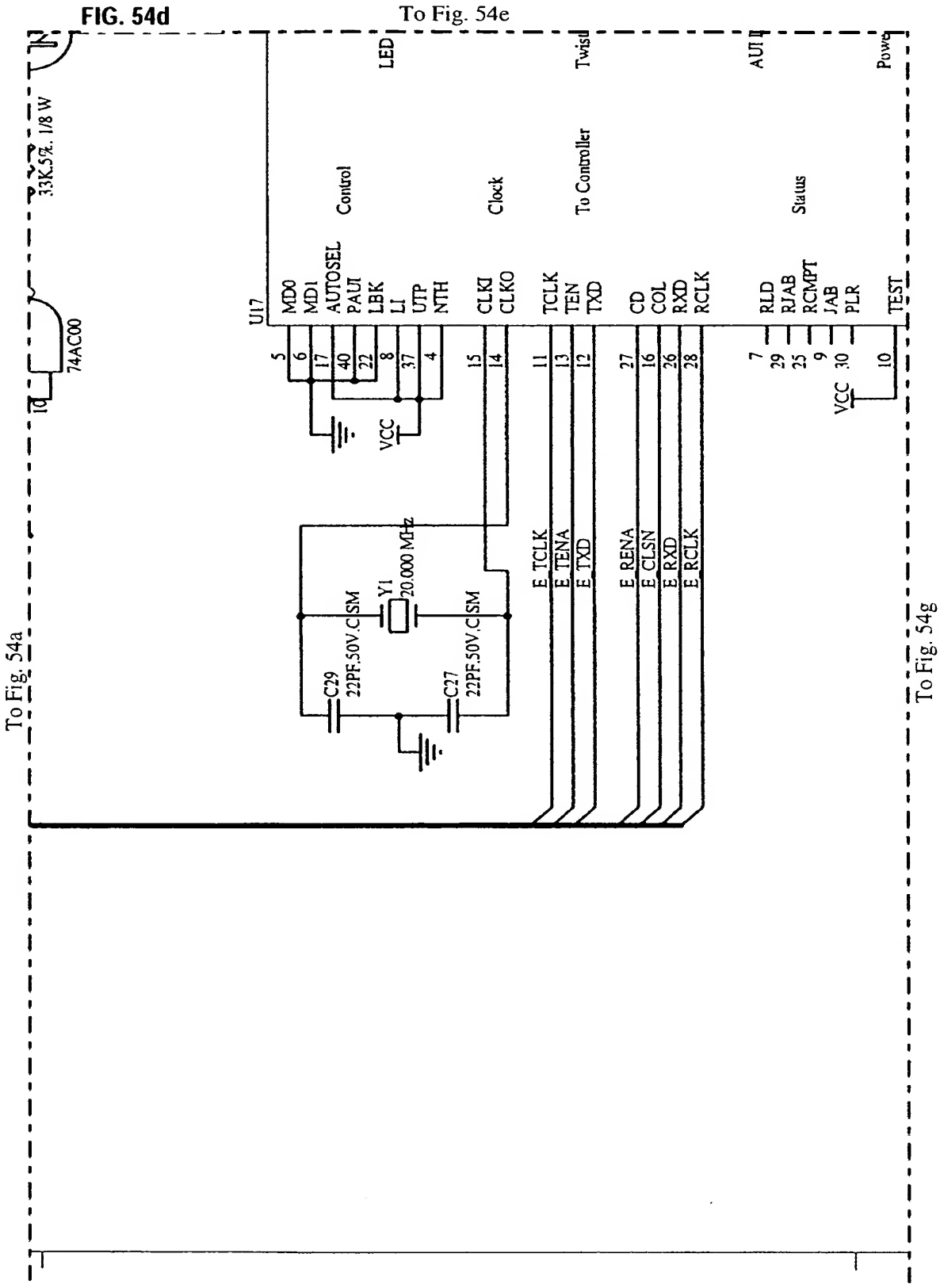
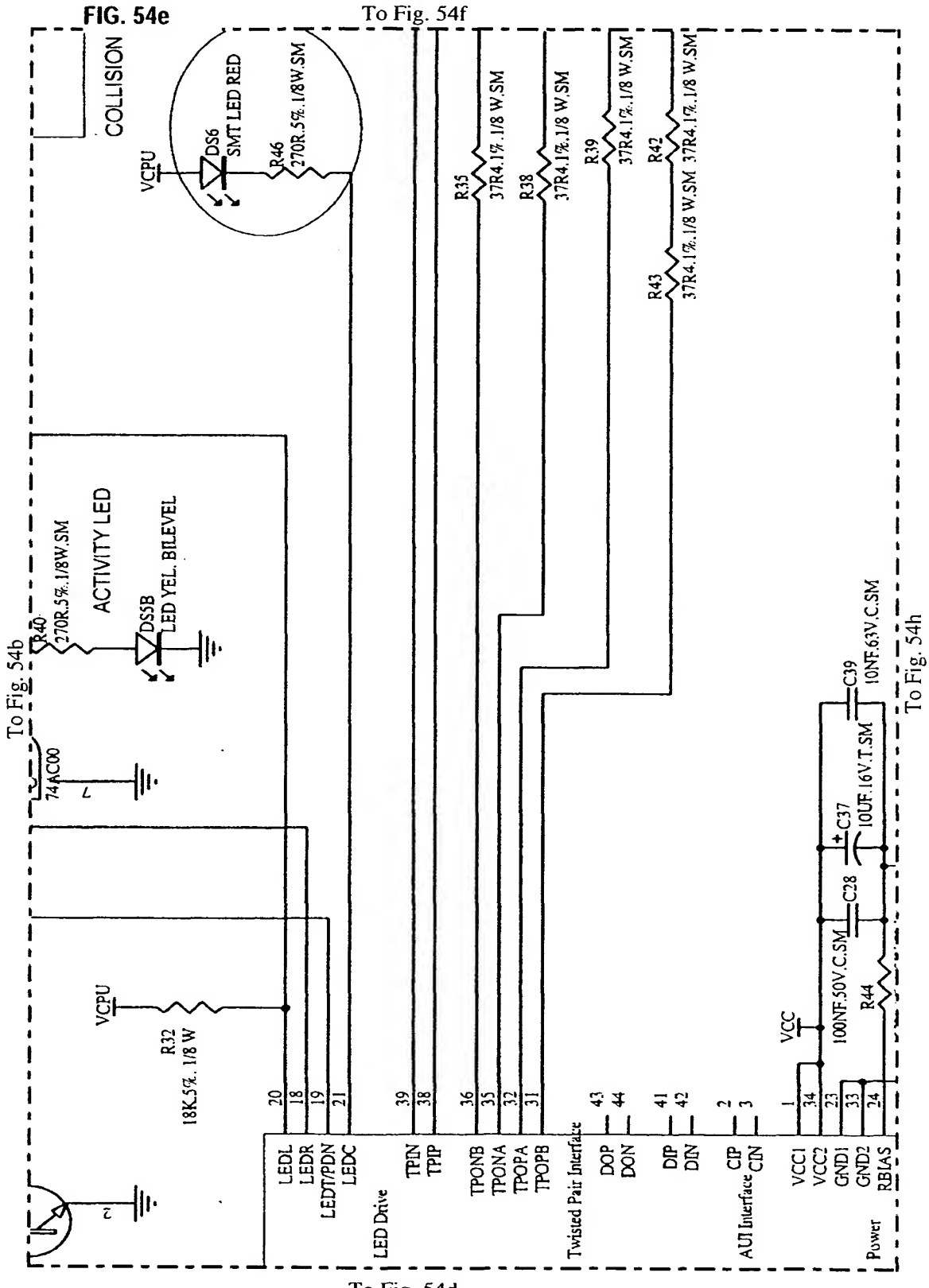

To Fig. 54e
To Fig. 54a
To Fig. 54g
33K,5%, 1/8 W
74AC00
U17
LED
Control
Clock
To Controller
Twisd
AUI
Status
Powe
MD0
MD1
AUTOSEL
PAUI
LBK
LI
UTP
NTH
CLKI
CLKO
TCLK
TEN
TXD
CD
COL
RXD
RCLK
RLD
RJAB
RCMPT
JAB
PLR
TEST
VCC
Y1
20.000 MHz
C29
22PF.50V.CSM
C27
22PF.50V.CSM
E_TCLK
E_TENA
E_TXD
E_RENA
E_CLSN
E_RXD
E_RCLK

FIG. 54e



To Fig. 54d

FIG. 54f

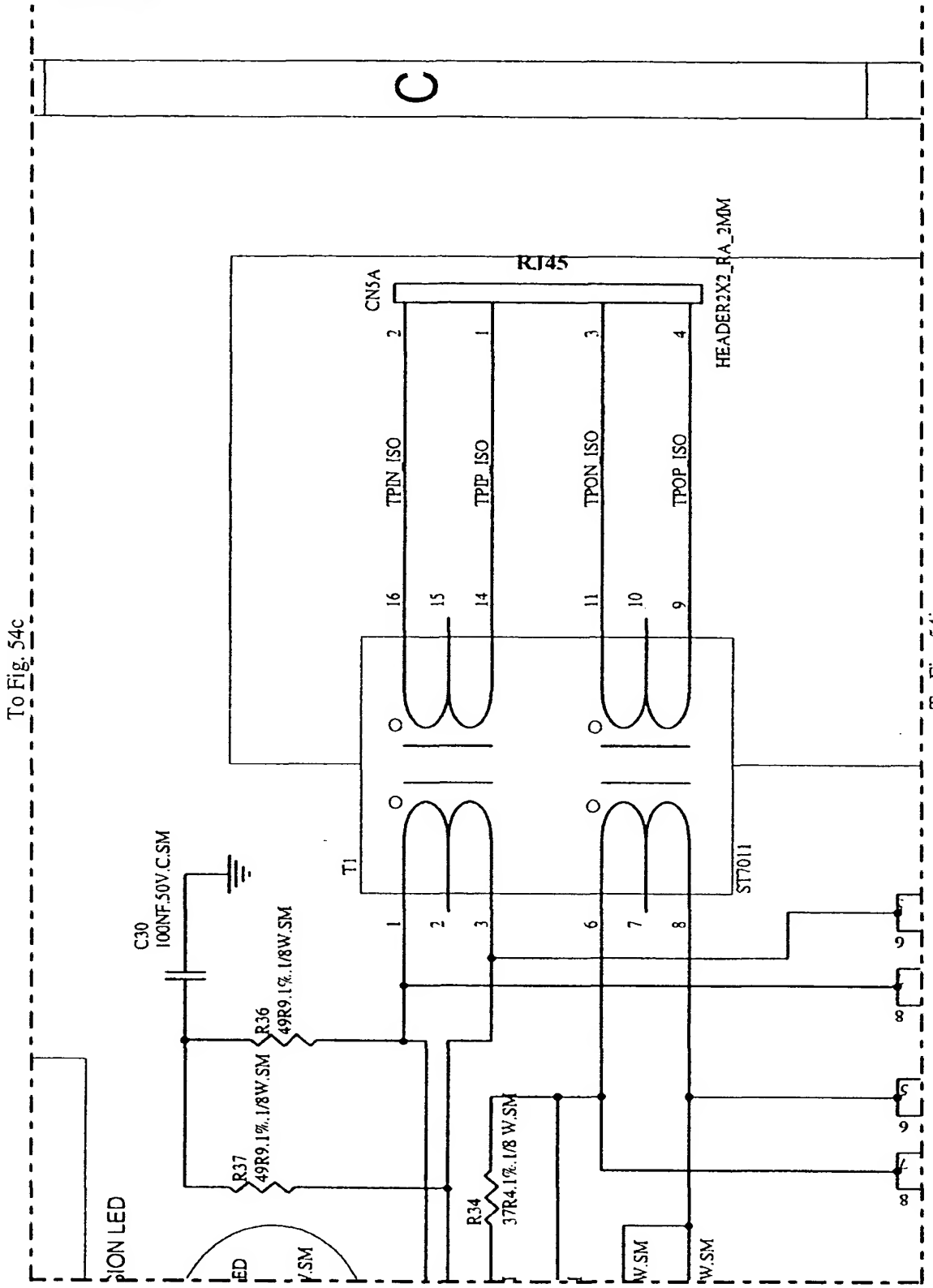

C
RJ45
CN5A
HEADER2X2_RA_2MM
TPIN ISO
TPIP ISO
TPON ISO
TPOP ISO
T1
ST7011
C30
100NF.50V.C.SM
R36
49R9.1%.1/8W.SM
R37
49R9.1%.1/8W.SM
R34
37R4.1%.1/8 W.SM
ION LED
To Fig. 54c
To Fig. 54i
To Fig. 54e

FIG. 54g

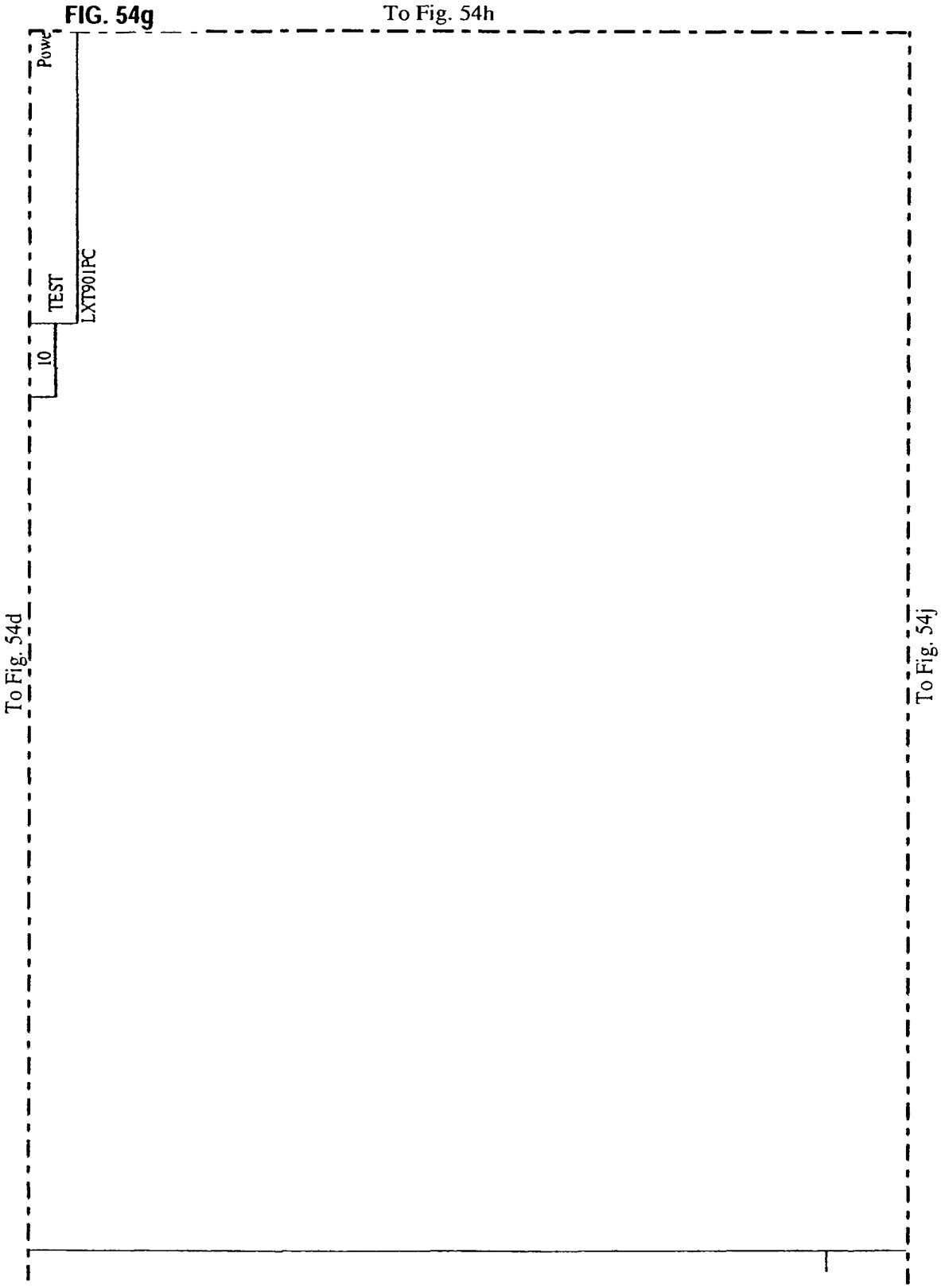
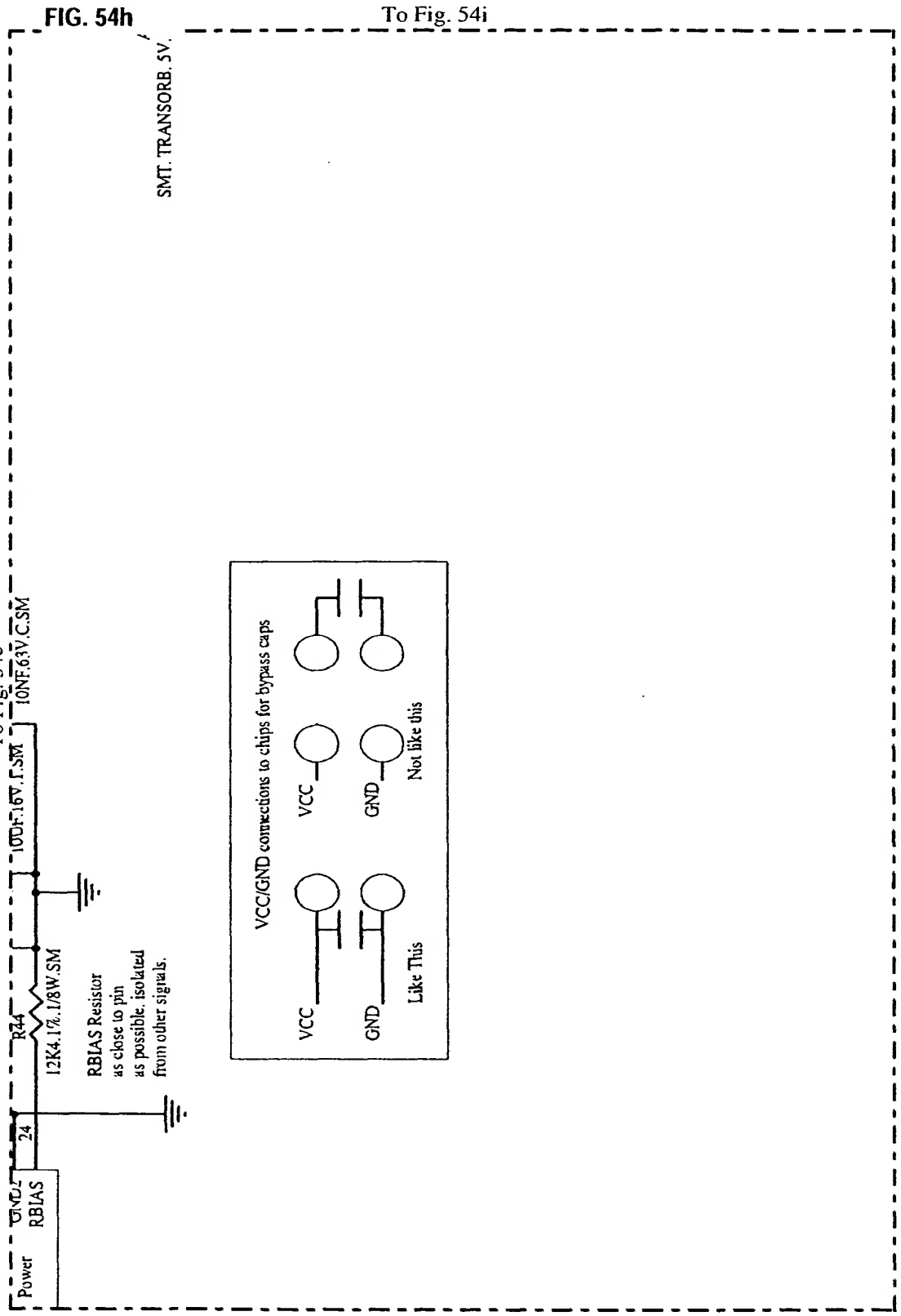
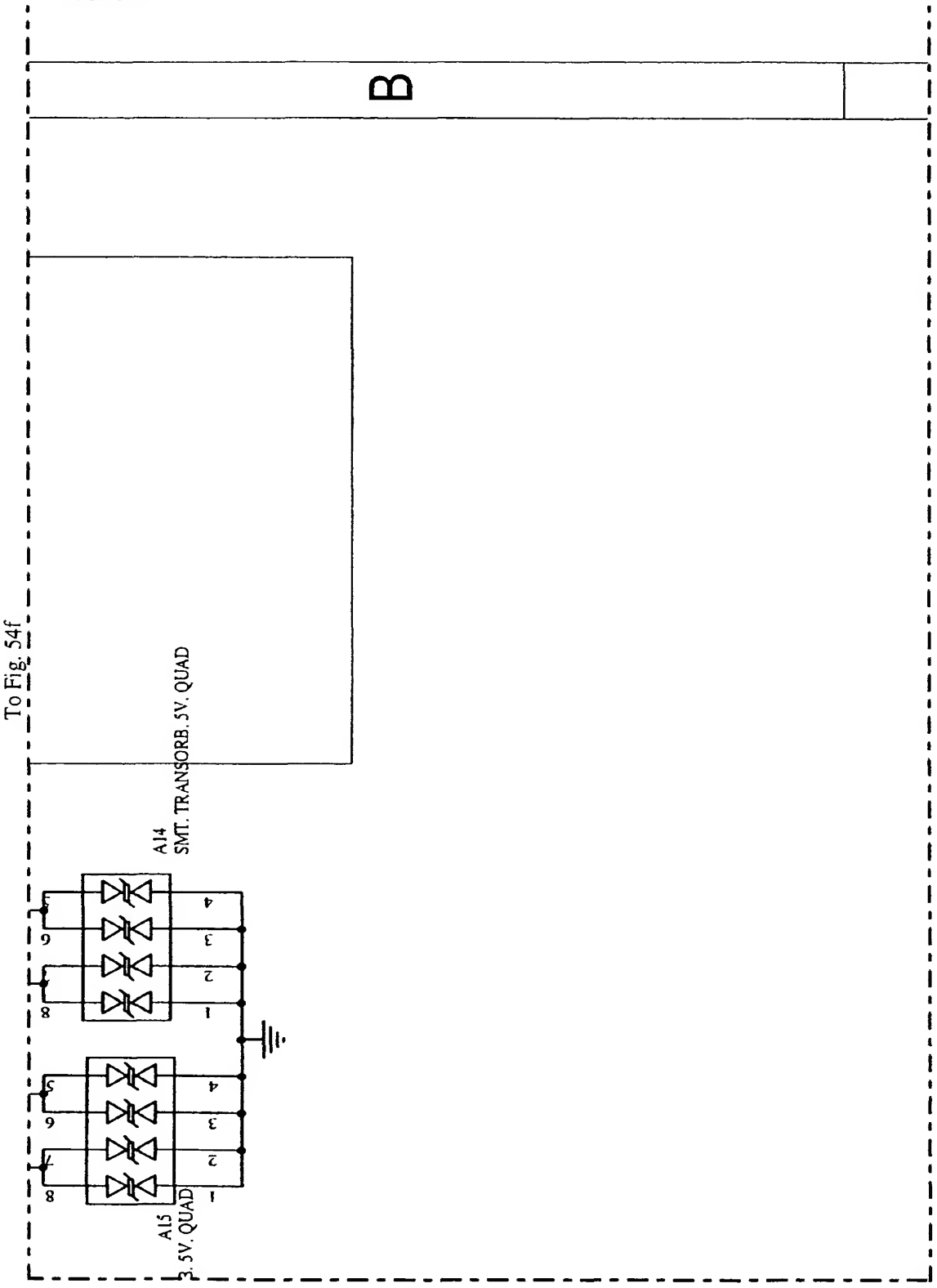


FIG. 54h



To Fig. 54g

FIG. 54i



To Fig. 54h

FIG. 54j

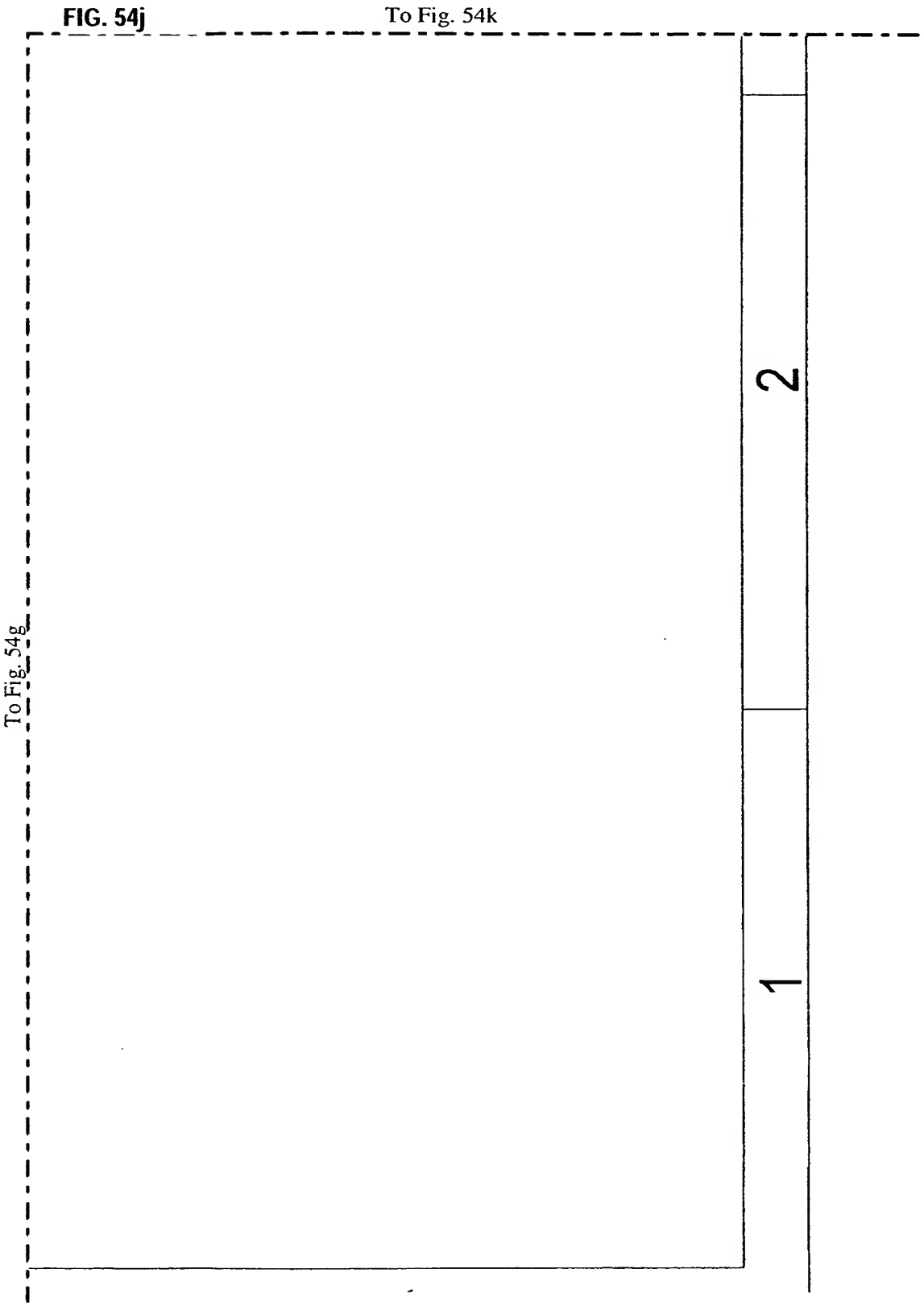


FIG. 54k

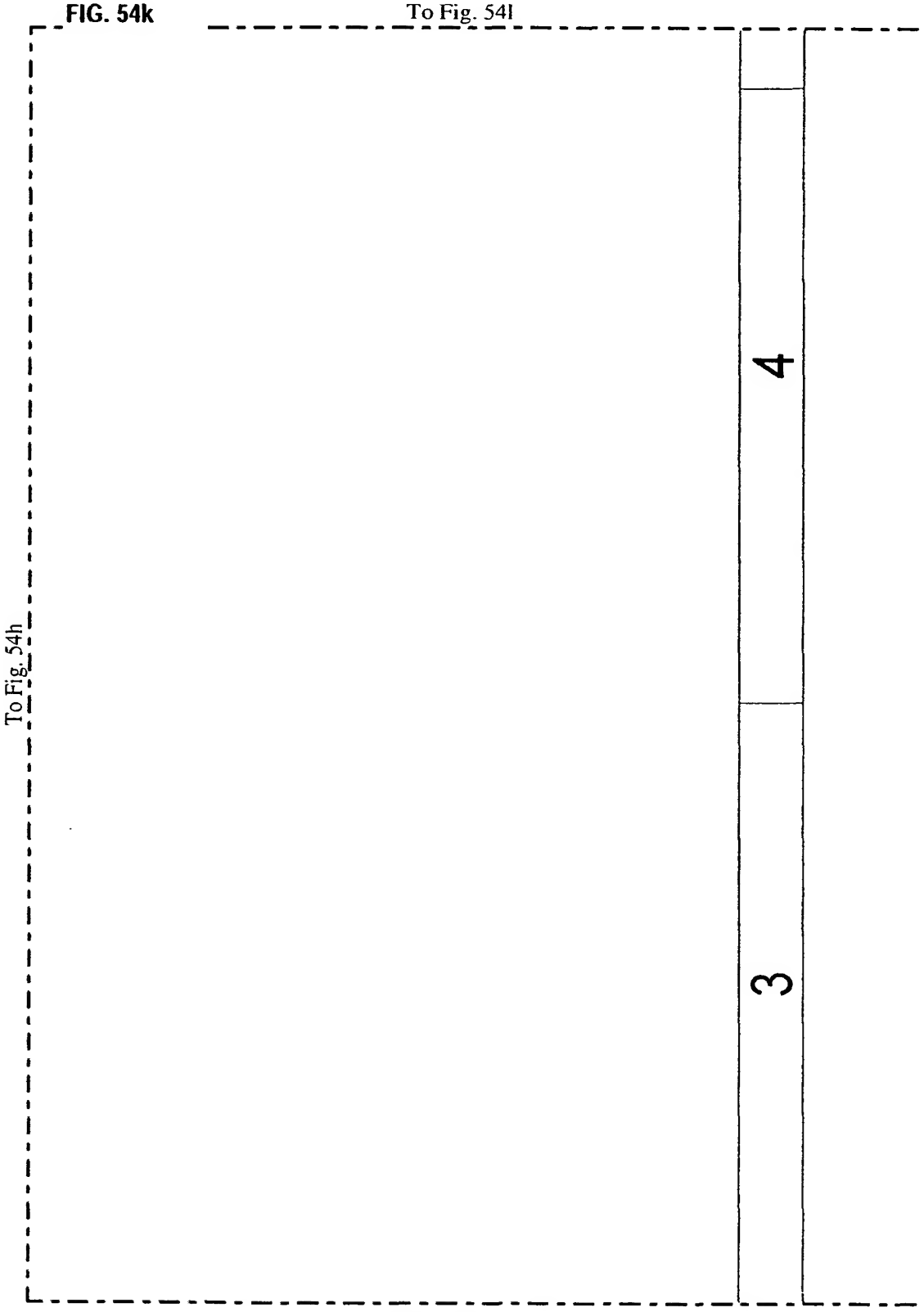


FIG. 54l

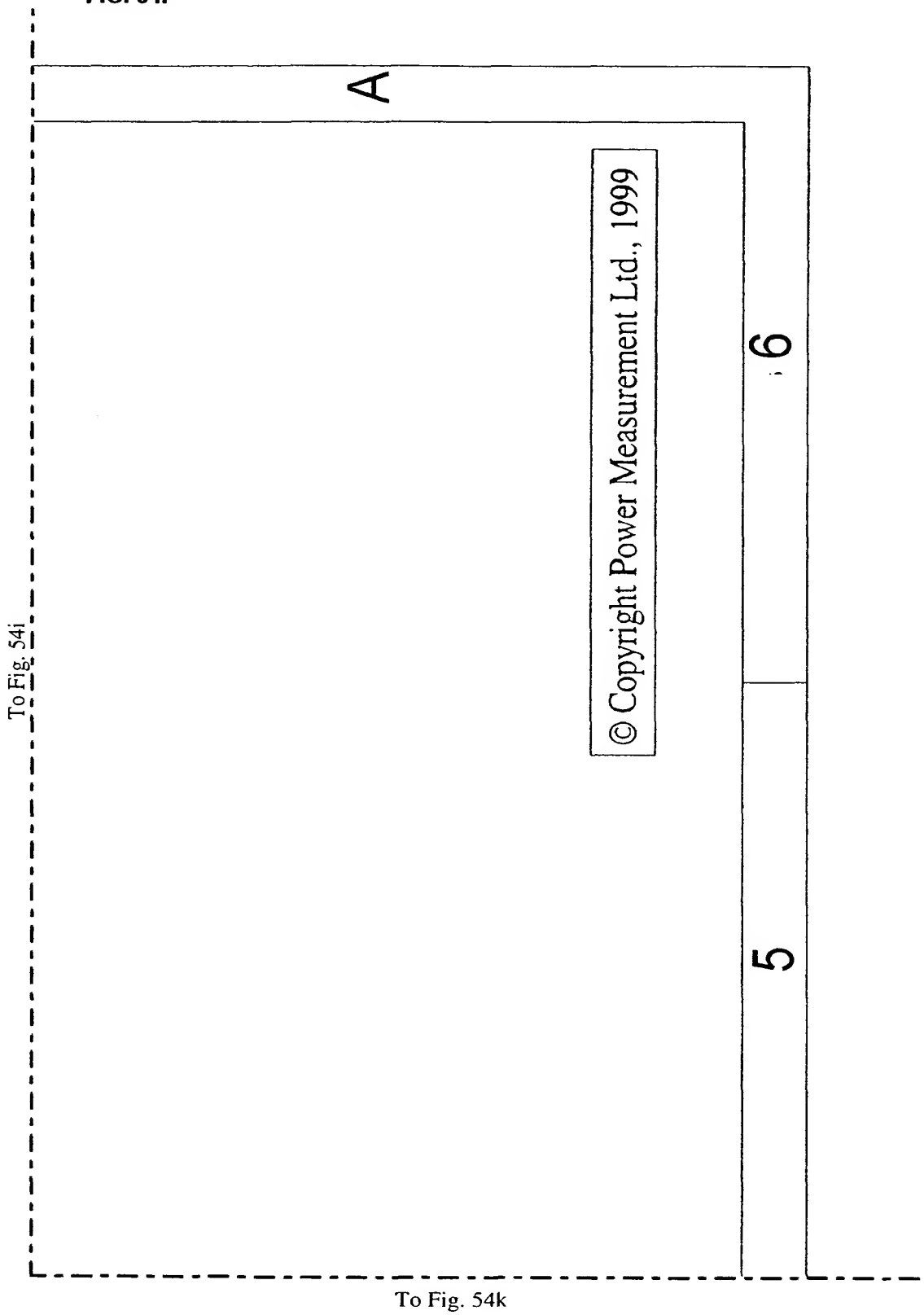

A
6
5
© Copyright Power Measurement Ltd., 1999
To Fig. 54i
To Fig. 54k

FIG. 55a

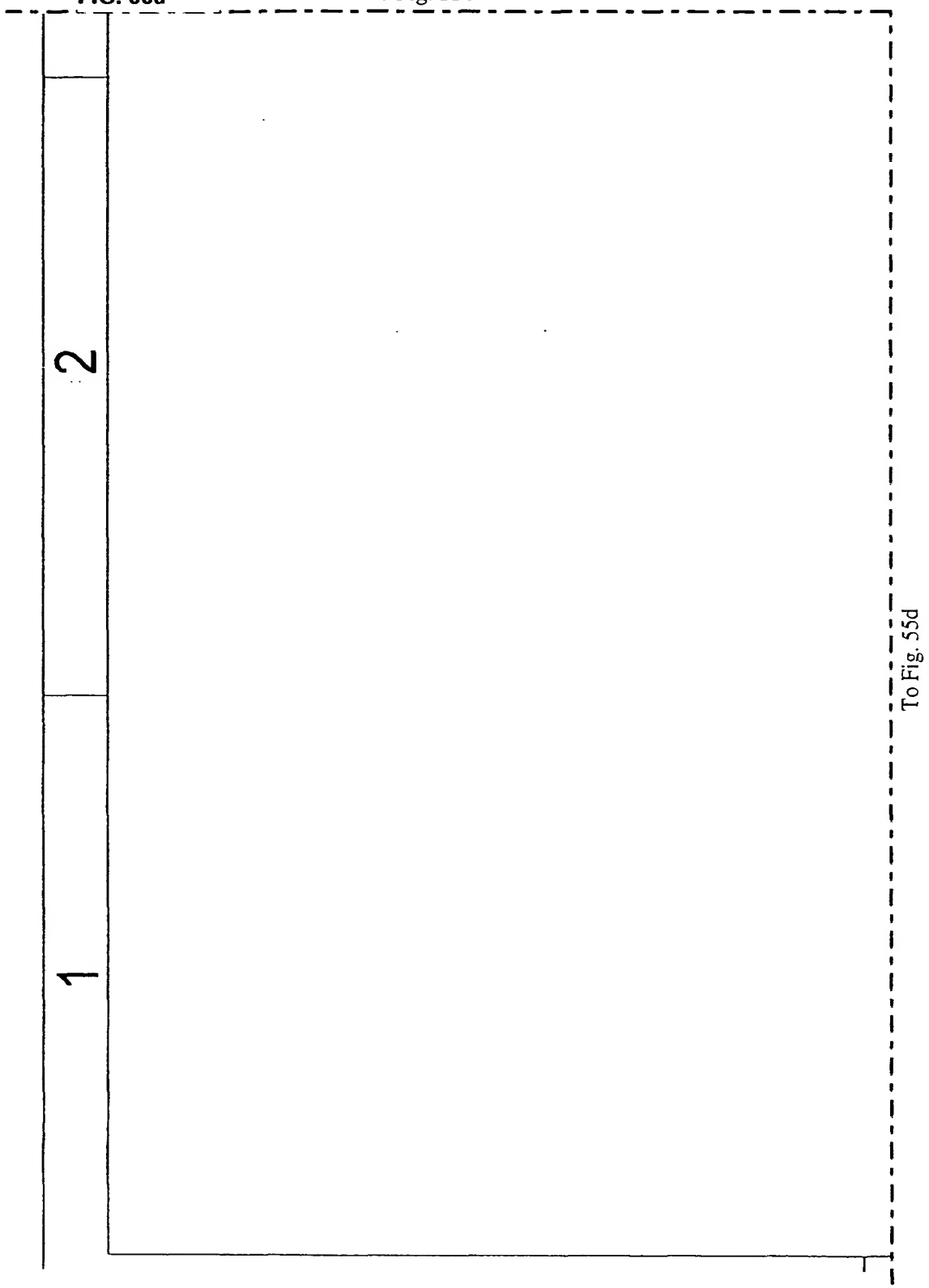


FIG. 55b

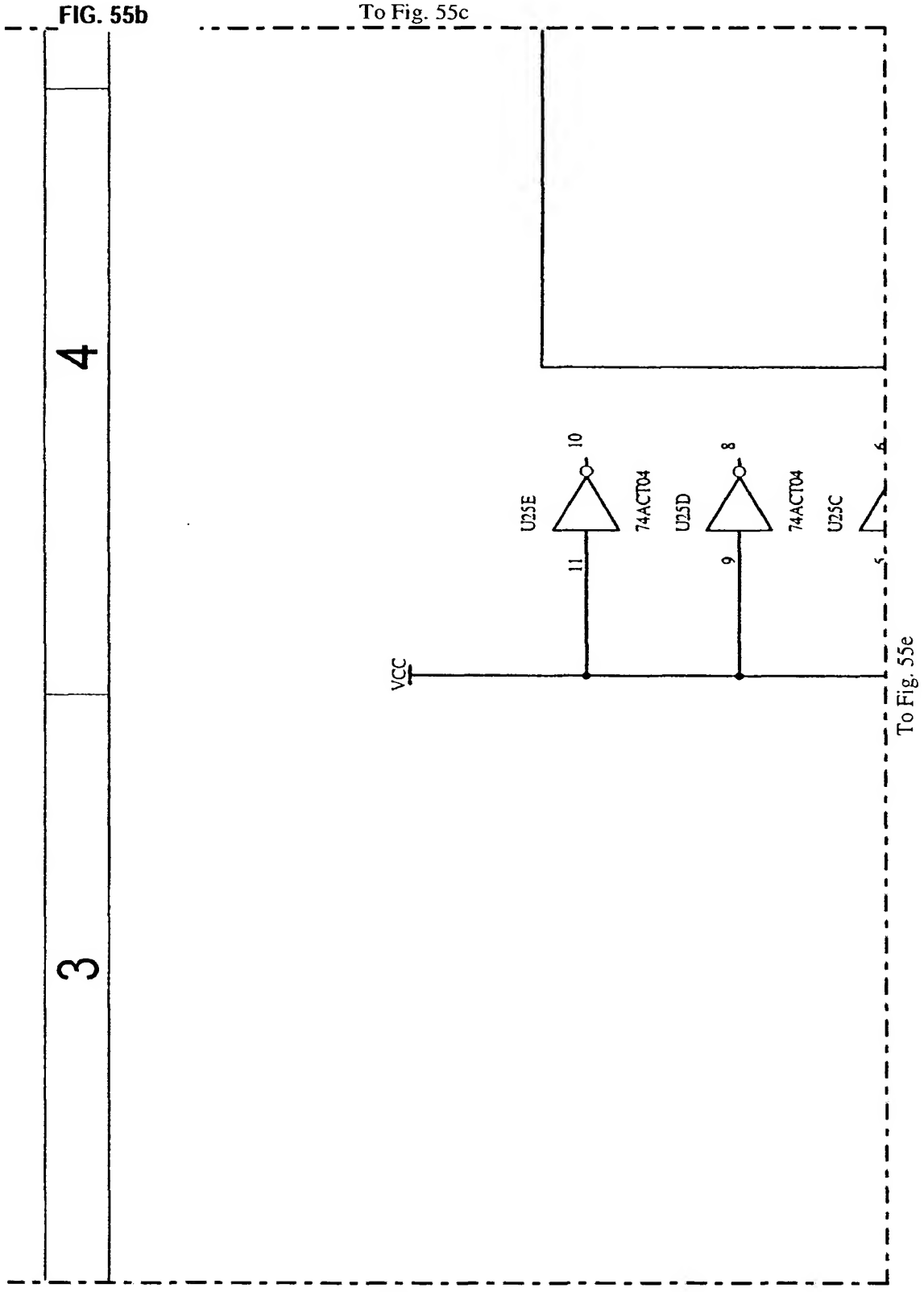

To Fig. 55c
4
3
U25E
74ACT04
U25D
74ACT04
U25C
10
8
6
11
9
5
VCC
To Fig. 55e
To Fig. 55a

FIG. 55c

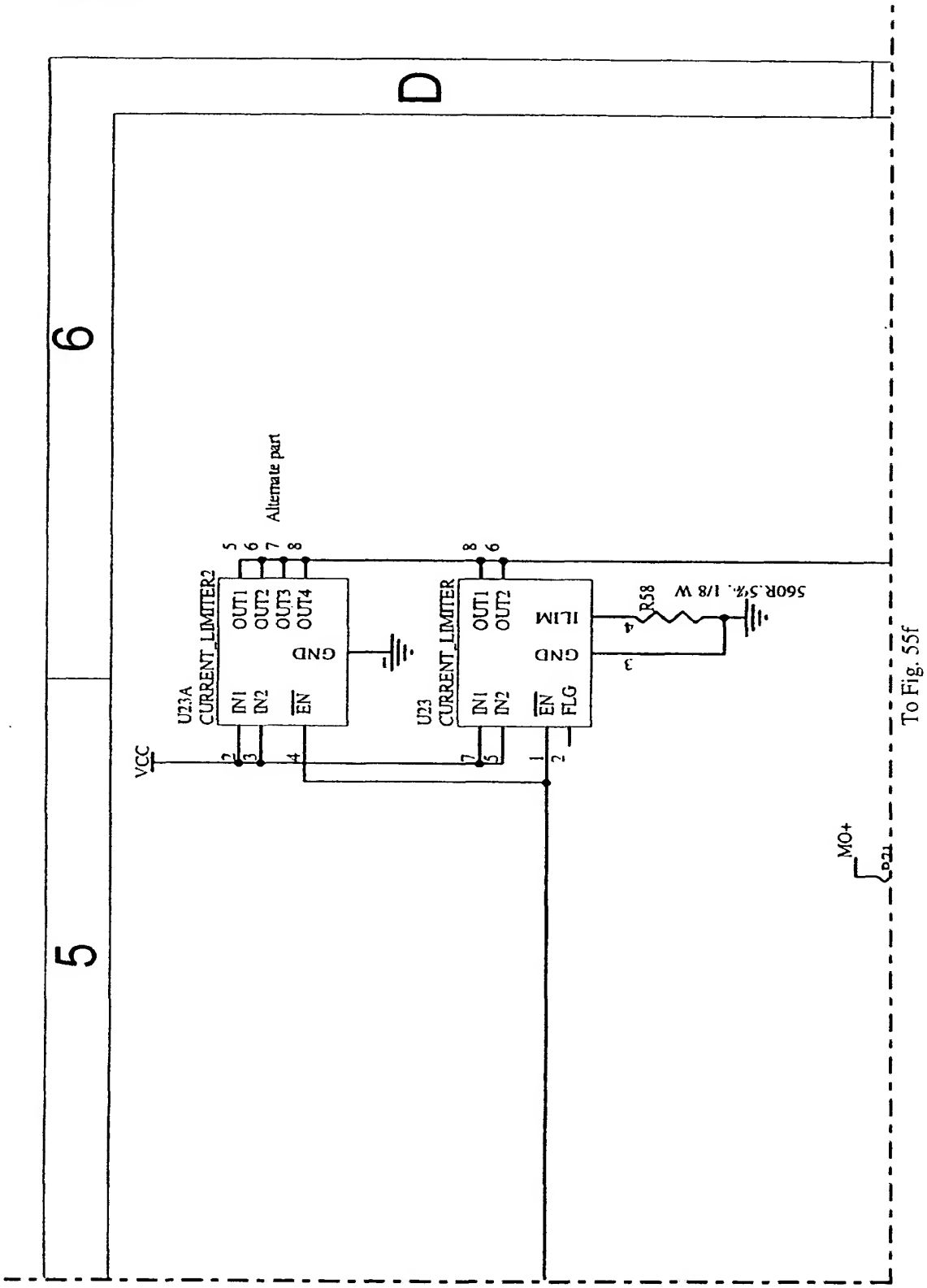

D
6
5
Alternate part
U23A
CURRENT_LIMITER2
OUT1
OUT2
OUT3
OUT4
GND
IN1
IN2
EN
U23
CURRENT_LIMITER
OUT1
OUT2
ILIM
GND
IN1
IN2
EN
FLG
R58
560R 5% 1/8 W
VCC
MO+
To Fig. 55f
To Fig. 55b

FIG. 55d

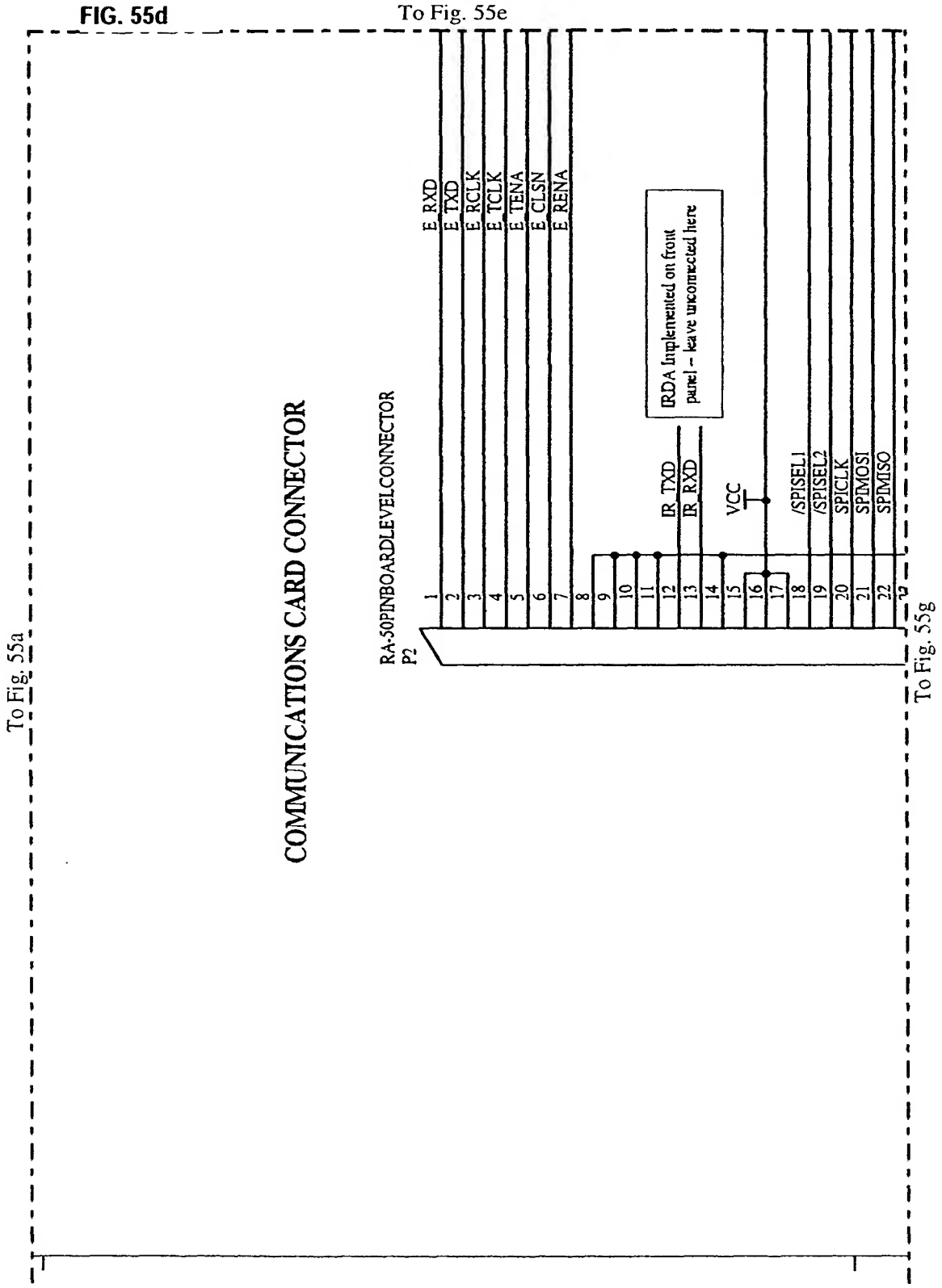

To Fig. 55e
To Fig. 55a
To Fig. 55g
COMMUNICATIONS CARD CONNECTOR
RA-50PINBOARDLEVELCONNECTOR
P2
E_RXD
E_TXD
E_RCLK
E_TCLK
E_TENA
E_CLSN
E_RENA
IR_TXD
IR_RXD
VCC
/SPISEL1
/SPISEL2
SPICLK
SPIMOSI
SPIMISO
IRDA Implemented on front panel – leave unconnected here
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22

FIG. 55e

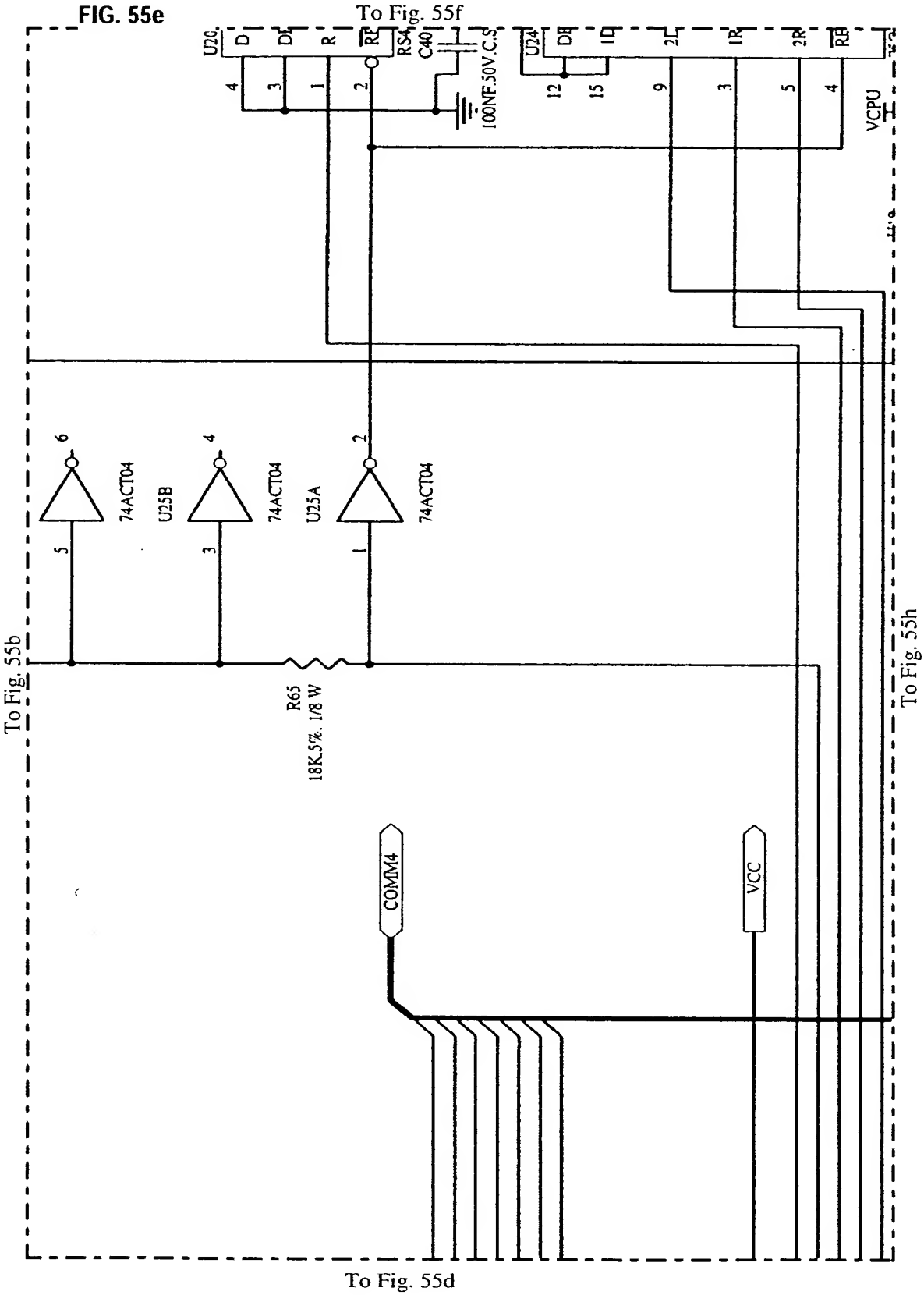

To Fig. 55f
U20
D
D1
R
R1
RS1
C40
100NF.50V.C.S
U24
D2
1D
2D
1R
2R
R2
VCPU
74ACT04
U25B
U25A
R65
18K.5%. 1/8 W
To Fig. 55b
To Fig. 55h
COMM4
VCC
To Fig. 55d

FIG. 55f

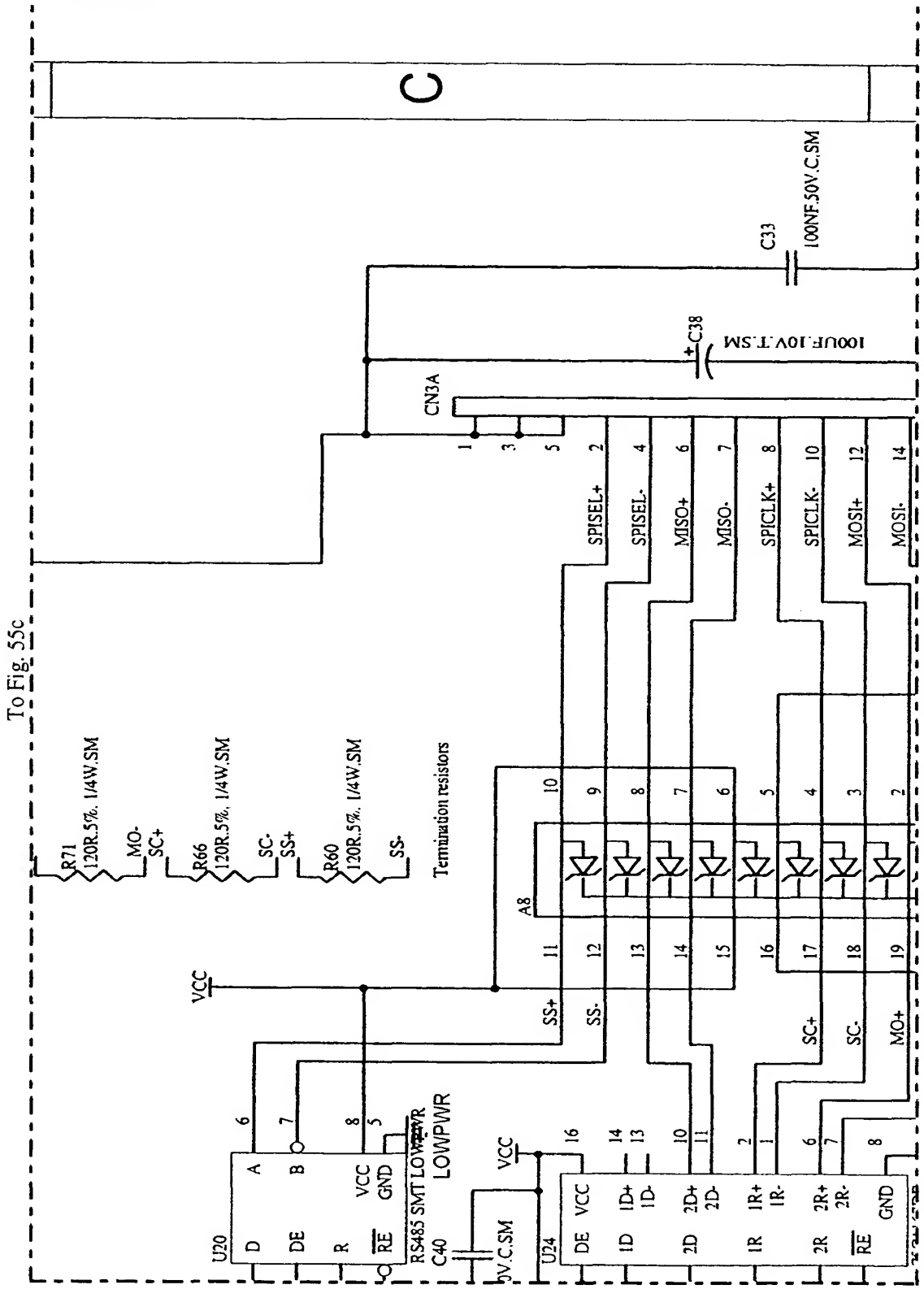

C
C33
100NF.50V.C.SM
C38
100UF.10V.T.SM
CN3A
SPISEL+
SPISEL-
MISO+
MISO-
SPICLK+
SPICLK-
MOSI+
MOSI-
To Fig. 55c
To Fig. 55i
R71
120R.5%. 1/4W.SM
MO-
SC+
R66
120R.5%. 1/4W.SM
SC-
SS+
R60
120R.5%. 1/4W.SM
SS-
Termination resistors
A8
VCC
SS+
SS-
SC+
SC-
MO+
U20
D
DE
R
RE
A
B
VCC
GND
RS485 SMT LOWPWR
LOWPWR
C40
.1V.C.SM
U24
DE
VCC
1D+
1D-
1D
2D+
2D-
2D
1R+
1R-
1R
2R+
2R-
2R
RE
GND
To Fig. 55e

FIG. 55g

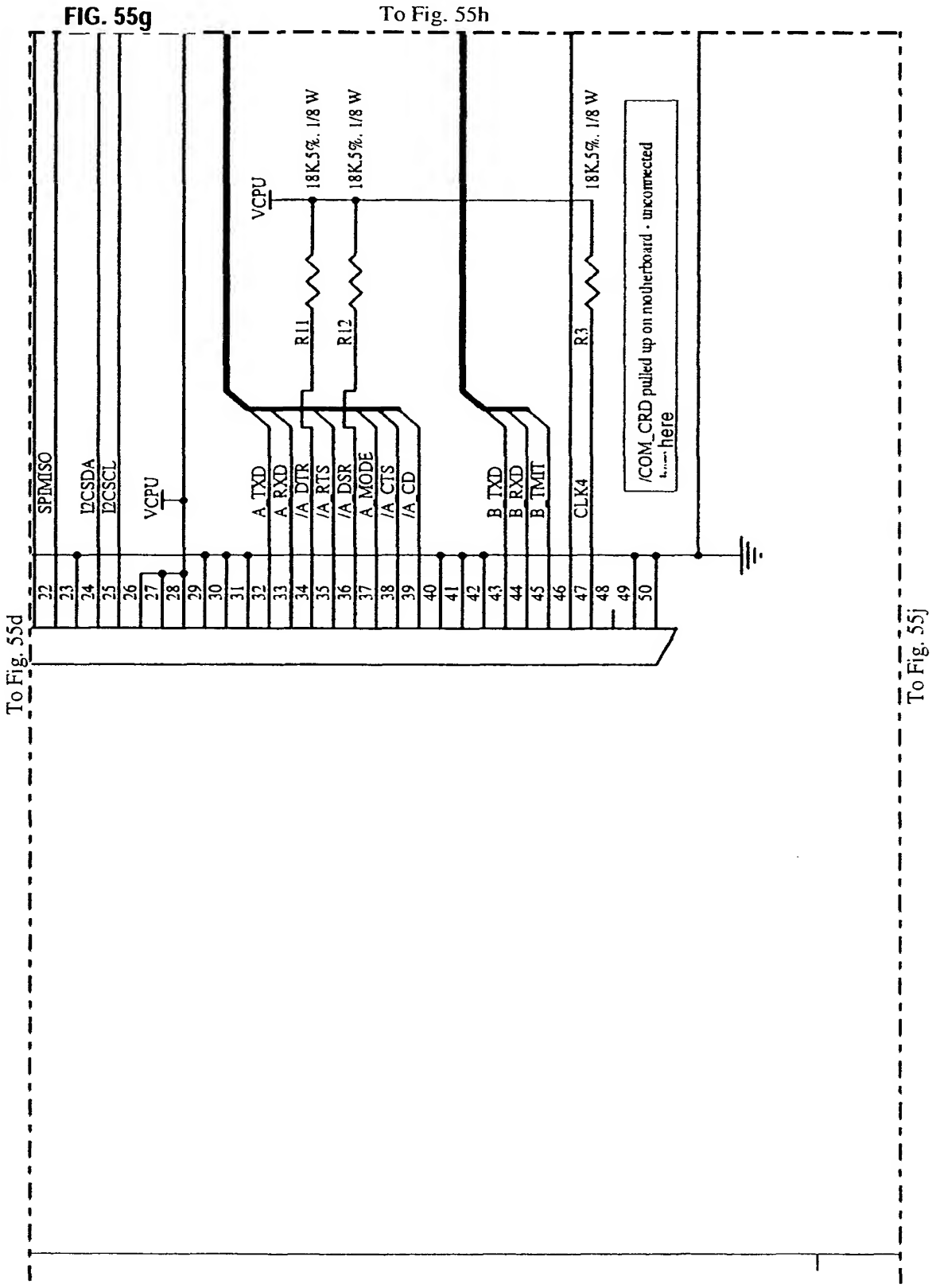

To Fig. 55h
To Fig. 55d
To Fig. 55j
SPIMISO
I2CSDA
I2CSCL
VCPU
VCPU
A_TXD
A_RXD
/A_DTR
/A_RTS
/A_DSR
A_MODE
/A_CTS
/A_CD
B_TXD
B_RXD
B_TMIT
CLK4
R11
R12
R3
18K.5%. 1/8 W
18K.5%. 1/8 W
18K.5%. 1/8 W
/COM_CRD pulled up on motherboard - uncon... here
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50

FIG. 55h

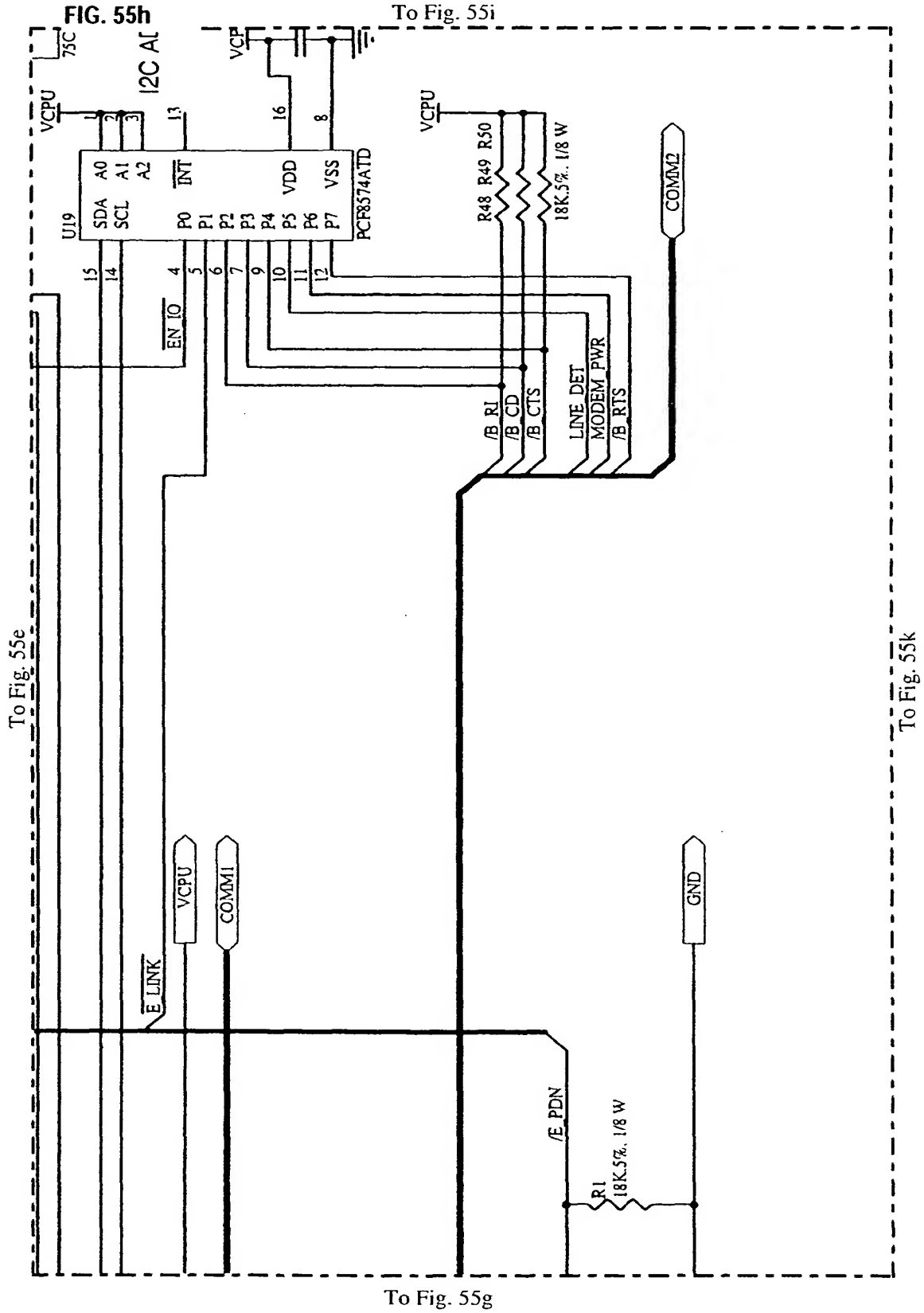

To Fig. 55i
To Fig. 55e
To Fig. 55k
To Fig. 55g
I2C A[
75C
VCPU
VCP
U19
PCF8574ATD
A0
A1
A2
INT
VDD
VSS
SDA
SCL
P0
P1
P2
P3
P4
P5
P6
P7
R48
R49
R50
18K.5%. 1/8 W
COMM2
EN IO
/B RI
/B CD
/B CTS
LINE DET
MODEM PWR
/B RTS
E LINK
COMM1
GND
/E PDN
R1
18K.5%. 1/8 W

FIG. 55i

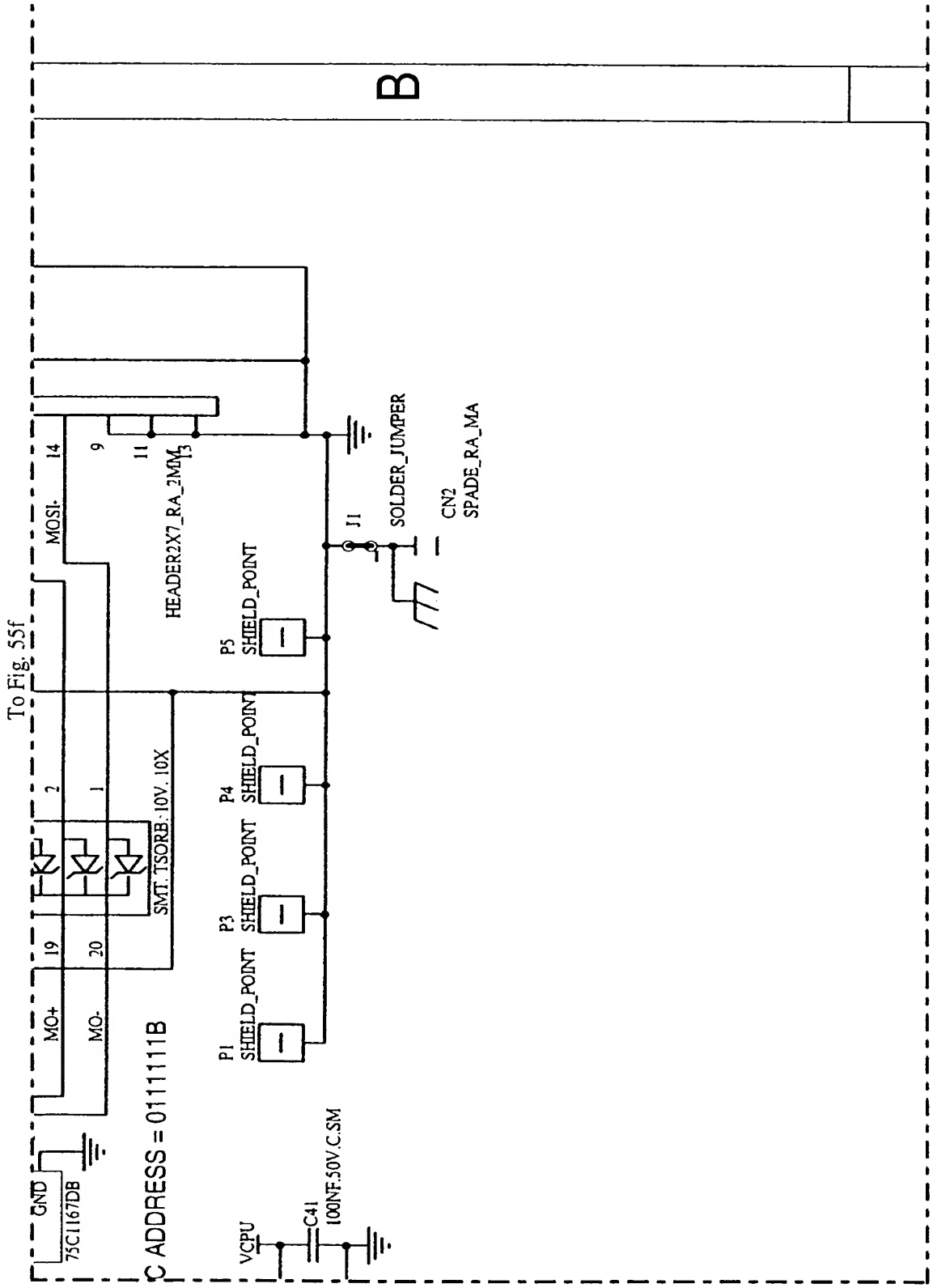
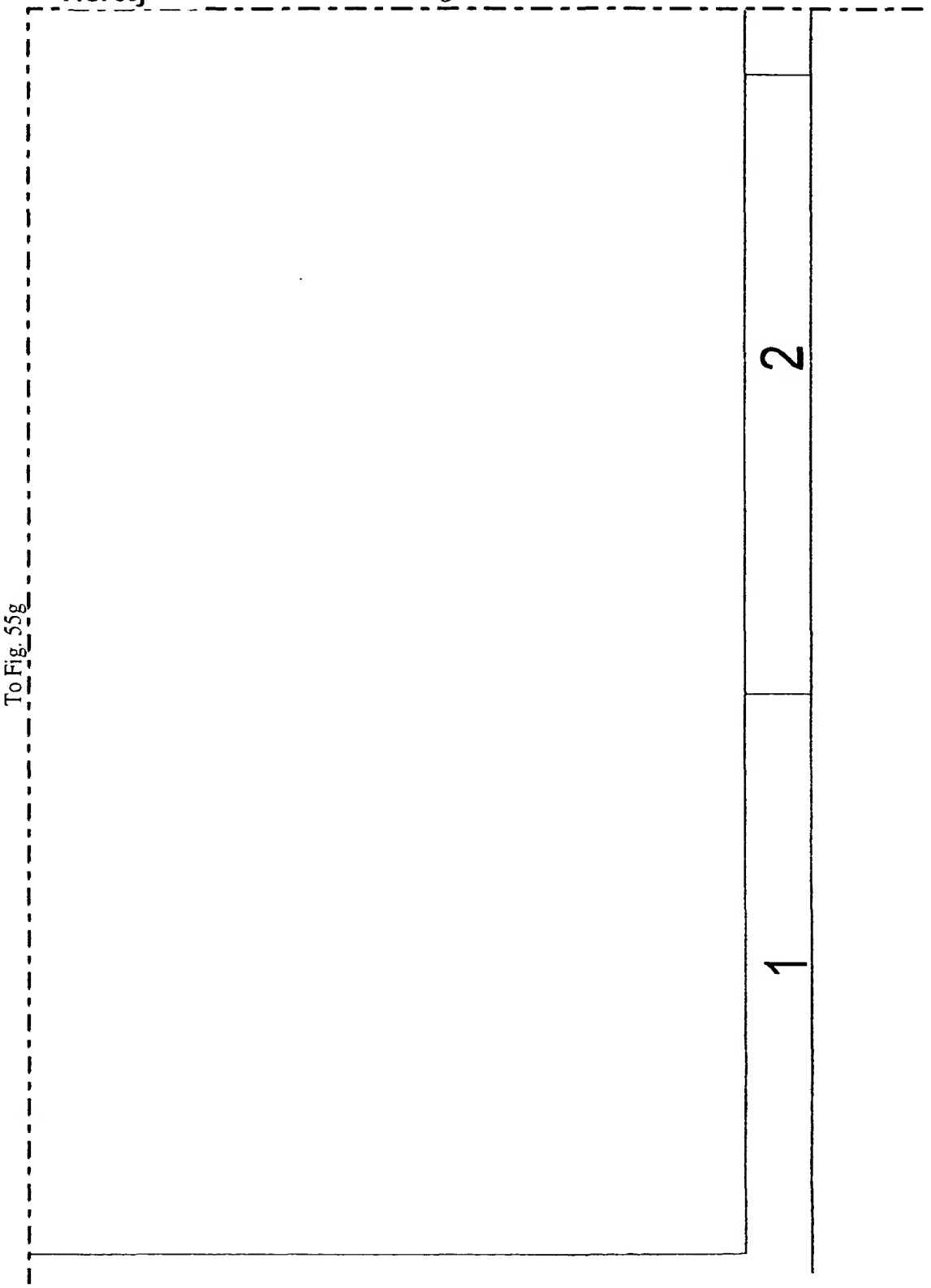

B
To Fig. 55f
To Fig. 55l
To Fig. 55h
C ADDRESS = 0111111B
GND
75C1167DB
MO+
MO-
MOSI-
19
20
14
2
1
9
11
13
SMT. TSORB: 10V. 10X
HEADER2X7_RA_2MM
P1 SHIELD_POINT
P3 SHIELD_POINT
P4 SHIELD_POINT
P5 SHIELD_POINT
J1
SOLDER_JUMPER
CN2
SPADE_RA_MA
VCPU
C41
100NF.50V.C.SM

FIG. 55j

To Fig. 55k



To Fig. 55g

FIG. 55k

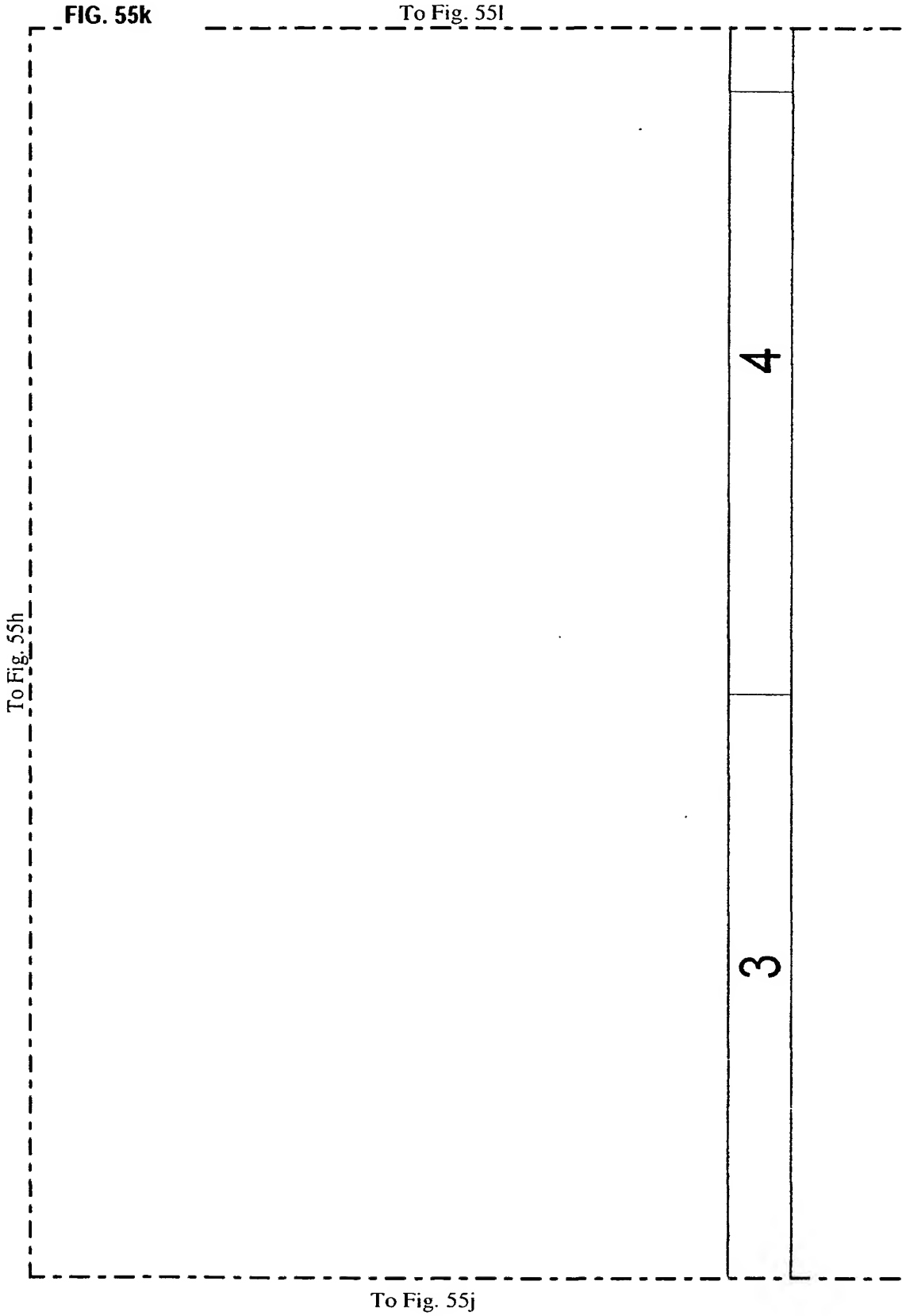


FIG. 55l

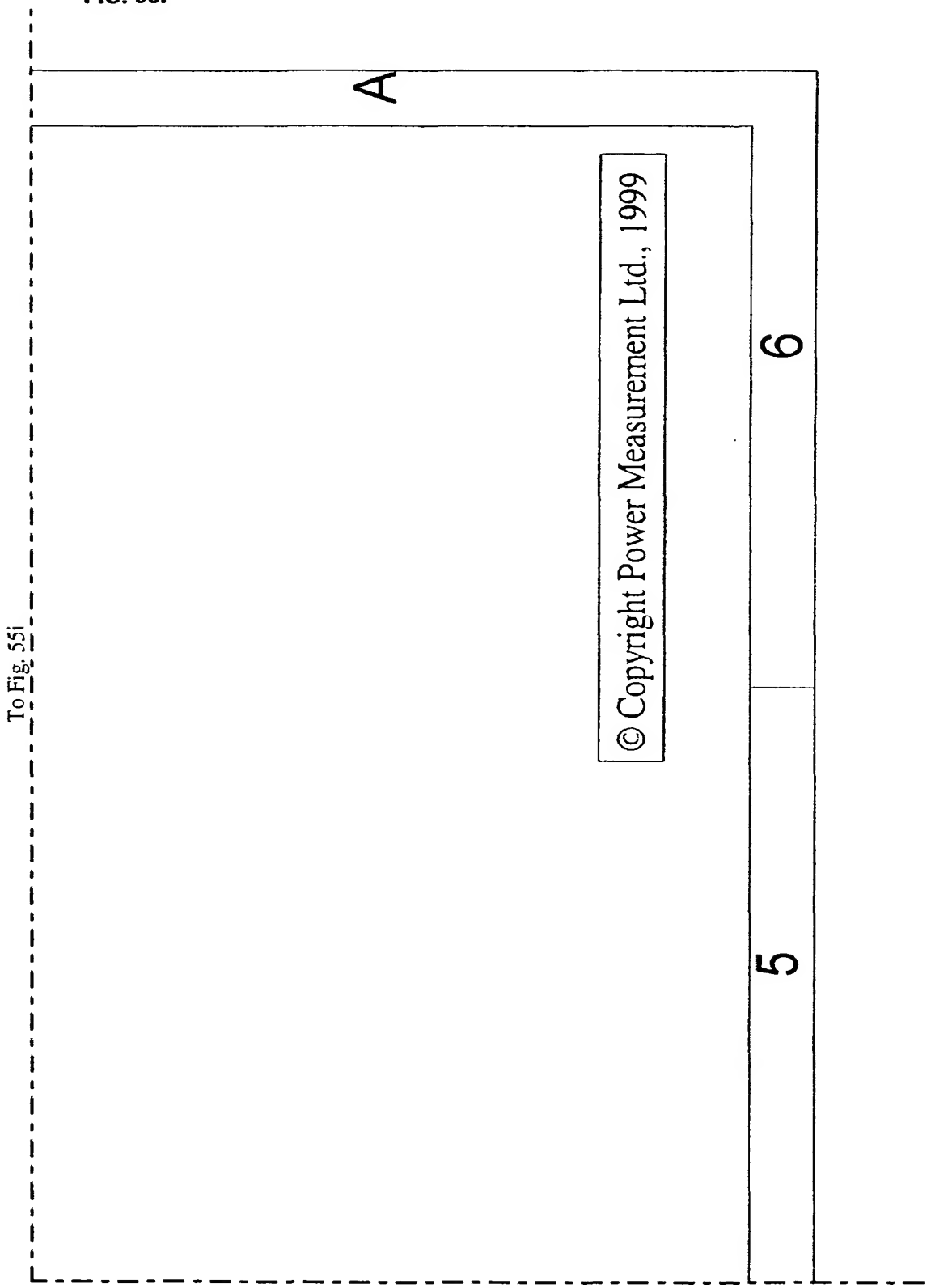

A
6
5
© Copyright Power Measurement Ltd., 1999
To Fig. 55i
To Fig. 55k

FIG. 56a

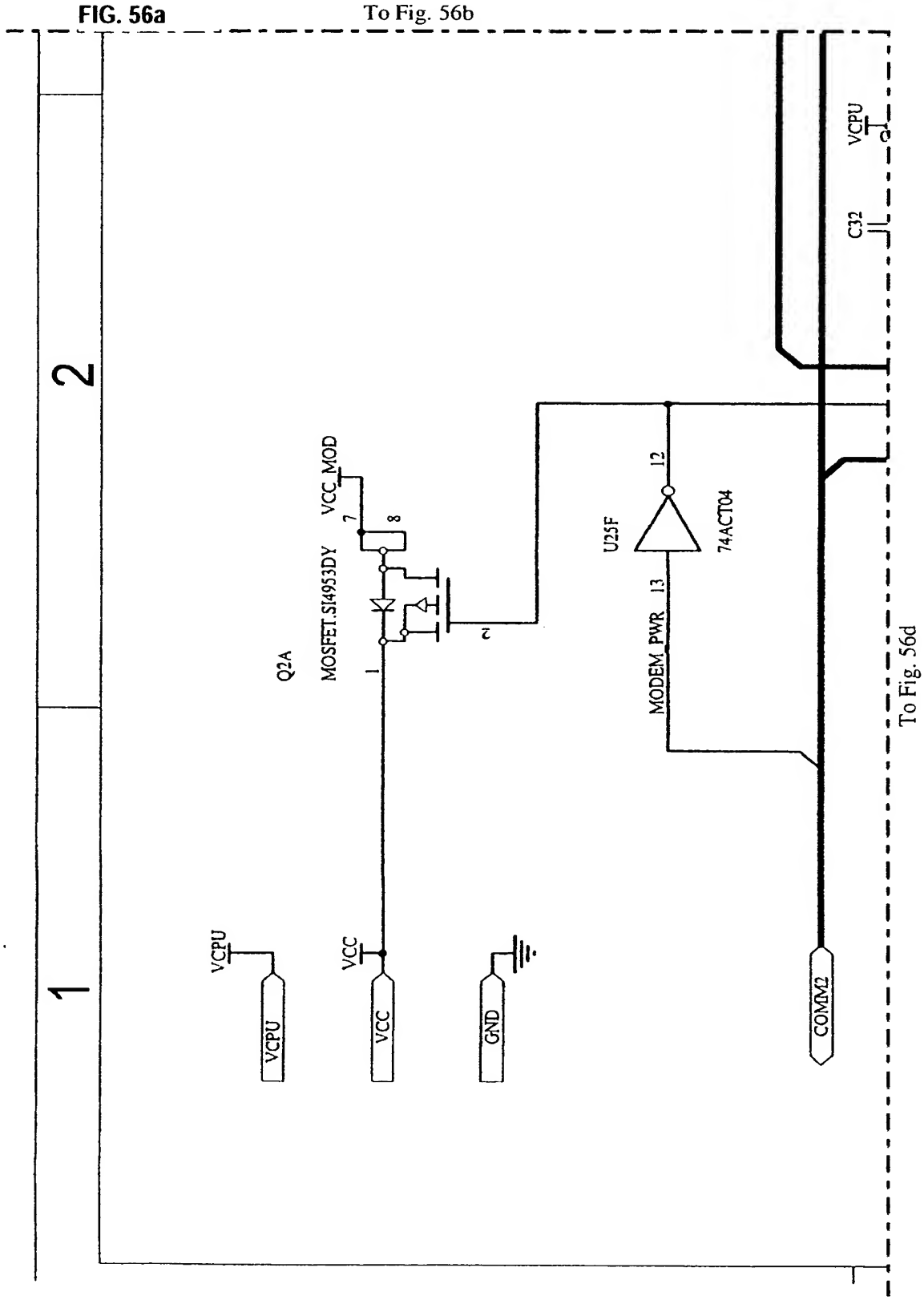

To Fig. 56b
2
1
VCPU
C32
VCC_MOD
7
8
MOSFET.SI4953DY
Q2A
1
2
U25F
12
74ACT04
MODEM_PWR
13
To Fig. 56d
VCPU
VCPU
VCC
VCC
GND
COMM2

FIG. 56b

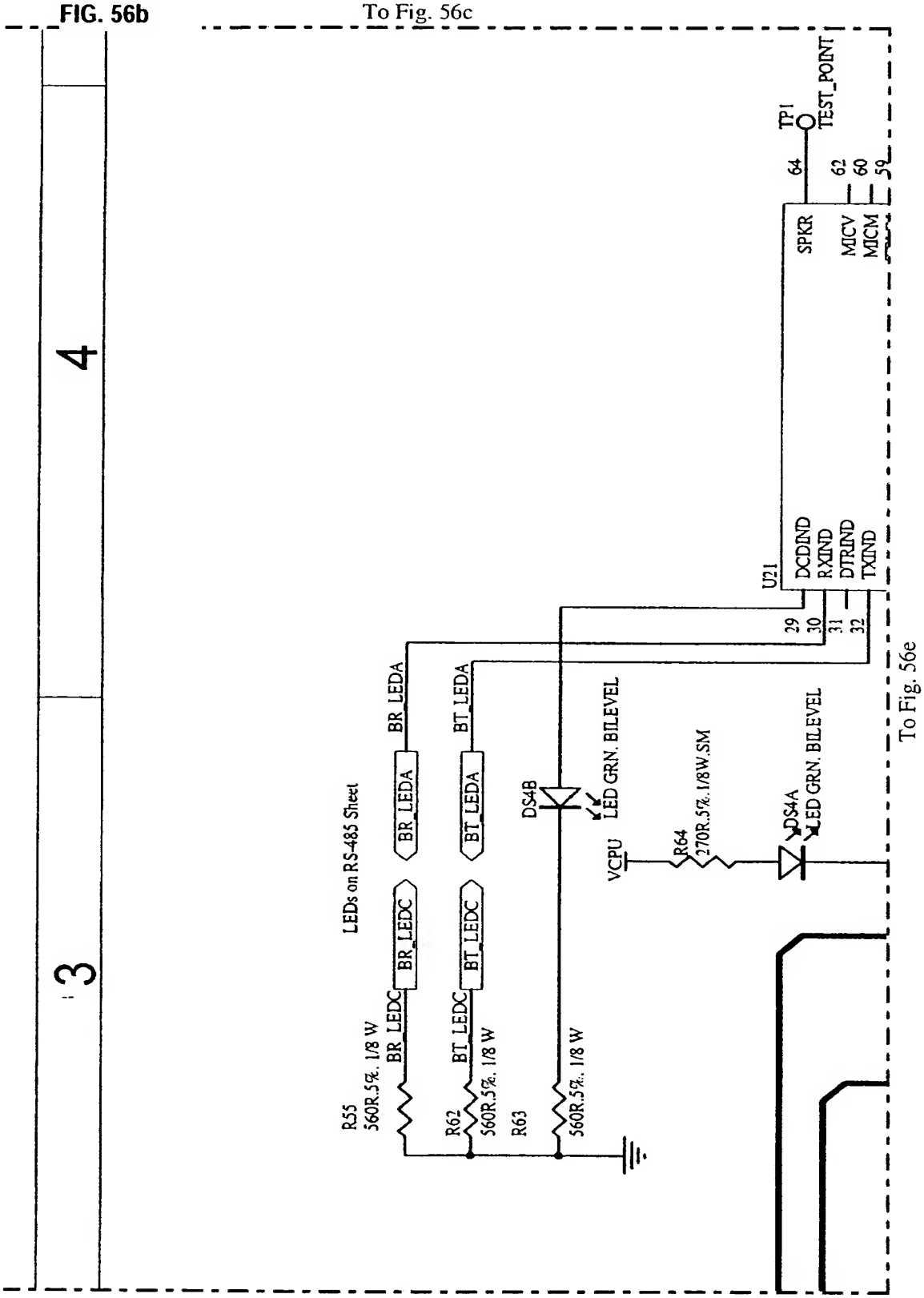

To Fig. 56c
TP1
TEST_POINT
64
62
60
59
SPKR
MICV
MICM
U21
DCDIND
RXIND
DTRIND
TXIND
29
30
31
32
BR_LEDA
BT_LEDA
DS4B
LED GRN. BILEVEL
DS4A
LED GRN. BILEVEL
VCPU
R64
270R.5%.1/8W.SM
LEDs on RS-485 Sheet
BR_LEDC
BT_LEDC
R55
560R.5%. 1/8 W
R62
560R.5%. 1/8 W
R63
560R.5%. 1/8 W
To Fig. 56e
To Fig. 56a

FIG. 56c

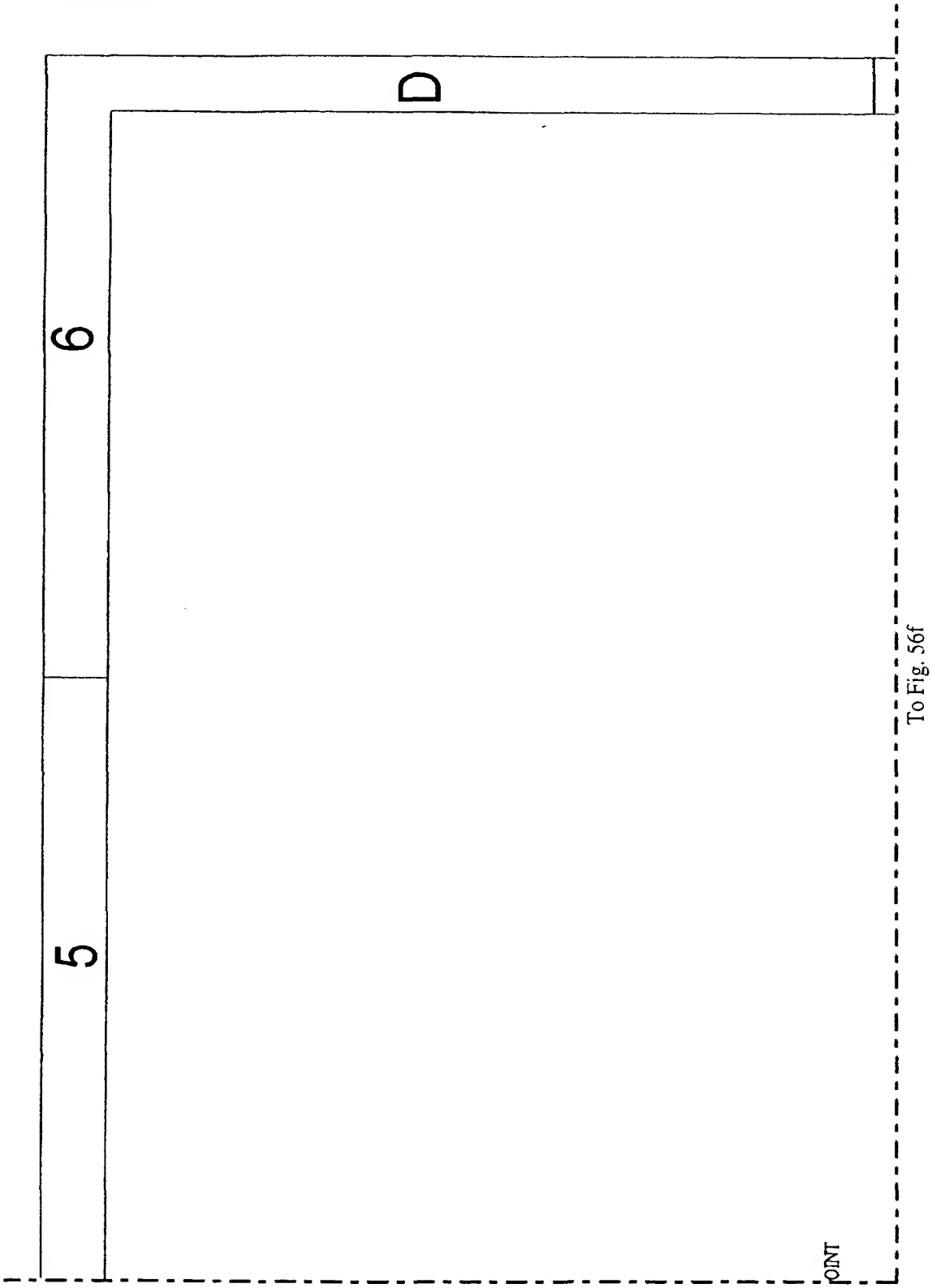
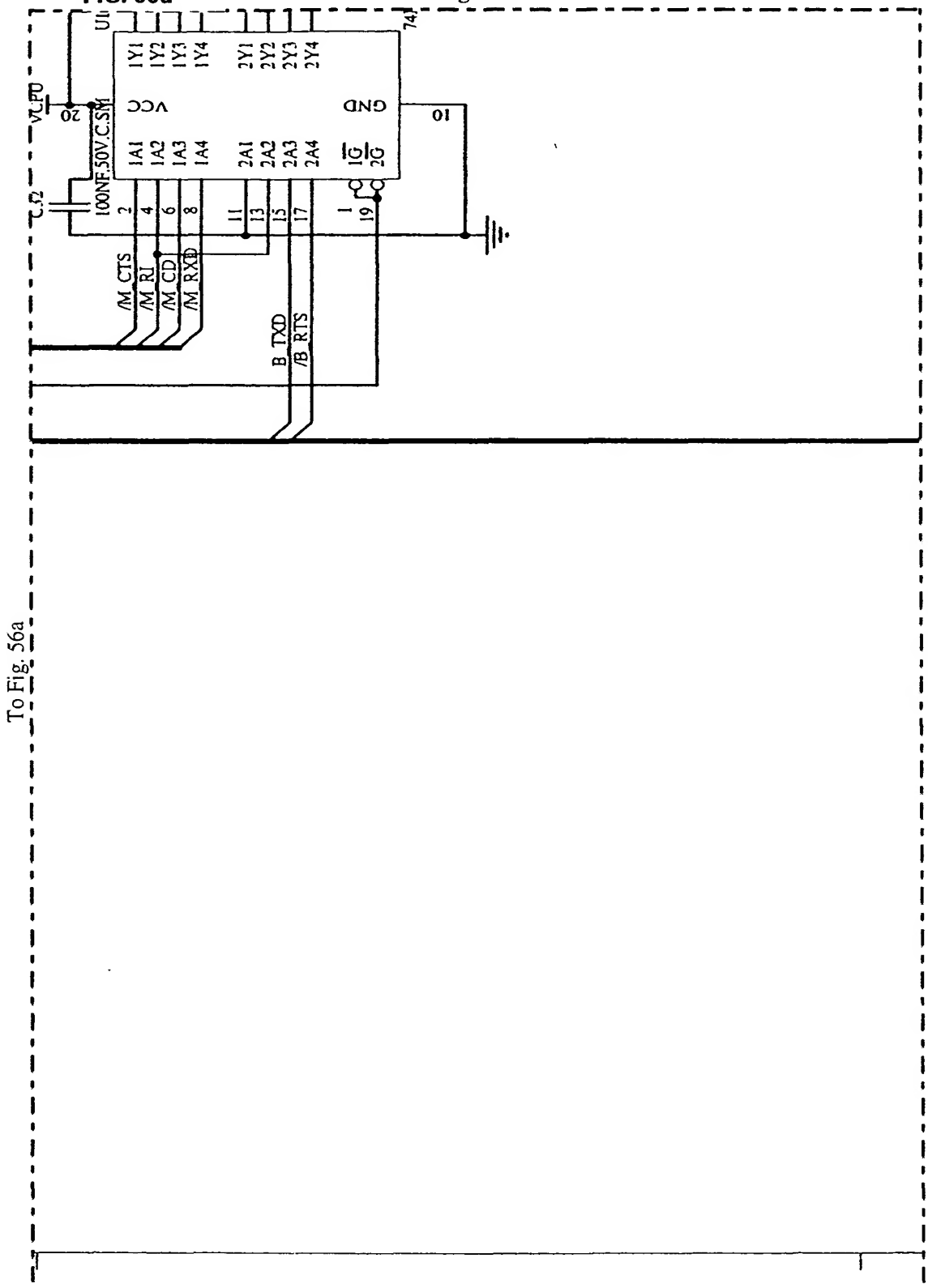


FIG. 56d

To Fig. 56e



To Fig. 56a

To Fig. 56g

FIG. 56e

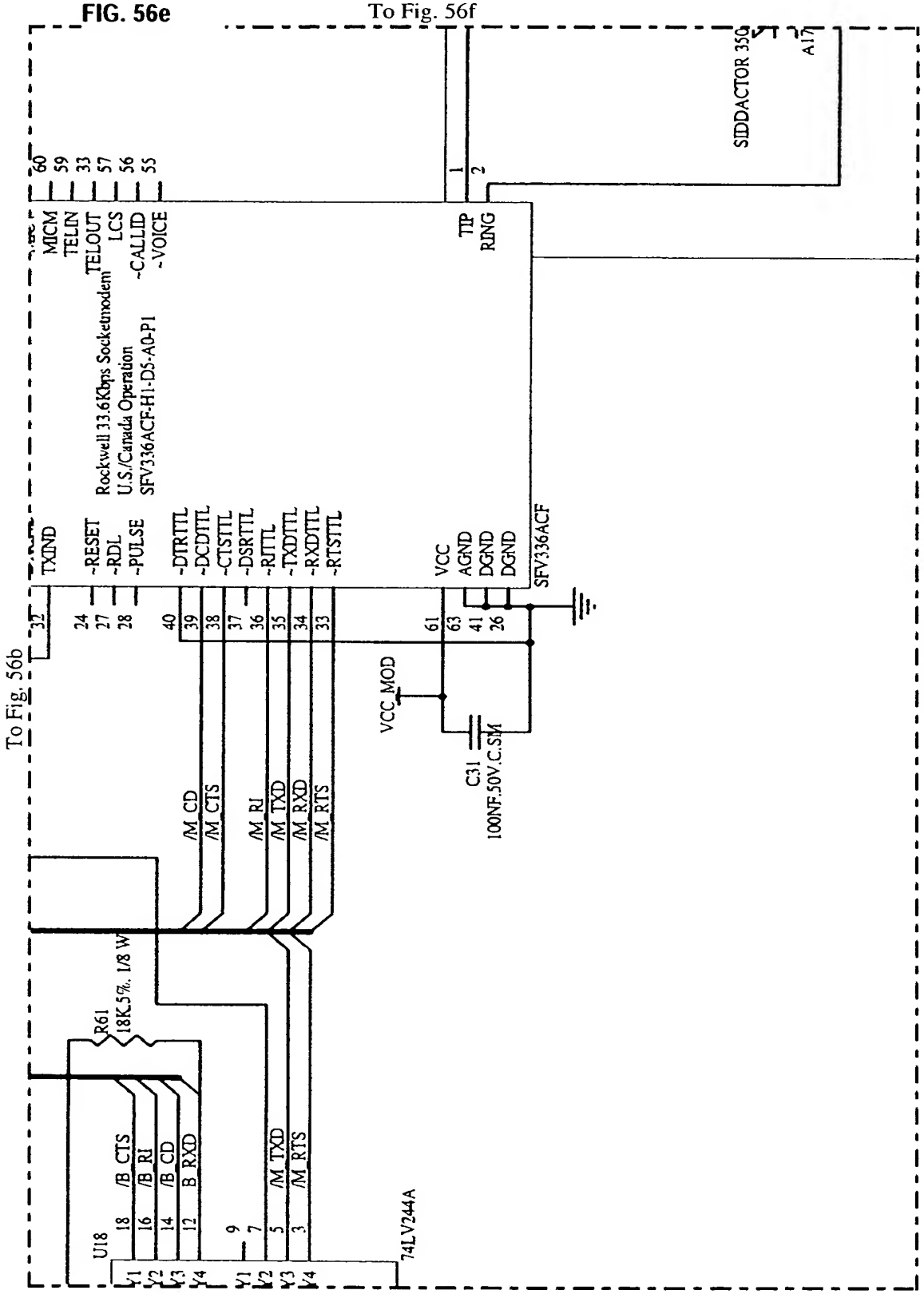
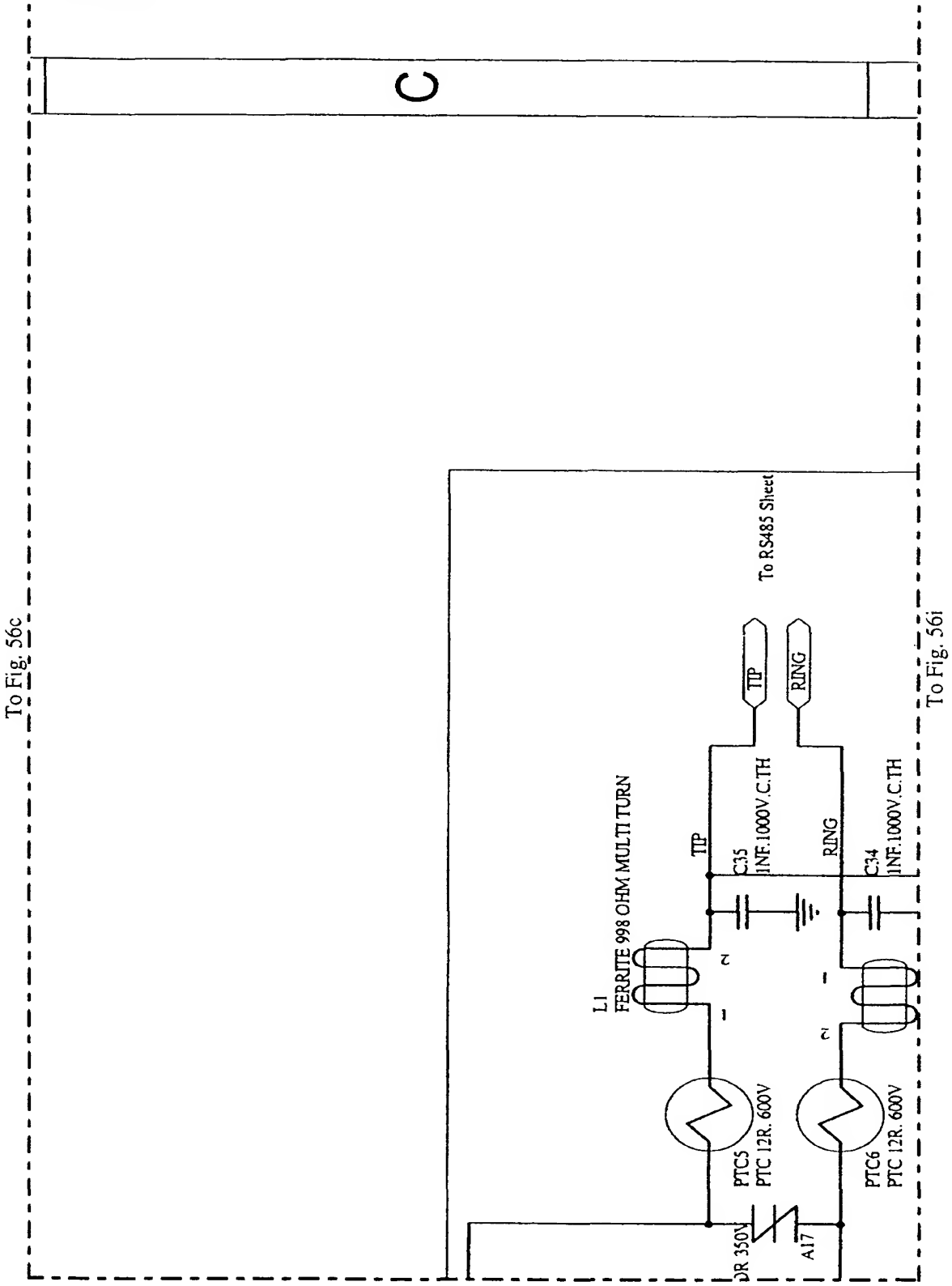

To Fig. 56f
SIDACTOR 350
A17
MICM
TELIN
TELOUT
LCS
-CALLID
-VOICE
TIP
RING
Rockwell 33.6Kbps Socketmodem
U.S./Canada Operation
SFV336ACF-H1-D5-A0-P1
TXGND
-RESET
-RDL
-PULSE
-DTRTTL
-DCDTTL
-CTSTTL
-DSRTTL
-RITTL
-TXDTTL
-RXDTTL
-RTSTTL
VCC
AGND
DGND
DGND
SFV336ACF
To Fig. 56b
VCC_MOD
C31
100NF.50V.C.SM
/M_CD
/M_CTS
/M_RI
/M_TXD
/M_RXD
/M_RTS
R61
18K.5%. 1/8 W
U18
/B_CTS
/B_RI
/B_CD
B_RXD
/M_TXD
/M_RTS
74LV244A
To Fig. 56h
To Fig. 56d

FIG. 56f



To Fig. 56e

FIG. 56g

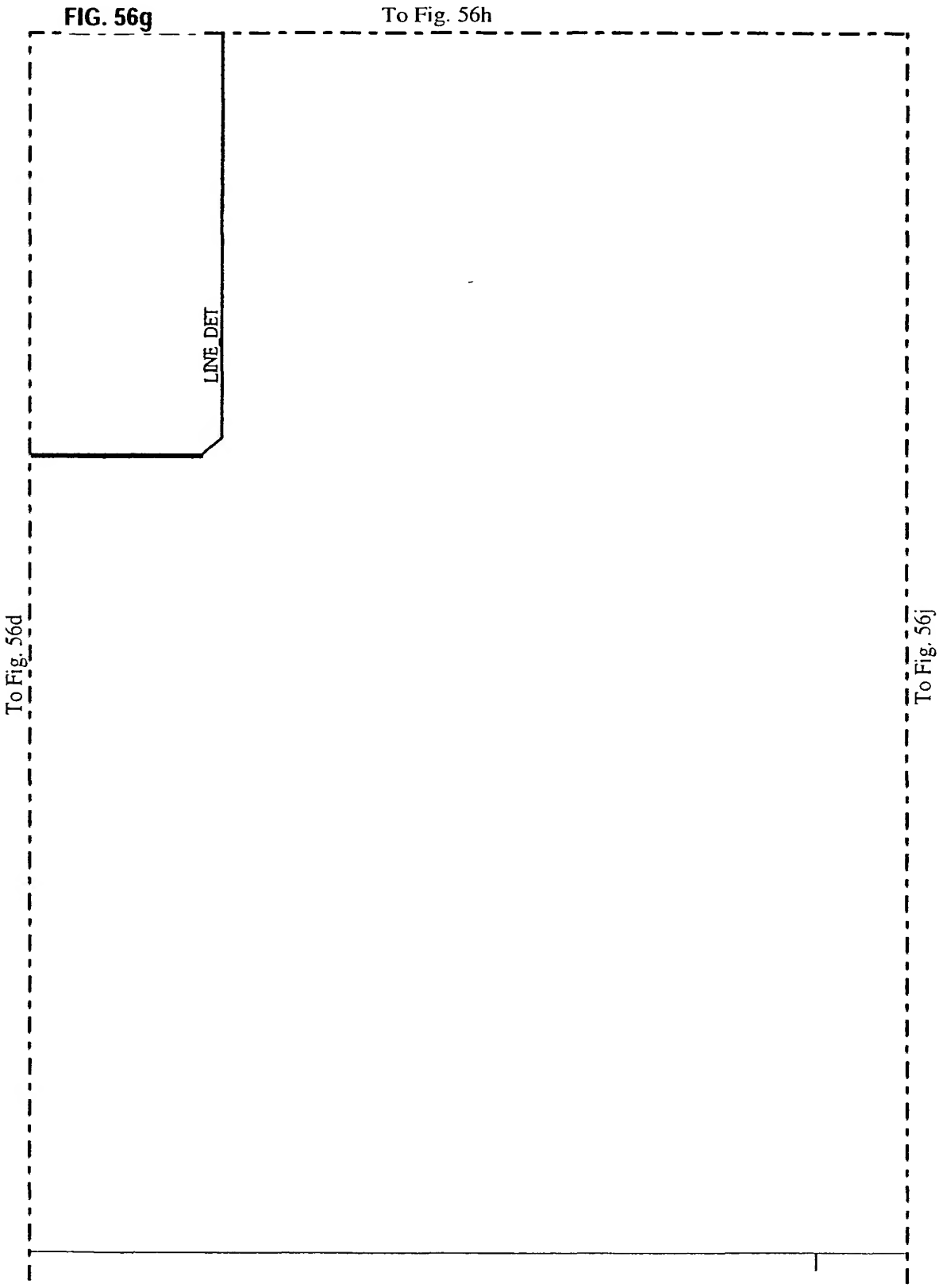


FIG. 56h

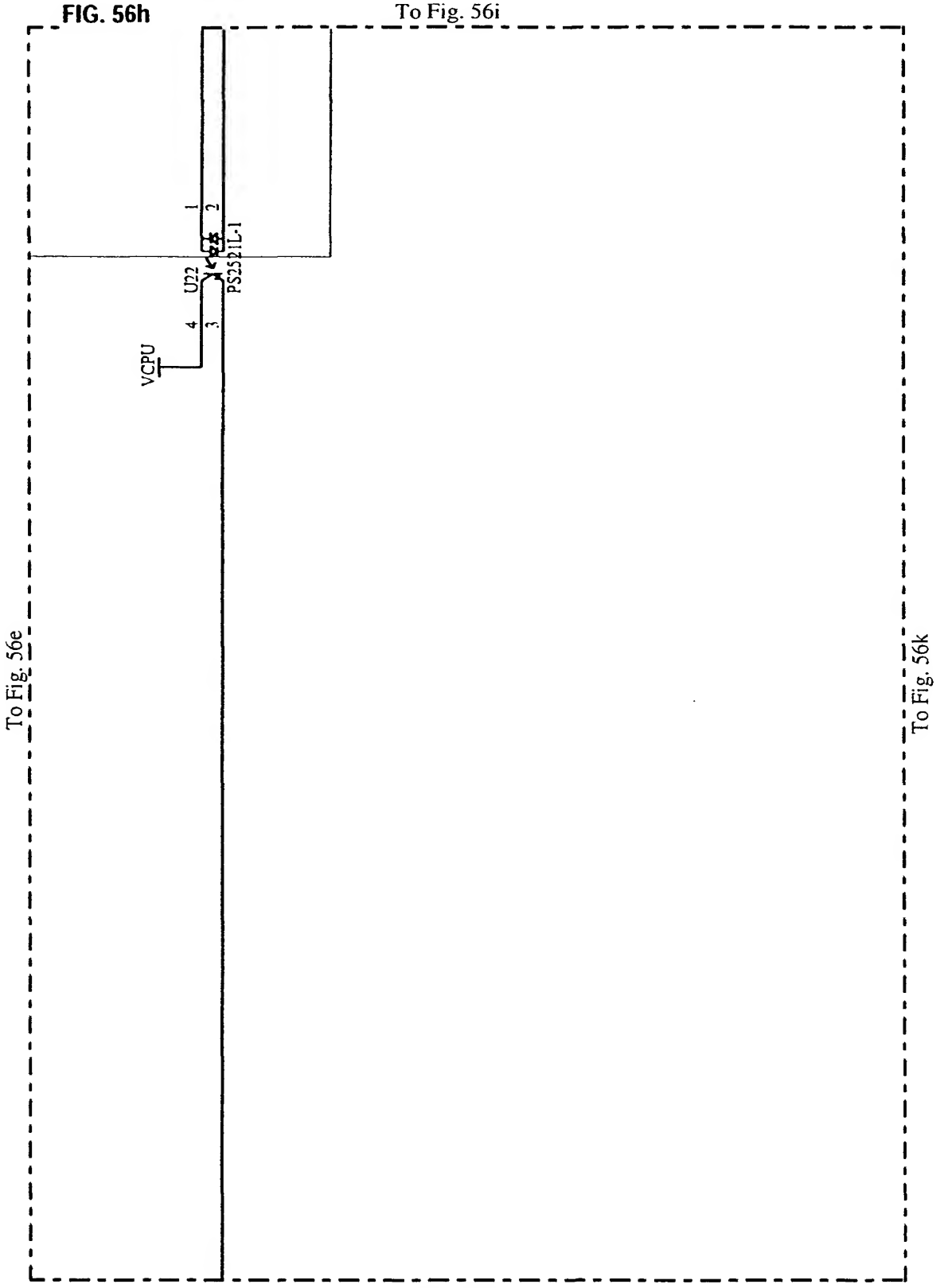
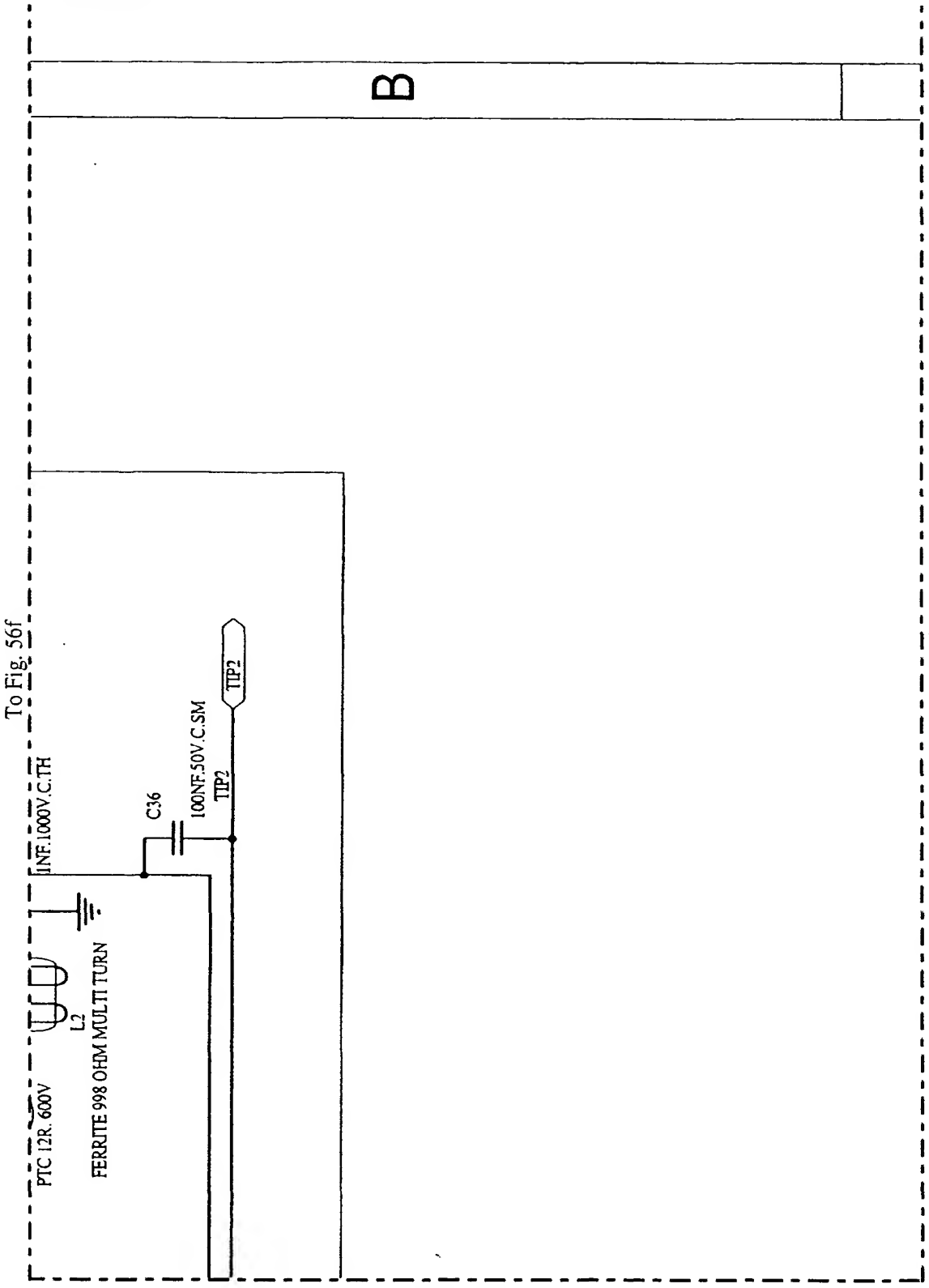

To Fig. 56i
To Fig. 56e
To Fig. 56k
To Fig. 56g
U22
PS2521L-1
1
2
3
4
VCPU

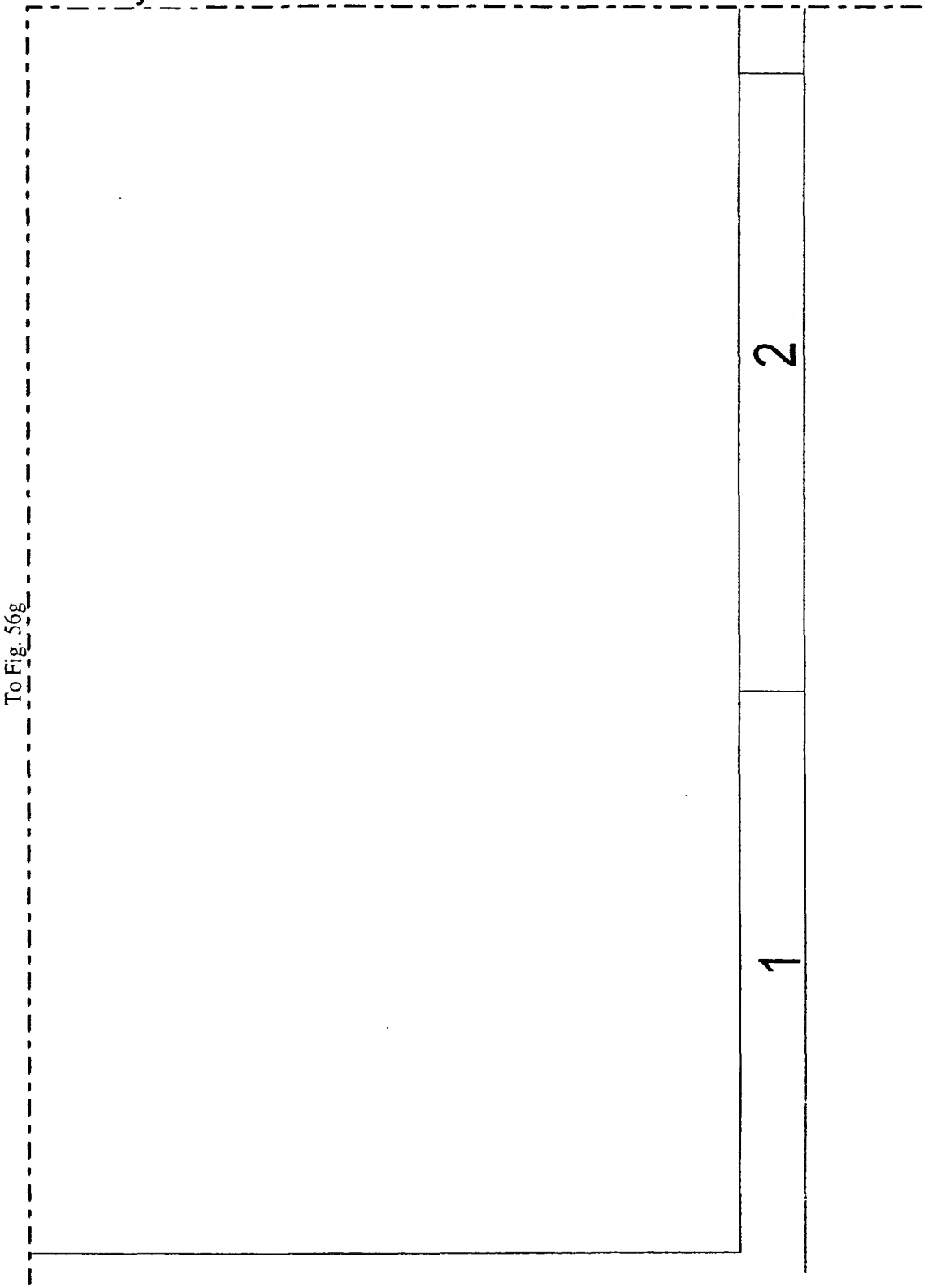
FIG. 56i



To Fig. 56h

FIG. 56j

To Fig. 56k



To Fig. 56g

FIG. 56k

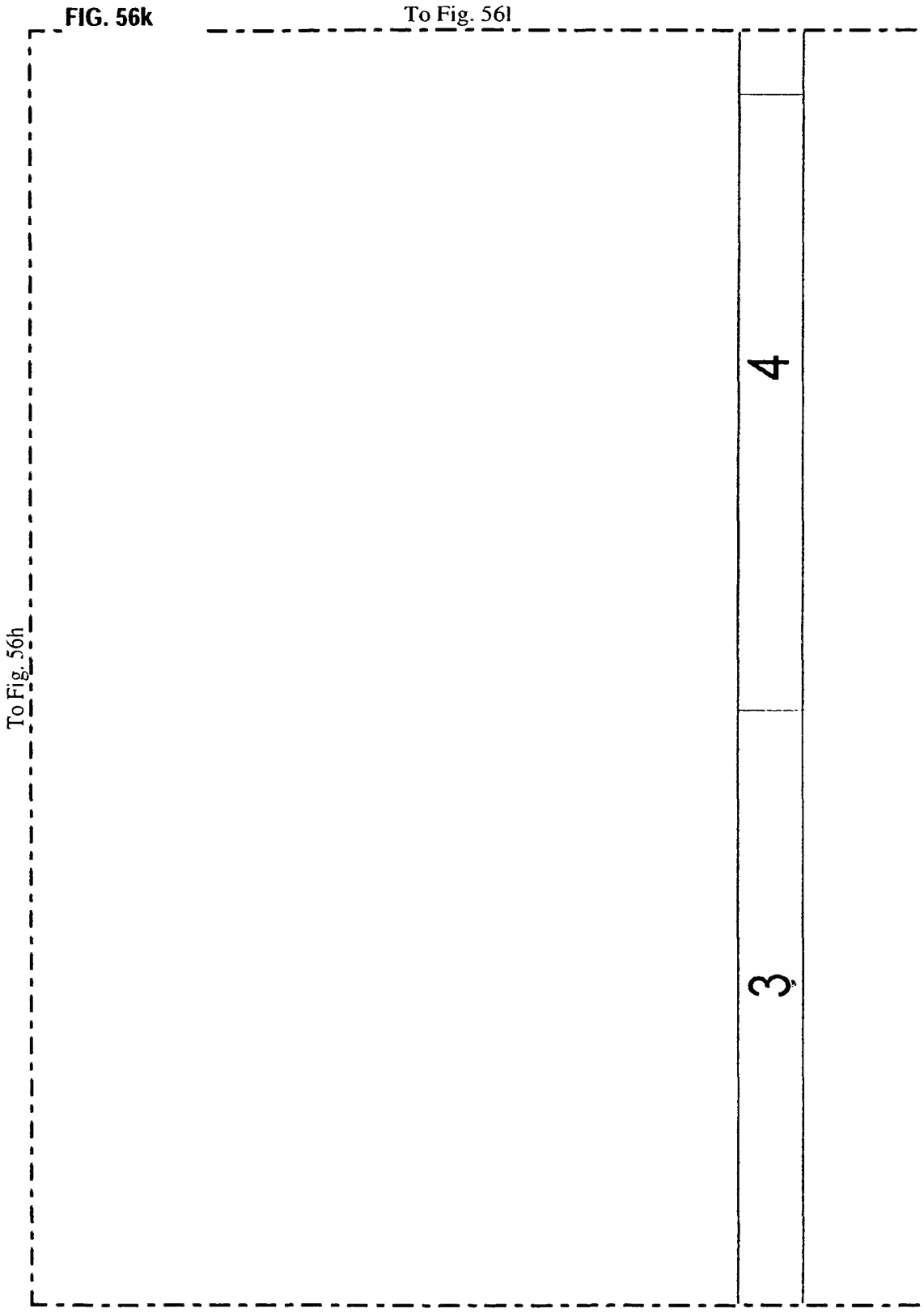
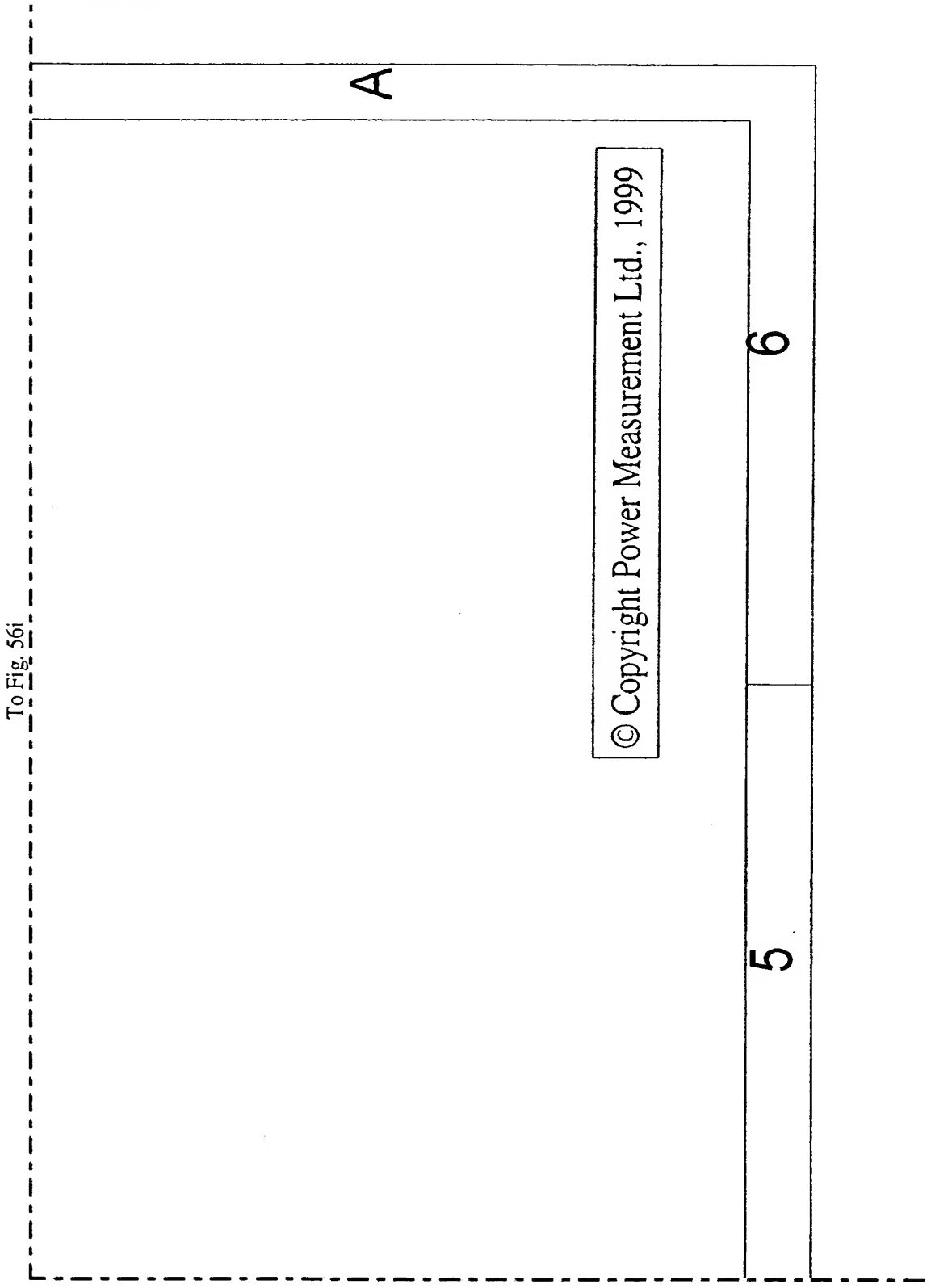


FIG. 56l


A
6
5
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To Fig. 56i
To Fig. 56k